Advanced MEMS Process for Wafer Level Hermetic Encapsulation of MEMS Devices Using SOI Cap Wafers With Vertical Feedthroughs

Mustafa Mert Torunbalci, Said Emre Alper, and Tayfun Akin

***Abstract*— This paper reports a novel and inherently simple fabrication process, so-called advanced MEMS (*aMEMS*) process, that is developed for high-yield and reliable manufacturing of wafer-level hermetic encapsulated MEMS devices. The process enables lead transfer using vertical feedthroughs formed on an Silicon-On-Insulator (SOI) wafer without requiring any complex via-refill or trench-refill processes. It requires only seven masks to fabricate the hermetically capped sensors with an experimentally verified process yield of above 80%. Hermetic encapsulation is achieved by Au–Si eutectic bonding at 400 °C, and the pressure inside the encapsulated cavity has been characterized to be as low as 1 mTorr with successfully activated thin-film getters. The pressure inside the encapsulated cavity can also be adjusted in the range of 1 mTorr-5 Torr by various combinations of outgassing and gettering options in order to satisfy the requirements of different applications. The package pressure is being monitored for the selected chips and is observed to be stable below 10 mTorr since their fabrication about 10 months ago. The shear strengths of several packages are measured to be as high as 30 MPa with average shear strength of 22 MPa, indicating a mechanically strong bonding. The robustness of the packages is tested by thermal cycling between 100 °C and 25 °C, and absolutely no degradation is observed in the hermeticity and the package pressure. The package pressure is also verified to remain unchanged after storing the packages at a high storage temperature of 150 °C for 24 h. Furthermore, the packaged chips are observed to withstand a high temperature shock test performed at 300 °C for 5 min, at the end of which the characteristics of the encapsulated sensor indicates that the package still remains hermetic (no detectable leaks) and also the package pressure remains constant at ∼20 mTorr. [2014-0338]**

***Index Terms*— Microelectromechanical systems (MEMS), wafer level hermetic encapsulation, Au-Si eutectic bonding, vertical feedthroughs, advanced MEMS process (aMEMS).**

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M. M. Torunbalci and S. E. Alper are with the Middle East Technical University-Microelectromechanical Systems Research and Applications Center, Middle East Technical University, Ankara 06531, Turkey (e-mail: mtorunbalci@mems.metu.edu.tr; said@metu.edu.tr).

T. Akin is with the Middle East Technical University-Microelectromechanical Systems Research and Applications Center, Department of Electrical and Electronics Engineering, Middle East Technical University, Ankara 06531, Turkey (e-mail: tayfun-akin@metu.edu.tr).

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I. Introduction

The progress in the microelectromechanical systems (MEMS) has a great potential for the development of smart, small-sized, low cost, and reliable sensors for a large variety of industrial applications. Some of these MEMS devices such as the pressure and gas flow sensors have a direct physical contact to the outside world, whereas a great variety of the MEMS devices such as the inertial sensors, resonators, and infrared detectors must be isolated from operating environment by encapsulating them in the hermetically sealed packages [1], [2]. Therefore, hermetic encapsulation is essential for many MEMS devices, and is a major obstacle for successful commercialization.

Hermetic encapsulation can be achieved either at the die or wafer level. Die level encapsulation requires individual process for each MEMS device, which not only increases the packaging cost and labor time but also decreases the process yield and reliability. Wafer level encapsulation provides a better solution in all the above aspects, by encapsulating all the MEMS devices located on the wafer simultaneously by using well-known techniques, such as thin film encapsulation or wafer bonding [3]. Thin film encapsulation requires deposition of various thin films on top of MEMS sensor wafer, forming a thin but hermetically-sealed capping layer. This technique provides a low-cost packaging solution that eliminates the need for a separate cap wafer and bonding equipment [4]–[7]. However, it typically requires additional mechanical protection [7] in order to increase the robustness of the thin capping layer, and is also not compatible with conventional getter deposition techniques, limiting the cavity pressure to levels that are not sufficient for many MEMS devices. On the other hand, hermetic sealing by wafer bonding employs a separate cap wafer for the sealing purposes, which provides perfect mechanical robustness for the protection of encapsulated MEMS sensors, and also allows very low package pressures with the use of thin film getters.

Encapsulation, however, is just the first half of the packaging process, whereas the second half is the transfer of electrically conductive leads of the MEMS sensor to the outside world without degrading the hermeticity of the encapsulation. A widely used encapsulation method is the bonding of sensor and cap wafers with the help of glass-frit, which

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is successful in sealing step heights caused by laterally transferred sensor leads; however, it requires high bonding temperatures (>430°C) and wide bond rings (>150μm) [8]. The temperature and bonding area can be reduced with the use of metal-based sealing alloys [9]–[11] instead of the glass-frit material; however, these metals must then be isolated from the electrical leads of the structures by an additional dielectric layer, increasing the complexity and cost of the process especially when the leads are laterally transferred to outside of the package. Moreover, the step coverage of metal-based alloys is not as good as the glass-frit, since the thickness of these alloys is typically limited to few micrometers, mostly due to their high stress. There are also examples of vertically-transferred sensor leads in the literature [12]–[18]. These approaches typically require the drilling of the silicon or glass substrates by using a laser [12], DRIE [13]–[15], or wet etching [16], [17] and then hermetic filling of these trenches with thermal oxidation [15], metal bumps/patterning [16], [17], glass reflow [13], [14], or metal electroplating [12], [18]. Therefore, they either suffer complex process steps such as void-free hermetic-filling of the feedthrough openings [12], [15] or trench-refill processes [13], [16], [18]. Another challenge with the vertical feedthrough processes is to ensure precise control of the thicknesses and the relative offsets of the sealing material, sensor leads, sealing regions, and vertical feedthroughs [18], in order to achieve the sealing and the lead transfer simultaneously.

In summary, it is desirable to achieve wafer-level hermetic encapsulation of MEMS devices, preferably enabling low process temperatures, eliminating any step-coverage issues by employing vertical feedthroughs, and yet being simple, high-yield, and robust. This paper reports such a wafer level hermetic encapsulation process, called as the Advanced MEMS (*aMEMS*) process, which meets the abovementioned requirements by using an Silicon-On-Insulator (SOI) cap that is micromachined with the well-known and widely-used MEMS fabrication techniques [19], [20]. The proposed method has been successfully demonstrated to be completed by only seven fabrication masks including the masks for the sensor fabrication, to have a packaging yield above 80% deduced from the experiments performed on a number of fabricated wafers, and to provide cavity pressures as low as 1 mTorr which is observed to remain stable below 10 mTorr since the fabrication of the first prototypes around 10 months ago. The packages fabricated with the proposed method are also experimentally verified to be mechanically and thermally robust, as they successfully pass harsh shear and temperature tests without a detectable degradation in the leak rate and package pressure.

II. Package Design and Fabrication

A. Package Design

Fig. 1 shows the three-dimensional (3D) view of a sample MEMS structure encapsulated with the proposed *aMEMS* process. The SOI cap wafer forms the sealing wall as well as the package roof surrounding the MEMS structure, and it is bonded to the glass substrate with the help of a metal sealing material. The sealing material and sensor leads can be formed

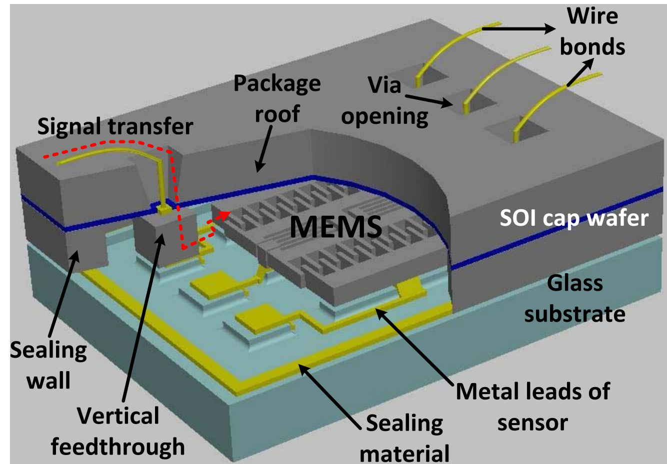


Fig. 1. Three-dimensional (3D) view of the *aMEMS* process.

using the same metal without requiring an additional mask. Sensor leads are pressed by conductive vertical feedthroughs formed on the SOI cap wafer, and signal transfer is achieved through the wire bonds connected to the exposed faces of the vertical feedthroughs as in [21], eliminating the need for via-refill or trench-refill process steps.

B. Fabrication

Fig. 2 shows the major fabrication steps for the *aMEMS* process. The proposed process requires only seven masks to fabricate the hermetically-capped sensors and starts with an SOI wafer on which the via openings are formed by a KOH wet etching process (Fig. 2-a). The handle layer of the SOI wafer not only defines the thickness of the package roof in Figure 1 but also specifies the dimensions of the vertical feedthroughs. The 30 nm/300 nm Cr/Au pad metals are formed inside the via openings by using the lift-off technique for wire bonding purposes (Fig. 2-b). The sealing walls and vertical feedthroughs are both made of highly doped silicon, and they are simultaneously formed by etching the device layer of the SOI cap wafer with DRIE (Fig. 2-c). The thickness of the device silicon layer determines the cavity depth. Two different cavity depths are selected in this study, as 100 μm and 300 μm, in order to check the effect of different cavity volumes on the package pressure. Finally, thin film getters are deposited inside the cavities by using a custom designed and formed shadow mask. The getter material consists of 1 μm thick 4.3 mm × 2.6 mm titanium film which can be deposited either with evaporation or sputtering techniques. The titanium getter is inherently activated during the wafer level encapsulation process with Au-Si eutectic bonding, improving the package pressure.

The corresponding sensor wafer in Fig. 2-d is fabricated by using a modified silicon-on-glass (M-SOG) technology as in [22], where 35 μm thick silicon resonators are suspended over the glass substrate. The sealing material and the sensor leads are formed simultaneously using a 30 nm/150 nm thick Cr/Au metal layer. This ensures simultaneous Au-Si eutectic bonding between "the sealing material and the sealing wall"

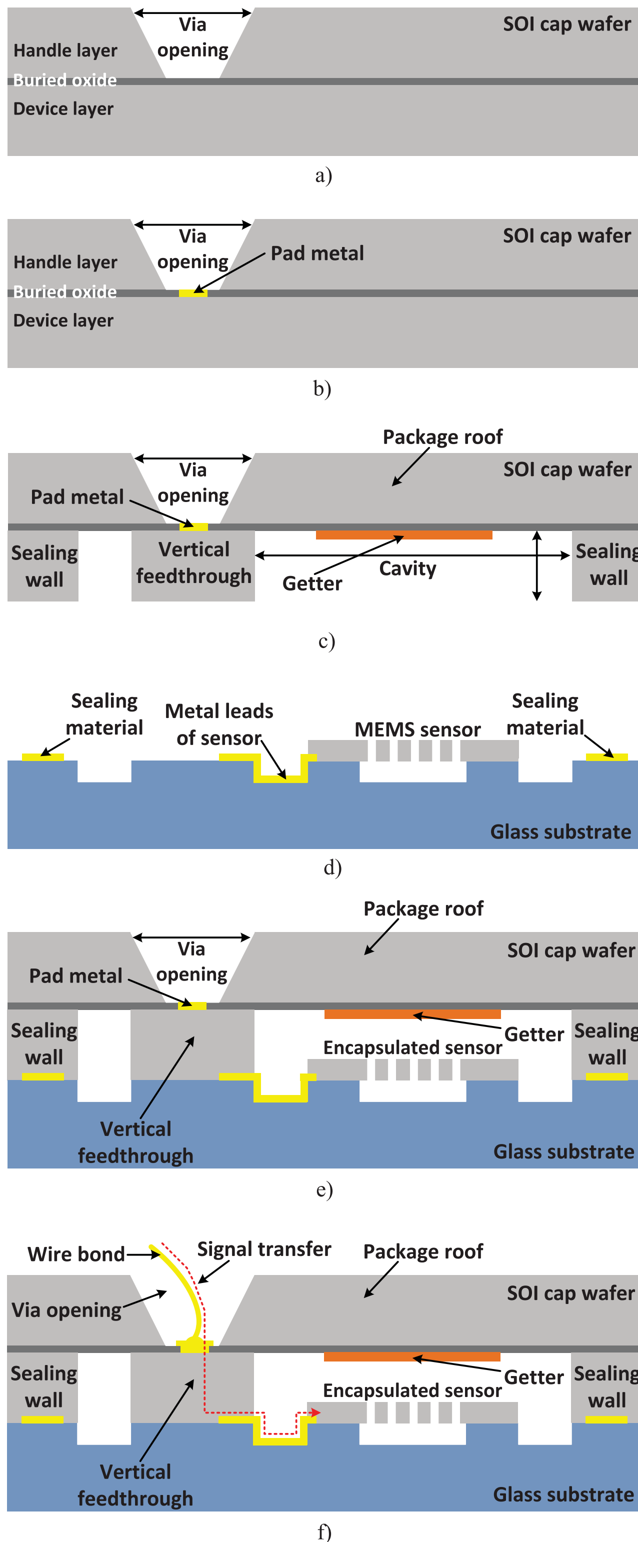


Fig. 2. Major fabrication flow for the *aMEMS* process. a) Formation of via on the handle layer with KOH. b) Pad metals are formed after etching the buried oxide with lift off. c) Simultaneous formation of sealing walls and vertical feedthroughs on the device layer with DRIE, and the deposition of thin film getter. d) Fabrication of MEMS sensor wafer using M-SOG technology. e) Wafer level hermetic encapsulation with Au-Si eutectic bonding. f) Wire bonding for the signal transfer.

as well as "the sensor leads and the vertical feedthroughs" during the final encapsulation step, as shown in Fig. 2-e. The Au-Si eutectic bonding is performed at 400°C by using a

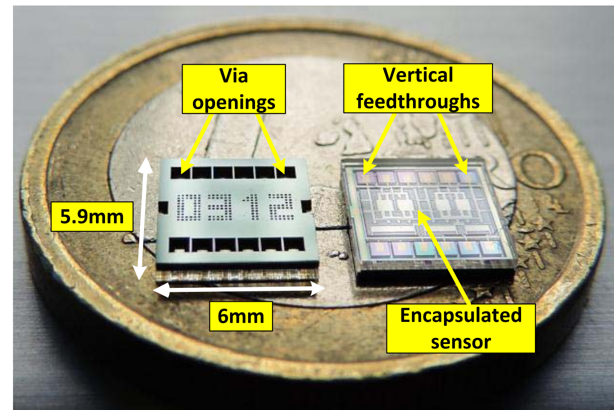


Fig. 3. Photographs of hermetically packaged dies from the top (on the left) and bottom (on the right) faces, fabricated using the *aMEMS* process.

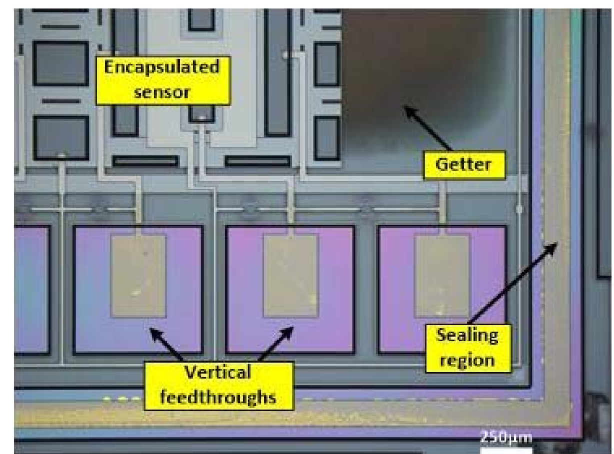


Fig. 4. The magnified view of the sealing region, vertical feedthroughs, thin-film getters, and the encapsulated sensor as seen through the bottom face of the packaged chip.

bond pressure around 3 MPa. After the encapsulation process, the vertical feedthroughs are simply accessed by wire bonds, eliminating any need for via-refill as shown in Fig. 2-f [21].

C. Fabrication Results

Fig. 3 shows the photographs of hermetically packaged dies from the top and bottom faces, fabricated using the *aMEMS* process. The die size of the hermetically sealed packages is 5.9 mm × 6 mm for this particular design. Fig. 4 presents the magnified view of the sealing region, thin-film getter, encapsulated sensor, and vertical feedthroughs, as seen through the bottom face of the packaged chip. The amount of the Au-Si eutectic flow can be adjusted by optimizing the bonding pressure. Fig. 5 shows the wirebonds that are used to electrically connect the pads of a fabricated chip to the pads of a ceramic package.

Fig. 6 presents the SEM pictures of the MEMS devices fabricated using the *aMEMS* process, showing the details of the vertical feedthroughs, sealing walls, via openings, and encapsulated sensor. The current pitch size of the fabricated vertical feedthroughs and via openings is selected to be 700 μm, in order to stay on the safe side during the

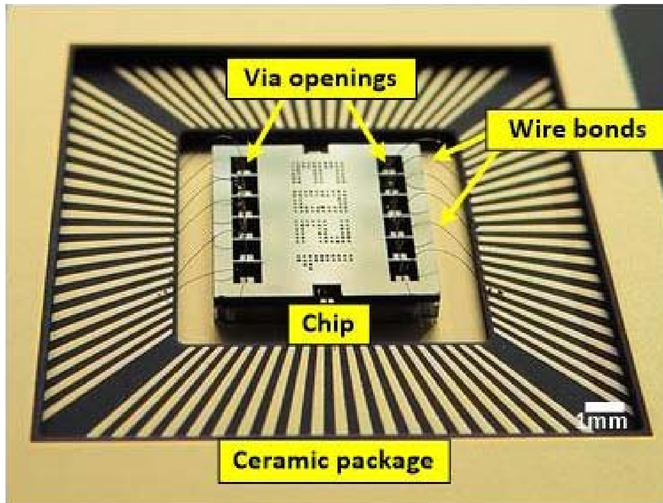


Fig. 5. The photograph of a fabricated chip mounted in a ceramic package.

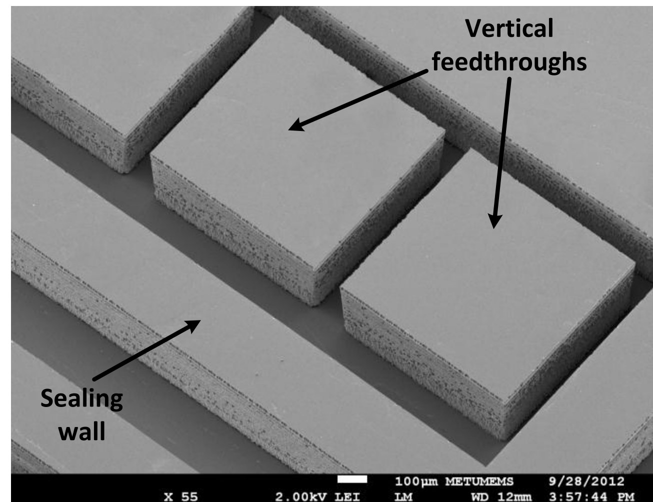
initial demonstration of the concept. This pitch size can be easily reduced down to 350 μm by reducing the thickness of the handle layer of the SOI cap wafer [23], [24]. Further reduction is also possible as described in [24].

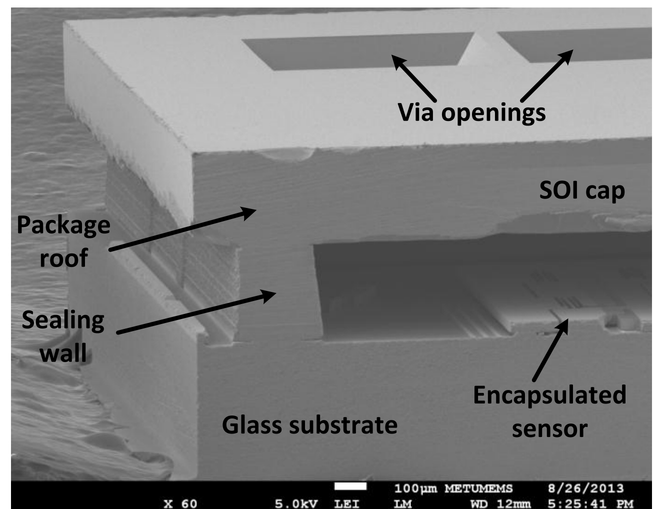
III. Characterization Results

Various tests are performed on the packages fabricated with the *aMEMS* process in order to measure the vertical feedthrough resistance, package pressure, production yield, bonding strength, and thermal robustness.

A. Vertical Feedthrough Resistance

The feedthrough resistance is a critical parameter for various MEMS applications, and it should be low enough to prevent any loss during the signal transfer from the sensor to the outside world. As the vertical feedthroughs are made by etching the device silicon layer of the SOI wafer in this study, the SOI device layer is selected to be low resistive silicon (<0.005 Ω.cm); this layer is then bonded to the metal leads of the sensor forming a low resistive Au-Si ohmic contact. The electrical resistance of the vertical feedthrough is measured using the setup in Fig.7. The measurements include the total feedthrough, contact, and line resistance, which adds up to 150Ω. Feedthrough resistance can be easily estimated from the doping level of silicon and the dimensions of the vertical feedthroughs, which is in less than 1Ω. Similarly, the line resistance is estimated to be less than 5Ω. Subtracting the theoretical values of the line and feedthrough resistances from the total resistance measurement leaves a contact resistance in the order of 60-150Ω which is acceptable for a large variety of MEMS applications that do not require RF and higher frequencies. This value is believed to be improved by optimizing the bonding recipe.





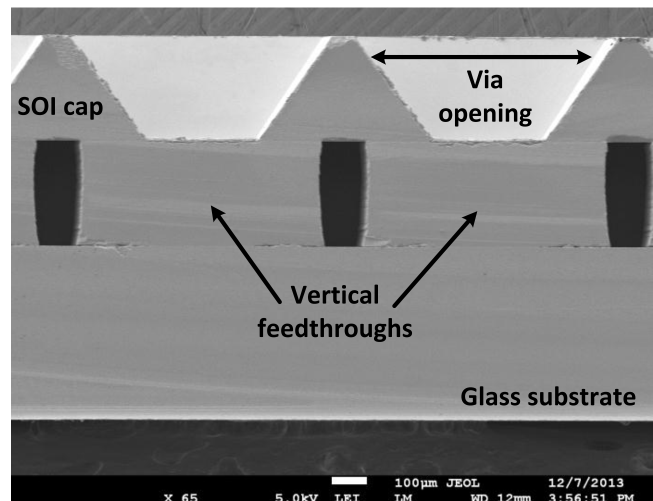


Fig. 6. SEM pictures of the MEMS devices fabricated using the *aMEMS* process, showing the details of the vertical feedthroughs, sealing walls, via openings, and encapsulated sensor.

B. Package Pressure

The package pressure is measured by tracking the quality factors of benchmark resonators encapsulated with the *aMEMS* process.

The quality factor directly depends on the air damping that provides a direct measure of the pressure change inside the encapsulated cavity. The resonators on the MEMS sensor wafer are characterized before and after the

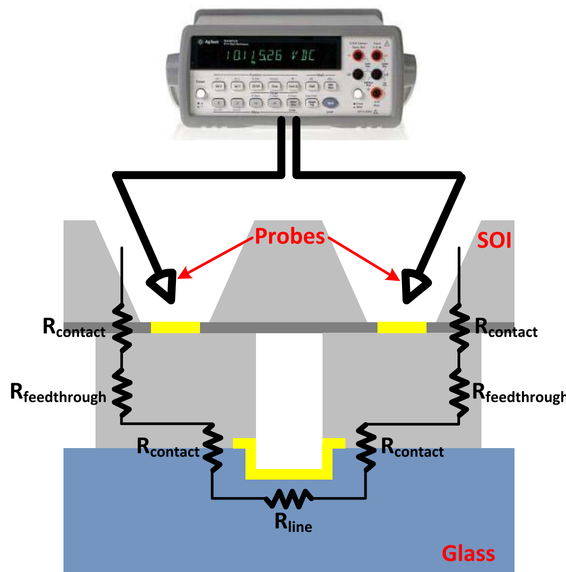


Fig. 7. Measurement setup for the vertical feedthrough resistance.

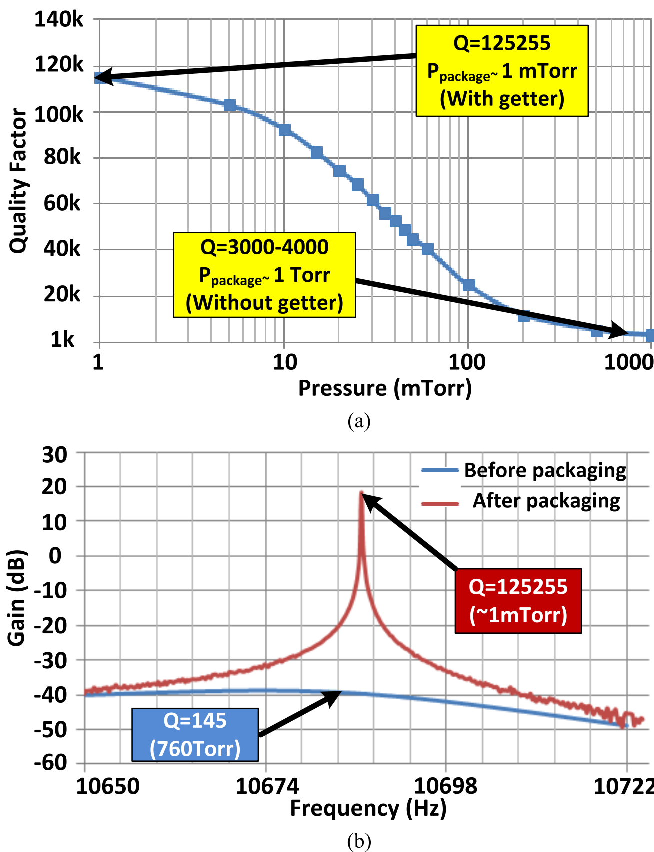


Fig. 8. Test results of the fabricated prototypes: (a) Variation of the quality factor of the MEMS resonator tested at different pressure levels in a controlled pressure environment before the wafer-level packaging process. (b) Resonance characteristics of a MEMS resonator before and after wafer-level packaging, showing a measured quality factor of 125,255 corresponding to a cavity pressure around 1 mTorr with the help of successfully activated thin-film getters.

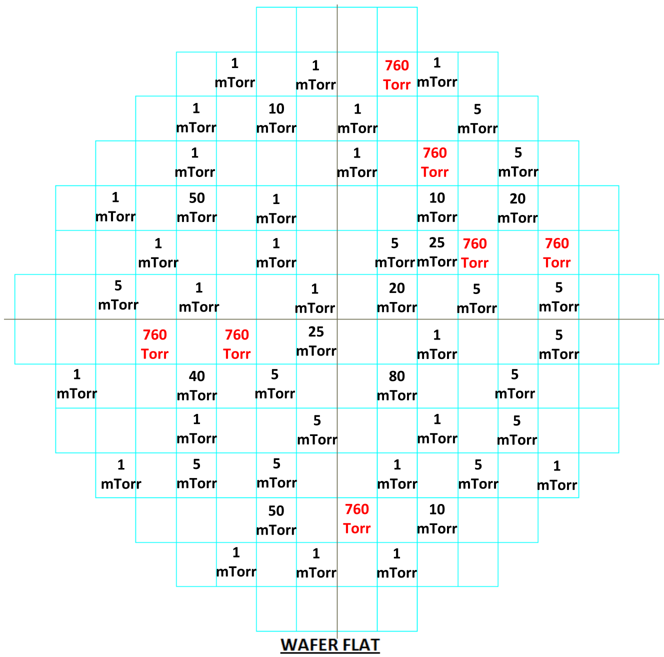


Fig. 9. Wafer map showing the successfully packaged as well as the failed sensor dies. Among randomly selected 55 sensors, 87% have a cavity pressure lower than 100 mTorr, 74% lower than or equal to 10 mTorr, and 42% as small as 1 mTorr.

encapsulation process. First, the uncapped MEMS sensor wafer is placed inside a controlled pressure chamber where the pressure can be adjusted in the range of 10 μTorr to 10 Torr. The resonance characteristics of the resonators located on this wafer are obtained at different pressures using an Agilent 35670A Dynamic Signal Analyzer and an external readout circuit. The quality factors of the resonators are then extracted from these measurements. Figure 8-a presents the variation of the quality factor of a benchmark MEMS resonator at different pressure levels, as well as the measured Q-factors of two identical resonators (with and without getter inside the cavity) after the packaging process. Fig. 8-b shows the resonance characteristics of a benchmark resonator before and after wafer-level packaging, showing a measured quality factor of 125,255 corresponding to a cavity pressure around 1 mTorr with the help of successfully activated thin-film getters. Quality factors of MEMS resonators packaged on the same wafer typically exceed 100,000 as in Fig. 8-b, which is believed to be limited by the mechanical design rather than the package pressure.

Fig. 9 presents the wafer map showing the successfully packaged as well as the failed sensor dies among randomly selected 55 dies. The packaging yield (indicated by the vacuum level below 100 mTorr) is above 87%. More than 74% of the encapsulated cavities have an internal pressure less than 10 mTorr and 42% being as low as 1 mTorr, owing to the custom-developed and successfully-activated getter material. The failure in the hermeticity of the packages may be due to two reasons. The first failure mode, maybe the most dominant, is the quality of the Au-Si eutectic bonds. Any failure occurred during the patterning of the Cr/Au bond ring may affect the quality of the Au-Si eutectic bonding and degrade the hermeticity of the packages. Even if the Cr/Au bond ring is properly patterned, sealing may not be very strong due to a contamination across the sealing area. The second failure mode is the via openings. If there is a failure occurred during

TABLE I

SUMMARY OF WAFER LEVEL HERMETIC ENCAPSULATION AS WELL AS THE YIELD ANALYSIS OF DIFFERENT MEMS SENSOR WAFERS USING DIFFERENT OUTGASSING AND GETTERING OPTIONS

Bond#	Outgas/Getter	Cavity Volume	Pressure Range	Yield
1	No/No	4.8 mm^3	3-5 Torr	87%
2	1 hour@300°C/No	4.8 mm^3	1-3 Torr	92%
3	10 hours@300°C/No	4.8 mm^3	0.15 Torr-1.5 Torr	82%
4	1 hour@300°C/Yes	4.8 mm^3	~1 mTorr	91%
5	No/Yes	4.8 mm^3	1-50 mTorr	92%
6	No/Yes	1.6 mm^3	1-50 mTorr	87%

the patterning of the via openings with KOH, it results in a micro-leak which prevents the hermetic sealing. The packaging yield can be increased by further optimizing the Au-Si eutectic bonding recipe. Although a very high bonding yield is obtained with this technology, it may be further increased by adjusting the bond temperature and force.

Table 1 presents the robustness of the wafer level encapsulation process as well as the yield analysis for different MEMS sensor wafers capped by using different outgassing and gettering options. The hermetic packaging is performed using an EVG wafer bonder having a bond chamber that is pumped down to pressure levels around 10 μTorr. Still, the pressures inside the cavities are measured to be as high as 5 Torr after the bonding, if neither an outgassing step nor thin-film getters are used. Outgassing is the desorption of the gas molecules from the devices encapsulated in vacuum cavities. It has a more significant effect on the micro-sealed cavities since they are not continuously pumped and have a high surface to volume ratio. A way of minimizing this effect is to do an additional heat treatment for the outgassing inside the bond chamber before the actual encapsulation process. In this work, different outgassing periods at a fixed temperature of 300°C are used before the encapsulation process. Although the outgassing step enhanced the vacuum levels, still the package pressures are measured to be limited to 150 mTorr or higher without using any thin-film getters. Best results achieved in Bond#4 of Table 1, for which both outgassing and gettering options are used and the package pressures are measured to be around 1 mTorr for 91% of the tested sensors on this particular 4" wafer. Pressures in the range of 1 to 50 mTorr are achieved by the use of thin-film getters with a yield of 95%, even without any outgassing step prior to the encapsulation process. It should be reminded that getters are thin-films or alloys that react with the trapped gases in order to improve the package pressure. The getter material is capable of pumping the outgassing material until its capacity is reached, irrespective of the cavity volume. Therefore, similar cavity pressures are obtained for sensors encapsulated with 100 μm (cavity volume: 1.6mm^3) and 300 μm (cavity volume: 4.8mm^3) deep cavities. The cavity pressures can be coarsely set to different levels ranging from 1 mTorr up to 5 Torr, simply by varying the outgassing period and utilization of the getter material, enabling the proposed method be used for various types of MEMS devices with different package pressure requirements.

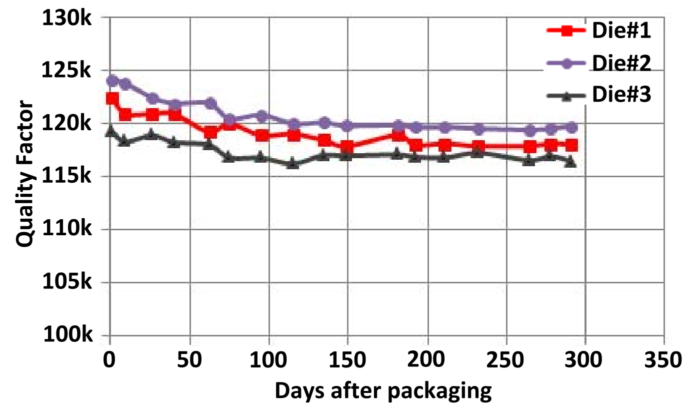


Fig. 10. Quality factor change over time for three different packaged chips. The pressure inside the cavities is observed to be lower than 10 mTorr for almost 10 months since the first prototypes has been fabricated.

Furthermore, there exist several vacuum levels in a packaged wafer. The reason may be due to the differences in the thin-film getter activation. Each die contains identical getter material with identical dimensions, but somehow it may show different activation characteristics which result in the different package pressure levels. Another reason may be the different outgassing characteristics of different dies. Although all dies are subjected to the same process steps and materials, their outgassing rates may be different. If the outgassing causes the release of non-getterable gases into the cavity, they cannot be absorbed by thin film getters and this results in different cavity pressures. As seen in the Table 1, the combination of outgassing and thin-film getters (Bond#4) provides a better pressure uniformity compared to the others. With this option, the effect undesired gases are prevented and more uniform package pressure can be obtained.

Fig. 10 presents the variation of the quality factors of resonators encapsulated in randomly selected three packages, and monitored within a period more than 10 months. The pressures inside all the three packages are observed to remain lower than 10 mTorr within this period. The lowest measured Q-factor in Figure 10 is above 115,000. Referring back to the data in Figure 8, this Q-factor value corresponds to a cavity pressure below 10 mTorr for all of the 3 dies monitored during the ten month period. The reduction of the Q-factors in Figure 10 corresponds to a change from an initial pressure around 1 mTorr to a stabilized pressure less than 10 mTorr within 150 days. This result shows that the proposed packaging method achieves a stable cavity pressure below 10 mTorr, which is sufficient for many applications.

C. Bonding Strength

The mechanical robustness of the packaged chips is evaluated by shear tests. Shear tests are performed for several packaged chips by using a conventional shear test tool. Fig. 11 presents the shear test results of 6 different packaged chips. The measured shear strengths of all chips are above 17 MPa with an average strength of 22 MPa, indicating a mechanically strong bond. Fig. 12 shows the photographs of cap and sensor chips separated from each other during

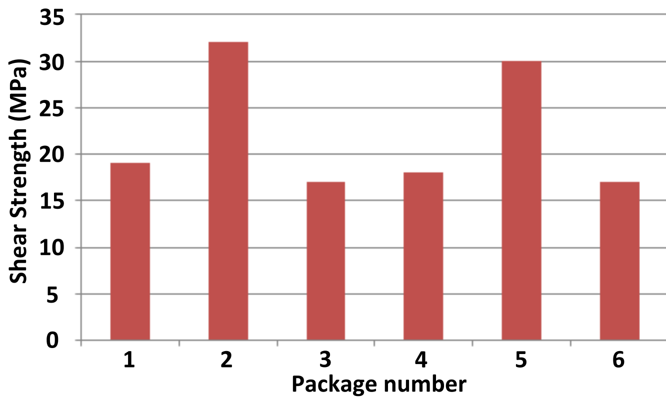


Fig. 11. Shear test results of 6 different packaged chips. The measured shear strengths of all chips are above 17 MPa with an average strength of 22 MPa, indicating a mechanically strong bonding.

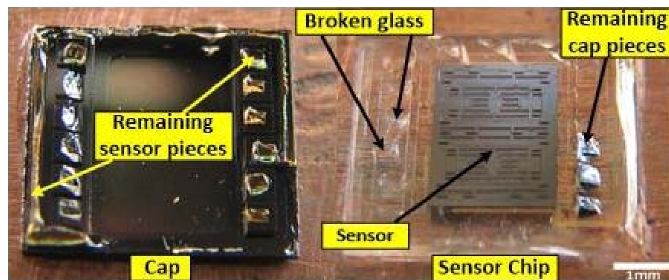


Fig. 12. Photographs of cap and sensor chips separated from each other during shear test. The Au-Si eutectic bonding interface is observed to withstand the shear test, as either the silicon cap or the glass substrate is broken, but not the bonding interface. This verifies that the Au-Si eutectic bonding strength is above 17 MPa.

the shear test. The strength of the Au-Si eutectic bonding interface is believed to be higher than the values in Figure 11, since the cap and sensor chips could not be separated from the bonding interface, but rather they are broken from other structural regions.

D. Thermal Robustness and Reliability

Thermo-mechanical robustness and reliability of the packaged chips are tested by thermal cycling, high temperature storage, and ultra-high temperature shock tests. At least two samples are subjected to each test in order to be sure from the accuracy of the results. Before each test, the resonators are tested similar to the initial vacuum characterization and their quality factors are extracted from the resonance characteristics. Then, packaged chips are subjected to the reliability tests. After the test, the quality factors of the resonators are again extracted by re-testing the resonators and compared with the initial values. The packaged chips are subjected to cyclic thermal shock tests between 100°C and 25°C for 5 cycles with 10 minute duration at each temperature and instant movements between hot and cold states. Fig. 13 presents the resonance characteristics of a packaged resonator die before and after the thermal cycling tests. The quality factor of the MEMS resonator was initially measured as 87,759 whereas it was 87,762 after the thermal cycling test. As the package

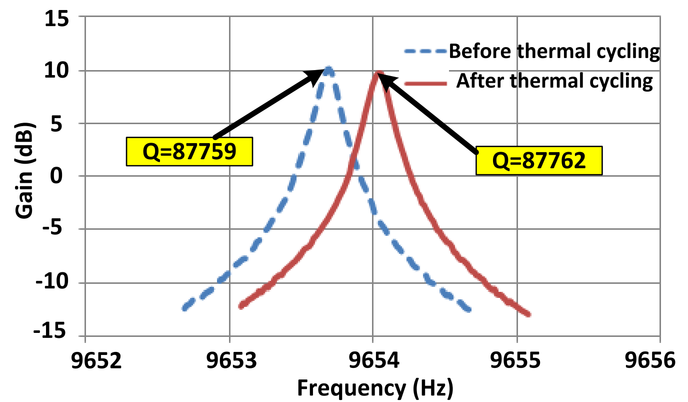


Fig. 13. Resonance characteristics of a packaged resonator before and after thermal cycling test in between 25°C and 100°C for 5 cycles with 10 minute duration for each cycle. No degradation is observed in the hermeticity of the packages at the end of this period.

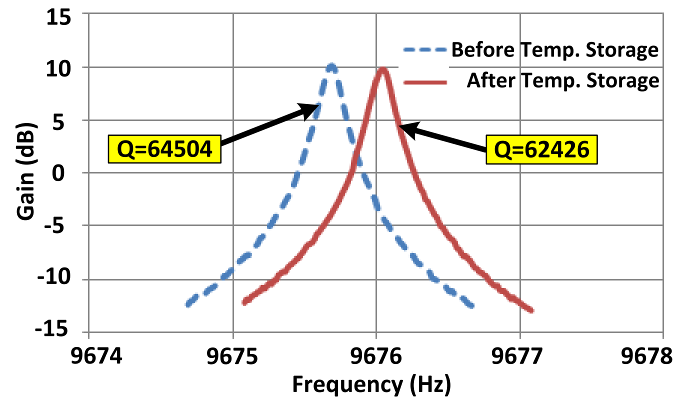


Fig. 14. Resonance characteristics of a packaged resonator die before and after high temperature storage test. Packaged chip is kept at 150°C for 24 hours for the high temperature storage test. The quality factor of a particular MEMS resonator was initially measured as 64,504 whereas it was 62,426 after the high temperature test, verifying that there is no change in the package vacuum and it is still below 25 mTorr.

pressure remains unchanged, it is verified that the hermeticity of the packages are preserved at the end of this test.

Next, high temperature storage tests are performed on the fabricated packages by keeping them at 150°C for a period of 24 hours. Fig. 14 shows the resonance characteristics of a packaged MEMS resonator die before and after the high temperature storage test. The quality factor of the resonator is measured to be reduced from 64,504 to 62,426 after the high temperature test. Such a reduction corresponds to a pressure change less than 1 mTorr at around 25 mTorr nominal package pressure. Finally, two of the packaged chips are subjected to a very high temperature shock test performed at 300°C for 5 minutes. The selected temperature value push the thermal robustness limit of the chips, and is still sufficiently far from the theoretical re-melting temperature (~363°C) of the Au-Si eutectic bonds. Fig. 15 presents the resonance characteristics of a sample resonator die before and after the high temperature shock test performed at 300°C for 5 minutes. Q values, and therefore, package pressures are measured to be almost unchanged before and after the test. This shows that a short

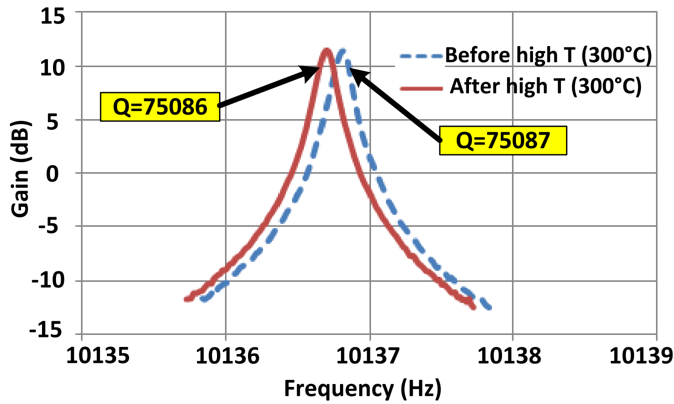


Fig. 15. Resonance characteristics of a packaged resonator die before and after the ultra-high temperature shock test performed at 300°C for 5 minutes. The hermeticity of the packaged chip withstands 300°C and mechanical failures such as crack initiation are not detected even after this test.

duration at high temperature does not degrade the hermeticity of the chips packaged with the *aMEMS* process.

IV. Conclusions

This study reports the extended results of an inherently simple, high-yield, reliable, mechanically and thermally robust wafer level hermetic encapsulation process, called as the advanced MEMS (*aMEMS*) process, developed at the METU-MEMS Research and Applications Center. The process employs vertical feedthroughs in order to eliminate step-coverage issues in conventional encapsulation methods, and yet does not require any complex via-fill and trench-refill process steps. The hermetic encapsulation is achieved by Au-Si eutectic bonding at 400°C, although it can be extended to other metal alloys. The fabricated prototypes are verified to be operational with cavity pressures as low as 1 mTorr with the use of thin-film getters. The cavity pressure can be coarsely tuned in the range from 1 mTorr up to 5 Torr by using proper combinations of outgassing steps and the getter material. The average packaging yield is around 90% for all different bonding trials at various process conditions. The package pressure is being monitored to remain stable below 10 mTorr for a period of 10 months until now. The mechanical strength of the packages has been checked with the conventional shear tests and measured to be as high as 30 MPa, indicating a mechanically-strong bonding. The robustness of the packages is also verified with thermal cycling, high temperature storage, and high temperature shock tests. No change has been observed in the package pressure after subjecting the packaged chips to thermal cycling tests between 100°C to 25°C for 5 cycles with 10 minute duration at each temperature step. The hermeticity of the packages is also verified to be preserved after storing the packages at 150°C for 24 hours, or applying a very high temperature shock as high as 300°C for 5 minutes. In conclusion, the proposed packaging method provides a new, simple, high-yield, reliable, and robust solution for the wafer-level hermetic packaging of various MEMS devices.

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Mustafa Mert Torunbalci was born in Ankara, Turkey, in 1985. He received the B.S. degree from the Department of Physics Engineering, Ankara University, Ankara, in 2008, and the M.Sc. and Ph.D. degrees from the Department of Micro and Nanotechnology, Middle East Technical University (METU), Ankara, in 2011 and 2015, respectively.

He has been a Research Assistant with the METU-Microelectromechanical Systems (MEMS) Research and Applications Center since 2008. His major research interests include the design, simulation, fabrication, and wafer level packaging of MEMS inertial sensors.

Said Emre Alper was born in Ankara, Turkey, in 1976. He received the B.S., M.Sc., and Ph.D. (Hons.) degrees in electrical and electronics engineering from Middle East Technical University (METU), Ankara, in 1998, 2000, and 2005, respectively. From 1998 to 2005, he was a Research Assistant with the Microelectromechanical Systems (MEMS)-VLSI Research Group, Department of Electrical and Electronics Engineering, METU, where he was a Senior Research Scientist and an Instructor until 2008. Since 2008, he has continued research with the METU-MEMS Research and Applications Center, where he has been the Deputy Director since 2009. He is the Technical Leader of the Inertial Sensors Research and Technology Development Group with the METU-MEMS Research and Applications Center.

His major research interests include capacitive MEMS inertial sensors, capacitive interface circuits, analog closed-loop control, various microfabrication technologies, packaging and testing of MEMS inertial sensors, and also hybrid system design.

Dr. Alper was a recipient of the METU Thesis of the Year Award by the Prof. Mustafa N. Parlar Education and Research Foundation for his M.Sc. thesis and Ph.D. dissertation, in 2000 and 2005, respectively. He is the first author of the symmetric and decoupled gyroscope design, which received the First Prize Award in the Operational Designs category of the International Design Contest by the Design, Automation, and Test Conference in Europe, and CMP in 2001. He is also the first author of the tactical-grade symmetrical and decoupled microgyroscope design, which received the Third Prize Award, among 132 MEMS designs from 24 countries and 25 states across the U.S., in the International 3-D MEMS Design Challenge by MEMGEN Corporation (currently Microfabrica, Inc.) in 2003.

Tayfun Akin was born in Van, Turkey, in 1966. He received the B.S. (Hons.) degree from Middle East Technical University (METU), Ankara, in 1987, and the M.Sc. and Ph.D. degrees from the University of Michigan, Ann Arbor, in 1989 and 1994, respectively, all in electrical engineering. He went to the USA in 1987 for his graduate studies with a graduate fellowship by the NATO Science Scholarship Program through the Scientific and Technical Research Council of Turkey. He raised and managed over $65M USD funding for several national and international projects, including EU FP6, FP7, NATOSfS, and NSF-USA projects. Since 1995, 1998, and 2004, he has been an Assistant Professor, an Associate Professor, and a Professor, respectively, with the Department of Electrical and Electronics Engineering, METU. He is currently the Director of the METU-Microelectromechanical Systems (MEMS) Research and Applications Center, which has a 1300-m2 clean room area for 4–8 in MEMS processing. His current research interests include MEMS, microsystems technologies, uncooled infrared detectors and readout circuits, inertial microsensors, silicon-based integrated sensors and transducers, and analog and digital integrated circuit design. He was a recipient of the First Prize in Experienced Analog/Digital Mixed-Signal Design Category at the 1994 Student VLSI Circuit Design Contest organized and sponsored by Mentor Graphics, Texas Instruments, Hewlett-Packard, Sun Microsystems, and *Electronic Design Magazine*. He co-authored the Symmetric and Decoupled Gyroscope Project, which received the First Prize Award in the Operational Designs category of the International Design Contest by the DATE Conference and CMP in 2001. He co-authored the Gyroscope project, which received the Third Prize Award of the 3-D MEMS Design Challenge by MEMGen Corporation (currently, Microfabrica). He has served in various MEMS, EUROSENSORS, and TRANSDUCERS conferences as a Technical Program Committee Member. He was the Co-Chair of the 19th IEEE International Conference on Micro Electro Mechanical Systems (MEMS 2006) in Istanbul. He was the Co-Chair of the Steering Committee of the IEEE MEMS Conference in 2007. He is the Steering Committee Member of the 18th International Conference on Solid-State Sensors, Actuators, and Microsystems (Transducers 2015).