Low-Complexity Constrained Coding Schemes for Two-Dimensional Magnetic Recording

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Presentation Outline

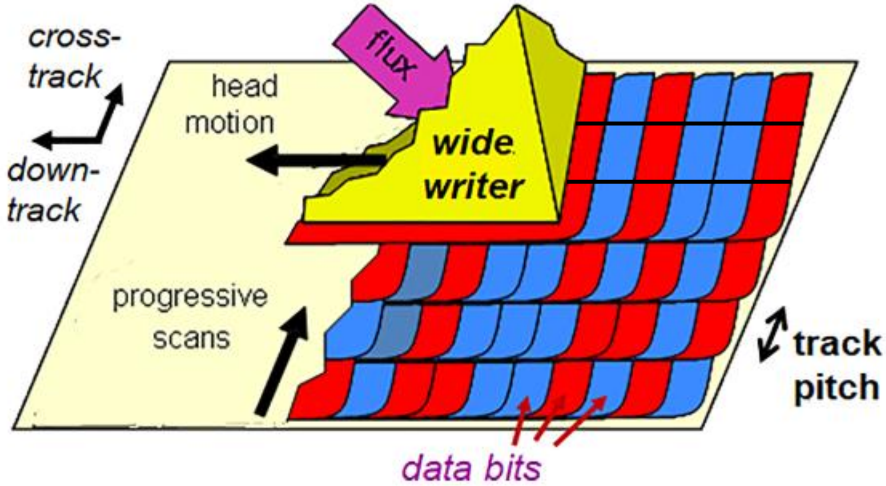
- Motivation and technical vision
- SP-LOCO coding scheme
- ST-LOCO coding scheme
- Transition probability analysis
- Experimental results
- Conclusion and future directions

Two-Dimensional Magnetic Recording (TDMR)

- **Tracks are squeezed and horizontal grain isolation is removed.**

- **Wide read heads, which read multiple tracks at the same time, can be adopted.**
  - Accesses 3 adjacent down tracks at the same time.
  - Allows one-dimensional (non-binary) coding.
  - Middle track suffers from interference the most compared with the lower and upper tracks.

[R1]



- **TDMR channel effects:**
  - Inter-symbol interference and inter-track interference (ISI and ITI).
  - TD jitter (timing) problems as well as electronic noise.

Advantages and Error Prone Patterns of TDMR

- **TDMR offers a remarkable storage density increase without the need for new magnetic materials.**
  - Up to 10 Terabits per square inch.
    - Track squeezing.
    - Shingled (Overlapped) writing.
    - Two-dimensional data processing.

- **In TDMR, data patterns involving a bit surrounded by complementary bits, i.e., isolated, horizontally and vertically are error-prone.**
  - 3×3 discretized TD channel impulse response.

·	0	·
0	1	0
·	0	·

History and Our Proposed Codes

FSTD of Constrained Codes, 1948, Shannon [R2]

↓

RLL Codes, Tang and Bahl [R3] Enumerative Source Coding, Cover [R4], 1970s

↓

State splitting and merging to produce FSMs, Adler, Coppersmith, and Hassner 1983 [R5]

↓

Optimization of FSMs, 1990s [R6, R7]

↓

Constrained Codes Based on Lexicographic Indexing, 2000s [R8, R9]

↓

LOCO Codes, 2020 [R10, R11, R12]

History and Our Proposed Codes

- **Constrained codes prevent error-prone patterns to mitigate interference.**
- **Lexicographically-ordered constrained codes (LOCO) codes achieve minimal redundancy and reconfigurability.**
- **Simple LOCO codes take the advantage of separation of uncoded streams.**
  - Low complexity.
  - Low latency.
  - Low error propagation.

1	0	0	1	1	1	0	1	1	…
1	0	0	1	1	0	0	1	0	…
0	1	0	0	1	0	1	1	0	…

Introduction to Constrained Codes

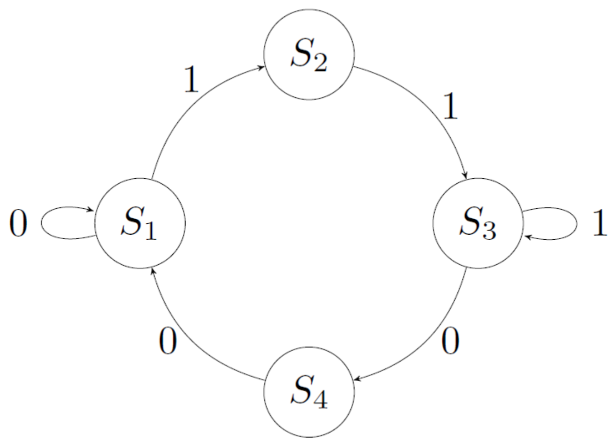
- **Constrained codes impose restrictions on written (transmitted) data.**
  - The set of forbidden patterns can be symmetric or asymmetric.
  - The rate is (# of information bits)/(# of coded bits or symbols).

- **The universe of constrained sequences is represented by an FSTD. The capacity is the highest achievable rate.**

- **Example:** $\mathcal{S}_1 = \{010, 101\}$ constraint.
  - The adjacency matrix of this FSTD is:

$$\mathbf{F} = \begin{bmatrix} 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 0 \end{bmatrix}$$

  - The capacity is $\log_2\left(\lambda_{\max}(\mathbf{F})\right)$, which is 0.6942 here.



Lexicographically-Ordered Constrained Codes

- Maps integers (codeword indices) to codewords and vice versa: Encoding-decoding rule.
- The set of forbidden patterns are connected directly to the cardinality and the rule of the LOCO code.

- Simple mathematical relation represents the encoding-decoding rule:
  - Less complex compared with look-up tables.
  - Allows reconfigurability.
- Capacity-achieving.
- At moderate lengths, LOCO codes provide a rate gain of up to 10% compared with practical RLL codes that are used to achieve the same goals.
- LOCO codes are immune to error propagation from one codeword into another.

Motivation of Low Complexity Codes

- **Optimal LOCO codes use GF(8).**
  - Offer minimal redundancy.
  - We want to reduce codeword to message error propagation and reduce complexity due to large alphabet size.
- **Simple LOCO codes with alphabet size smaller than GF(8)**
  - Uncoded tracks.
  - Data streams to be processed separately.

- **Advantages:**
  - Lower complexity.
  - Lower error propagation.
  - Complete track separation (SP-LOCO).
  - Data-stream separation (ST-LOCO).
  - Lower processing latency.
  - Better error performance.

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Forbidden Patterns of SP-LOCO / OP-LOCO

- **Plus isolation (PIS) patterns**

·	0	·
0	1	0
·	0	·

·	1	·
1	0	1
·	1	·

SP-LOCO Coding Scheme

- **For each group of 3 down tracks:**
  - Apply a GF(2) constrained code on the middle track such that all PIS patterns are eliminated.
  - Leave the data on the upper and lower tracks uncoded.

- **Forbid $\{010, 101\}$ on the middle track.**

- **S-LOCO on the middle track.**

Uncoded	1	0	0	1	1	1	0	1	1	…
S-LOCO	1	0	0	1	1	0	0	1	1	…
Uncoded	0	1	0	0	1	0	1	1	0	…

SP-LOCO Bridging, Self-Clocking, and Rate

- **Same idea that is used to bridge S-LOCO codewords:**
  - Repeat the rightmost bit of each codeword at instance t then the leftmost bit of each codeword at $t+1$.

- **Level-based signaling: Remove $\mathbf{0}^m$ and $\mathbf{1}^m$.**

- $R_{\mathrm{SP-LOCO}}^{\mathrm{n}} = \frac{1}{3}\left[\frac{\lfloor \log_2(N_2(m)-2)\rfloor}{m+2} + 2\right]$ where

$N_2(m) = N_2(m-1) + N_2(m-2),\ m \geq 2,$ which is the cardinality of S-LOCO.

Complexity Reduced!

- Comparison of normalized rate and adder size for OP-LOCO and SP-LOCO.
- For a LOCO code, the size of adders that execute the rule governs the encoding-decoding complexity.
- SP-LOCO offers remarkable complexity reduction via smaller adder sizes but incurs rate loss because it forbids more than needed.
- $C^{\mathrm{n}}_{\mathrm{SP-LOCO}} = \frac{0.6942+2}{3} = 0.8981.$ $C^{\mathrm{n}}_{\mathrm{OP-LOCO}} = 0.9710.$

m	$R^{\mathrm{n}}_{\mathrm{OP-LOCO}}$	Adder size, OP	$R^{\mathrm{n}}_{\mathrm{SP-LOCO}}$	Adder size, SP
13	0.9048	38 bits	0.8667	10 bits
23	0.9306	67 bits	0.8800	17 bits
39	0.9417	113 bits	0.8862	28 bits
53	0.9506	154 bits	0.8909	38 bits
89	0.9593	259 bits	0.8938	63 bits

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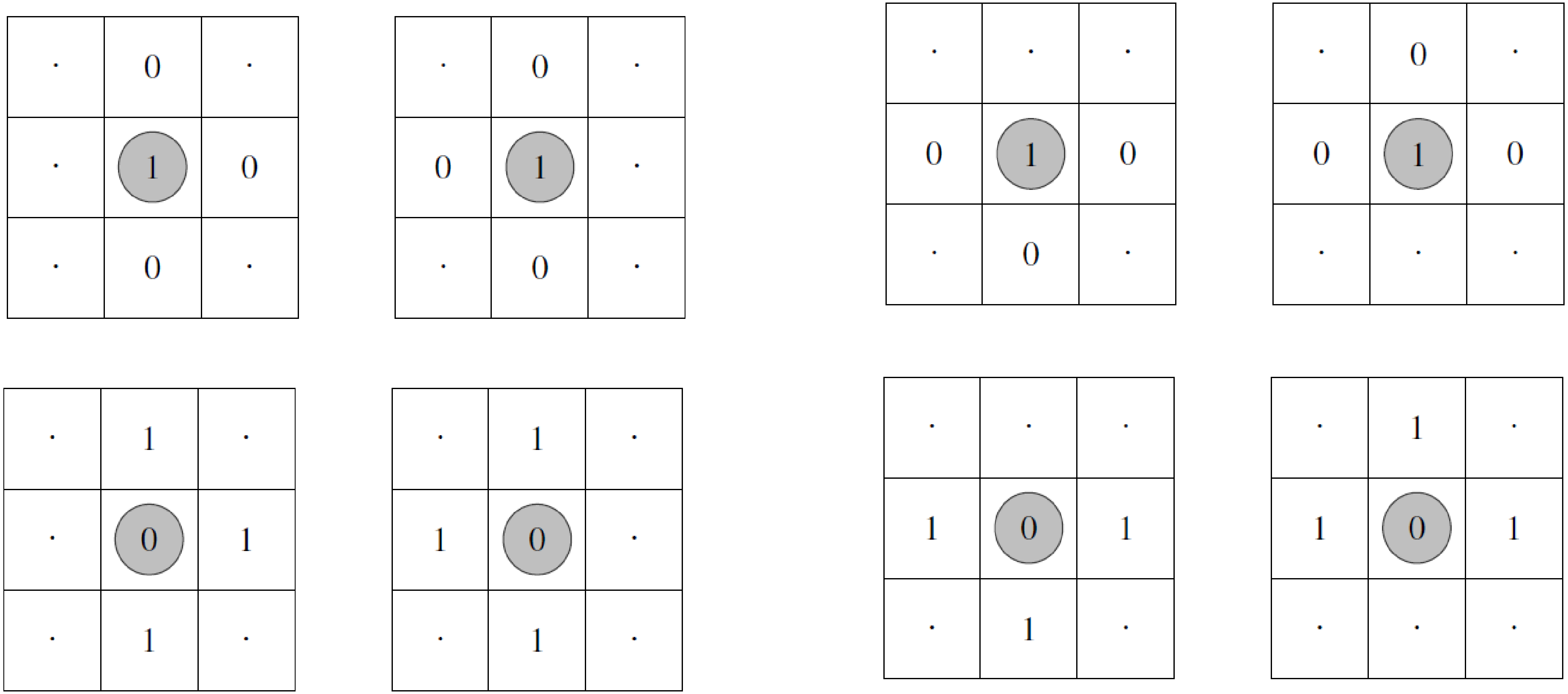
Forbidden Patterns of ST-LOCO / OT-LOCO

- **Rotated T isolation (RTIS) patterns**



ST-LOCO Coding Scheme

- Alphabet is defined over GF(4)

$$0 \leftrightarrow [0\ 0\ 0]^{\mathrm{T}} \text{ or } [0\ 0\ 1]^{\mathrm{T}} \qquad 1 \leftrightarrow [0\ 1\ 0]^{\mathrm{T}} \text{ or } [1\ 1\ 0]^{\mathrm{T}}$$
$$\alpha \leftrightarrow [1\ 0\ 1]^{\mathrm{T}} \text{ or } [1\ 0\ 0]^{\mathrm{T}} \qquad \alpha^2 \leftrightarrow [1\ 1\ 1]^{\mathrm{T}} \text{ or } [0\ 1\ 1]^{\mathrm{T}}$$

- Even though this mapping does not offer explicit track separation, there is one uncoded stream that is used to decide between the 3-tuple columns.

- Reason for this mapping: Decreasing the transition rates on the TD grid so that the performance is improved.

- To eliminate RTIS patterns, forbid $\{01, 10, 1\alpha, \alpha 1, \alpha\alpha^2, \alpha^2\alpha, 0\alpha^2 0, \alpha^2 0\alpha^2\}$.

ST-LOCO Bridging, Self-Clocking, and Rate

- **Bridging:**
  - 3-symbol bridging.
  - For every possible scenario, there are at least 4 bridging patterns out of which, we will use only 4. Thus, we encode 2 additional input message bits within bridging symbols to increase the finite-length rate.

- **Intrinsically self-clocked.**

- $R^{\mathrm{n}}_{\mathrm{ST-LOCO}} = \frac{1}{3}\left[\frac{\lfloor \log_4(N_4(m)) \rfloor + 2}{m+3} + 1\right]$ where

$$N_4(m) = 2N_4(m-1) + N_4(m-2), \quad m \geq 2.$$

ST-LOCO Rule and Example

- $g(\mathbf{c}) = \sum_{i=0}^{m-1} \left[\left(\frac{1}{2} \theta_{i,1} + \theta_{i,2} \right) N_4(i) + \frac{1}{2} \theta_{i,3} N_4(i-1) \right].$

- **Example:** Consider the ST-LOCO code $\mathcal{STC}_5^4$.
  - $N_4(5) = 140.$
  - $\mathbf{c} = \alpha^2\alpha^2\alpha^2\alpha^2\alpha^2$ (Last codeword according to the lexicographic order)
    $\rightarrow g(\mathbf{c} = \alpha^2\alpha^2\alpha^2\alpha^2\alpha^2) = N_4(5) - 1 = 139.$
  - We verify this via the encoding-decoding rule:
    - For c_4, $y_{4,3} = 1$. Thus, $\theta_{4,1} = \theta_{4,2} = \theta_{4,3} = 1$.
    - For $c_i, i \in \{0,1,2,3\}, y_{i,5} = 1$. Thus, $\theta_{i,1} = \theta_{i,3} = 0$ and $\theta_{i,2} = 1$, for all $i \in \{0,1,2,3\}$.

$$g(\mathbf{c} = \alpha^2\alpha^2\alpha^2\alpha^2\alpha^2) = \left[\frac{3}{2} N_4(4) + \frac{1}{2} N_4(3) \right] + N_4(3) + N_4(2) + N_4(1)$$

$$+N_4(0) = 139.$$

Complexity Reduced!

- Comparison of normalized rate and adder size for OT-LOCO and ST-LOCO.
- ST-LOCO offers remarkable complexity reduction via smaller adder sizes but incurs rate loss because it forbids more than needed.
- $C^{\mathrm{n}}_{\mathrm{ST-LOCO}} = \frac{1.2715+1}{3} = 0.7572.$ $C^{\mathrm{n}}_{\mathrm{OT-LOCO}} = 0.8498.$

m	$R^{\mathrm{n}}_{\mathrm{OT-LOCO}}$	Adder size, OT	$R^{\mathrm{n}}_{\mathrm{ST-LOCO}}$	Adder size, ST
9	0.7879	23 bits	0.7222	12 bits
12	0.8095	31 bits	0.7333	16 bits
23	0.8267	59 bits	0.7436	30 bits
34	0.8333	87 bits	0.7477	44 bits
49	0.8366	125 bits	0.7500	63 bits

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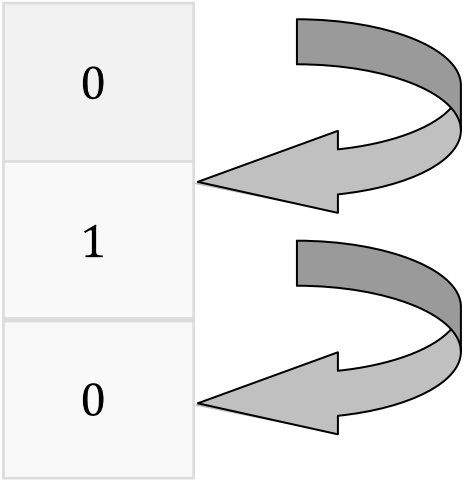
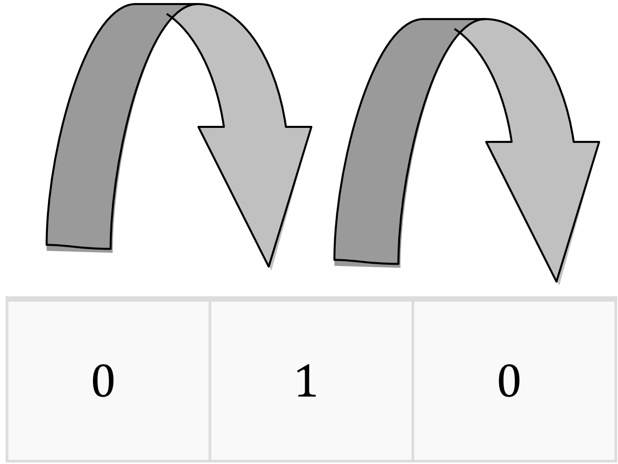
Motivation for Probability Analysis

- Investigation of transition rates on the TDMR grid will provide insights into the error performance.
- Offer insights about the capability of eliminating TD error-prone patterns after encoding using the relevant coding scheme.
- Vertical transition probability and horizontal transition probability were investigated.





Probability Calculations

- $P(T_\mathrm{h}) = \sum_i P(T_\mathrm{h}, d_i) = \sum_i \sum_j P(T_\mathrm{h}, d_i, S_j)$

$$= \sum_i \sum_j P(T_\mathrm{h} | d_i, S_j) P(d_i | S_j) P(S_j)$$

  where S_j denotes the previous state and d_i denotes previous symbol on the LOCO code state diagram (FSTD). T_h denotes the event of horizontal transition.

- $P(T_\mathrm{v}) = \sum_i P(T_\mathrm{v}, d_i) = \sum_i P(T_\mathrm{v} | d_i) P(d_i)$

  T_v denotes the event of vertical transition.

- $P(d_i)$ can be calculated as follows:

  $P(d_i) = \sum_j P(d_i, S_j) = \sum_j P(d_i | S_j) P(S_j)$.

OP, SP, OT, Then ST!

	OP-LOCO	SP-LOCO	OT-LOCO	ST-LOCO
Theoretical transition rates				
Horiz. all tracks	0.4819	0.4255	0.4325	0.3780
Vert. all tracks	0.4710	0.5000	0.4000	0.4268
Avg. all tracks	0.4765	0.4628	0.4163	0.4024
Horiz. middle track	0.4380	0.2764	0.2764	0.1464
Experimental transition rates (using length-23 coding)				
Horiz. all tracks	0.4871	0.4231	0.4419	0.3810
Vert. all tracks	0.4576	0.5000	0.3989	0.4283
Avg. all tracks	0.4724	0.4616	0.4204	0.4047
Horiz. middle track	0.4450	0.2693	0.2695	0.1458

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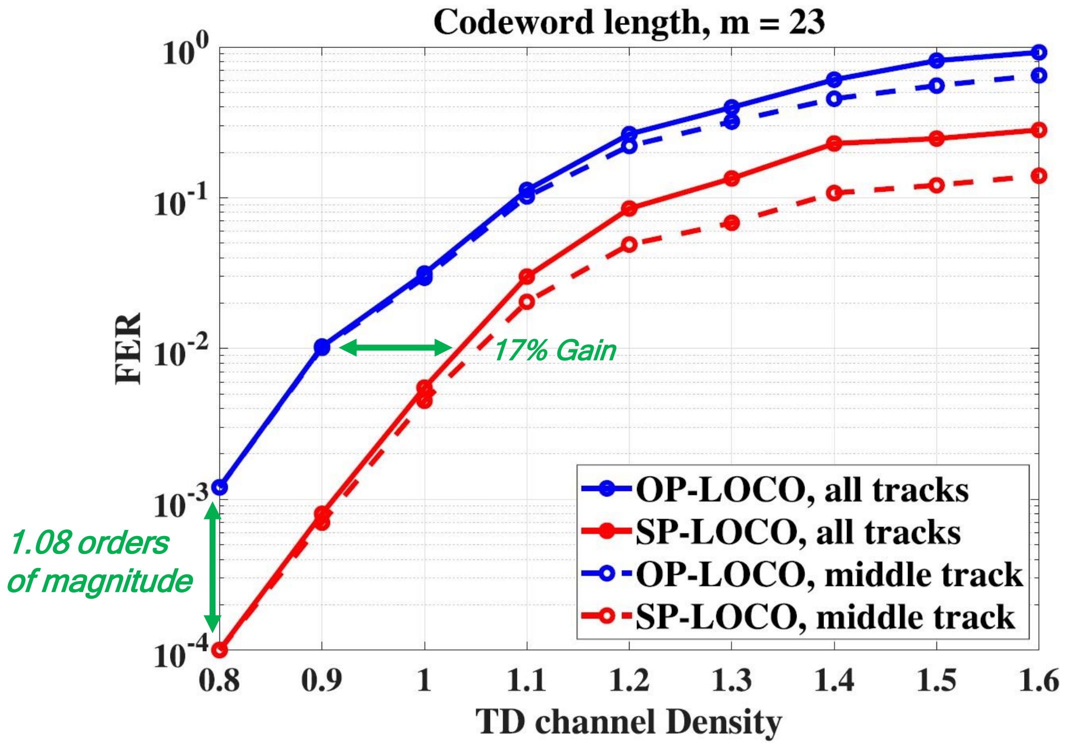
Remarkable Performance Gains via Track Separation

- At FER $\cong 1.0 \times 10^{-2}$, the SP-LOCO coding scheme achieves a TD density gain of about 17% for the middle track.

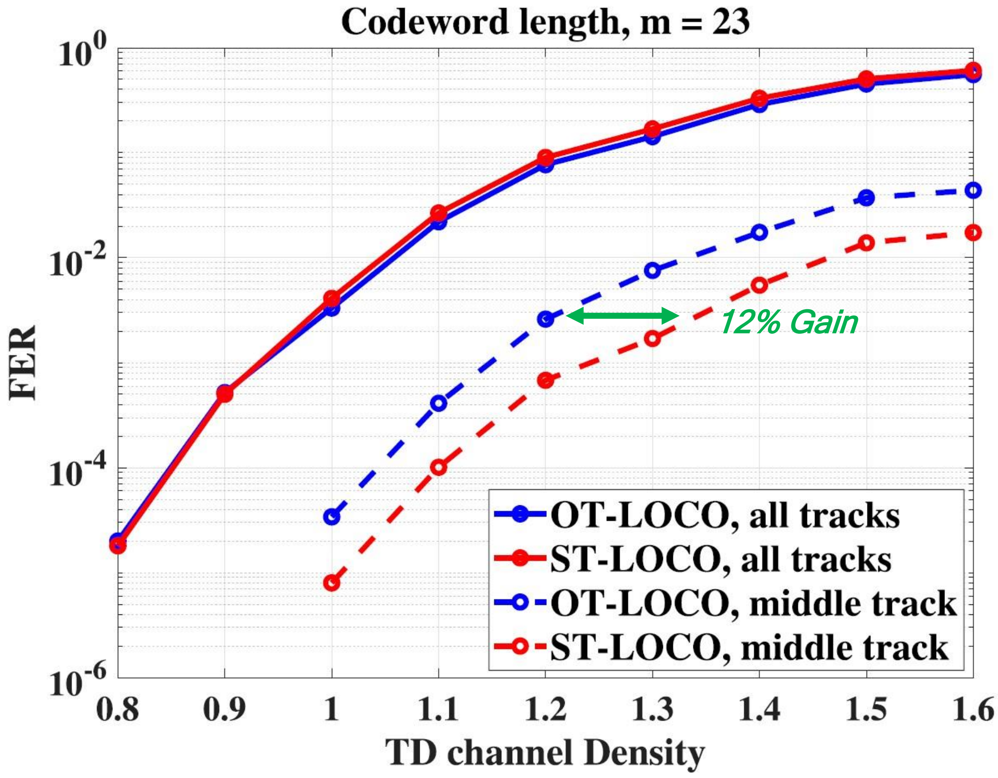
- At $D_{TD} = 0.8$, the SP-LOCO coding scheme achieves an FER performance gain of about 1.08 orders of magnitude for all tracks.



Remarkable Performance Gains via Track Separation

- At FER $\cong 2.7 \times 10^{-3}$, the ST-LOCO coding scheme achieves a TD density gain of about 12% for the middle track.

- At $D_{TD} = 1.2$, the ST-LOCO coding scheme achieves an FER performance gain of about 0.60 orders of magnitude for all tracks.



Reconfiguration

- **One proposal for reconfiguration is as follows:**
  - OP-LOCO can be used early in the lifetime of the device to prevent PIS patterns.
  - At the intermediate stage of the device lifetime, the coding scheme can be reconfigured to SP-LOCO to provide better performance.
  - The coding scheme can be reconfigured to OT-LOCO or to ST-LOCO when RTIS patterns become more dominant.

  - According to the application needs, the OT-LOCO or the ST-LOCO code can be used; the former offers higher rates for almost the same error performance, while the latter offers low complexity and low error propagation.

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Conclusion and Future Directions

- **Conclusions:**
  - Storage densities are rapidly growing with TDMR devices. Data require high protection.
  - Optimal LOCO codes offer remarkable error performance but suffer from codeword-to-message error propagation and complexity issues due to high alphabet size.
  - Simple LOCO codes use smaller field sizes to prevent the same error patterns with low complexity and error propagation (also with better error performance).

- **Future directions:**
  - Using machine learning to reconfigure the LOCO codes.
  - Combining our LOCO codes with multi-dimensional LDPC codes.

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Thank You!