EE 282
Homework #4

Due:April 20, 2011

Q1. For the RTL gate shown in Fig 3.1,

i. Find I_{B1}, I_{B2}, I_{RC}, and V_{OUT} for all combinations of V_{IN1} and V_{IN2} equal to 0 and 5 V. (Use $\beta_F = 20$, $V_{BE(FA)} = 0.7$ V, $V_{BE(SAT)} = 0.8$ V, and $V_{CE(SAT)} = 0.2$ V.)

ii. Determine the logic function implemented.

iii. Determine the fan-out, assuming V_{OUT} is connected to V'_{IN1} inputs of the following stages whose second inputs are connected to V_{CC}, i.e., $V'_{IN2}=V_{CC}$.

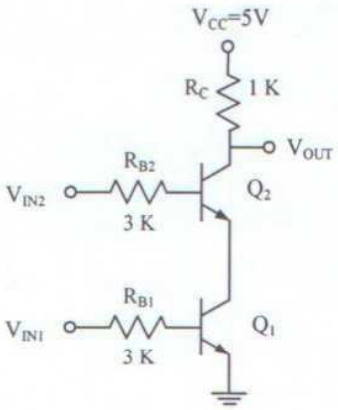

Fig. 3.1

Q2. Consider the implemented in the DTL circuit given in Fig. 3.2.

i. Determine the logic function.

ii. Determine and plot the voltage transfer characteristics (VTC) V_{OUT} vs V_{IN} with $V_{IN1} = V_{IN2} = V_{IN}$. Let $V_{D(ON)} = 0.7$ V for the diodes and $\beta_F = 100$. $V_{BE(FA)} = 0.7$ V, $V_{BE(SAT)} = 0.8$ V and $V_{CE(SAT)} = 0.2$ V for the BJT.

iii. Determine also the high and low noise margins.

iv. Determine the fan-out, assuming V_{OUT} is connected to V'_{INA} inputs of the following stages whose second inputs are connected to ground, i.e., $V'_{INB}=0$ V.

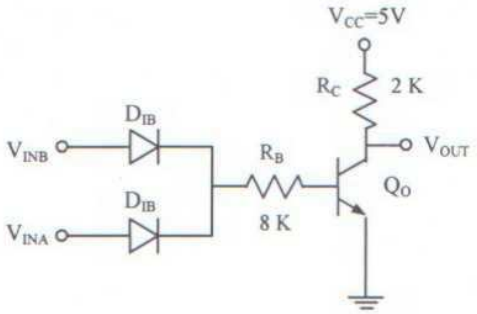

Fig. 3.2