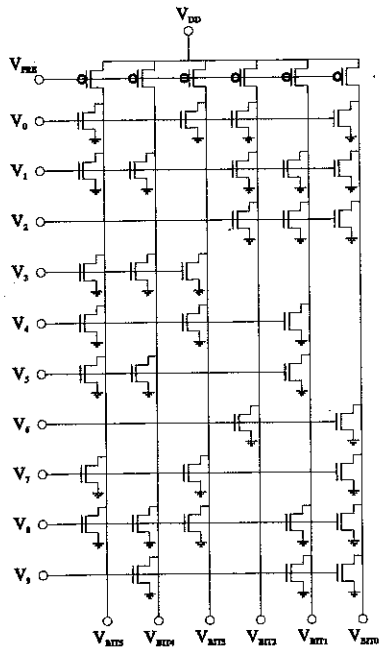

FIGURE P32.45

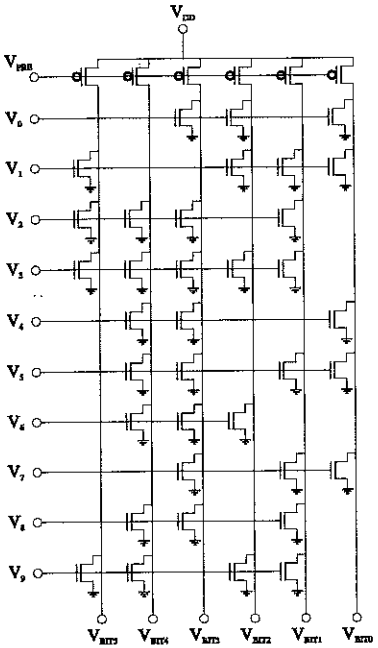

FIGURE P32.47

33 SEMICONDUCTOR STATIC RANDOM-ACCESS MEMORIES

All memories can be categorized into one of two types as follows:

1. **Read-only memories** (ROMs) in which data is stored permanently upon fabrication, and
2. **Read-write memories** (RWM) where data can both be read from and written to after fabrication.

In the previous chapter, the design of ROMs for diode, BJT, and MOSFET technologies is discussed. In this chapter, read-write memories are presented.

Read-write memories can be divided into two categories as follows:

1. **Sequential** in which data is read-from in the same sequence in which it was stored (magnetic tape is an example of a sequential read-write memory), and
2. **Random-access** memory (RAM) in which data can be read in a sequence independent of the order in which it was originally written

Random-access memory can be written-to and read-from much faster than sequential memory and therefore is used most often for the active memory or "work space," of modern computers. Sequential memory is most often used for large storage of data such as required in backup routines.

Semiconductor RAMs fabricated with transistors can be further subdivided into the following categories:

1. *Static* **RAMs** (SRAM) which can maintain storage of data as long as power to the semiconductor circuit employing it remains uninterrupted, and
2. *Dynamic* **RAM** (DRAM) which can possess greater packing densities but require incorporation of active *refreshing circuitry* to maintain storage of data over a period of several milliseconds

In this chapter the concepts and designs of semiconductor *SRAMs* are described. Because of the numerous types of refresh circuitry used with DRAMs, this type of memory is omitted for brevity. SRAMs built with MOSFETs and BJTs are discussed along with implantation of massive arrays of data bits used in modern computers. This chapter begins with a discussion of the MOSFET SRAM followed by an introduction to some additional administrative circuitry required to write-to and read-from each SRAM bit. SRAMs employing higher speed BJTs are similar in design and are presented following the presentation of MOSFET static RAMs.

33.1 STATIC RAM CELL WITH TRANSMISSION GATES

Figure 33.1a displays the configuration of a single-bit MOSFET static RAM cell. At any time, this single bit can store either a logic 0 or a logic 1. The block diagram symbol used for this cell is shown in Figure 33.1b. The use of this symbol considerably simplifies the discussion of multi-bit SRAM configurations.

Cross Coupled Inverter Latch

The basic embodiment for storing each bit of information in semiconductor SRAMs is the cross coupled inverter latch, presented in Chapter 31 (see Figures 31.4 and 31.5 and the accompanying discussion in

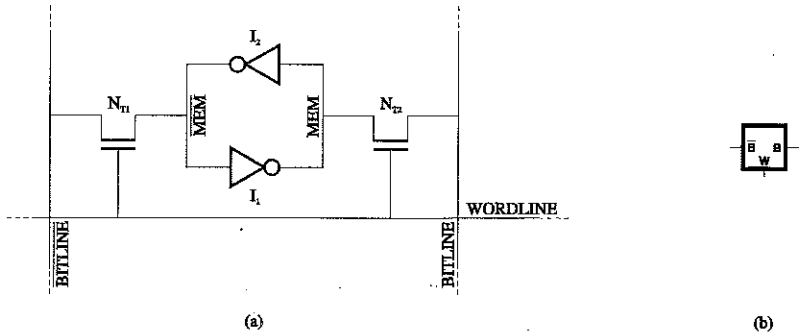

FIGURE 33.1 Basic Static RAM Cell with Transmission Gates: **(a)** Cross coupled inverter latch with complementary NMOS transmission gates, **(b)** Circuit symbol used in multi-bit static RAM cell

section 31.2). The inverters are labeled I_1 and I_2 in Figure 33.1a. The cross coupled inverters are used for both MOSFET SRAMs as well as BJT SRAMs, as will be seen later in this chapter.

The two NMOS transistors of Figure 33.1a act as transmission gates for reading-from and writing-to-this single bit SRAM cell. When the line labeled **WORDLINE** is brought high, both NMOS transistors are on, connecting **BITLINE** and $\overline{\text{BITLINE}}$ to the cross-coupled inverters. When **WORDLINE** is low, the two NMOS transmission gates are cutoff and the RAM bit stores a stable binary logic level 0 or 1.

The two ports labeled **BITLINE** and $\overline{\text{BITLINE}}$ are used to carry the data for writing-into and reading-from the bit. The mechanisms for writing and reading to this bit cell are presented after storage in each bit is explained.

Storage of Single-Bit Data

The cross coupled inverter latch of Figure 33.1a is used to understand the storage of logic **0**s and **1**s. Clearly, the two nodes of the cross coupled inverters hold complementary logic levels. Also, the two inverters I_1 and I_2 form a positive feedback loop and since I_1 and I_2 simultaneously drive the inversion of the two nodes labeled MEM and $\overline{\text{MEM}}$ (with their respected logic complements), this storage should be stable. The arbitrary labeling of the MEM and $\overline{\text{MEM}}$ refer to the inverse states of this memory cell.

Storage of a Logic 1

Consider the SRAM bit of Figure 33.1a with the **WORDLINE** port grounded so the two transmission NMOS devices are cutoff. This situation is displayed in Figure 33.2a. If the node common to the output of I_1 and input of I_2 is at logic 1, the node common to the output of I_2 and input of I_1 should be at logic **0**. The node labeled **MEM** is driven high by the inverter I_1, which has a low input. In turn, the $\overline{\text{MEM}}$ node is driven low by inverter I_2, which has a high input. This state represents a stored logic 1 with MEM = 1.

Storage of a Logic 0

The storage of logic **0** is the inverse of the storage of logic 1. If the node labeled MEM is at a logic level **0**, the node labeled $\overline{\text{MEM}}$ is driven high by the inverter I_2. The inverter I_1 with a high input in turn drives the MEM node low, reinforcing storage of a logic 0. This state is indicated in Figure 33.2b.

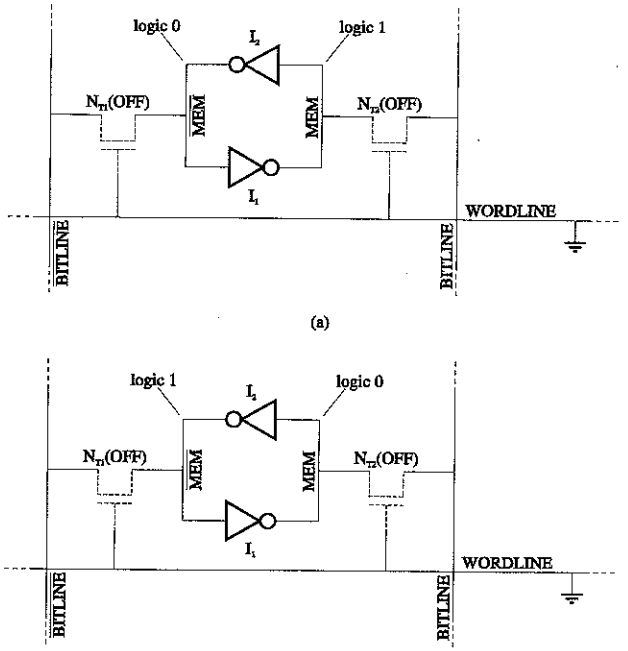

FIGURE 33.2 Logic States Stored in the Cross-coupled Latch of a RAM Cell Bit: **WORDLINE** low cuts off both transmission NMOS transistors, **(a)** Stored logic 1, **(b)** Stored logic 0

Writing to a Single-Bit

The single-bit MOSFET RAM cell of Figure 33.1a is written-to by holding the **WORDLINE** node high and **BITLINE** and $\overline{\text{BITLINE}}$ at complementary logic levels. This enables the NMOS transmission gates to pass logic levels from the **BITLINE** and $\overline{\text{BITLINE}}$ nodes to the cross-coupled inverter latch.

Writing a Logic 1

Consider Figure 33.3a with **WORDLINE** high, while **BITLINE** and $\overline{\text{BITLINE}}$ are simultaneously held high and low, respectively. Under these conditions, a logic 1 is written into the SRAM bit cell. The voltage levels of **BITLINE** and $\overline{\text{BITLINE}}$ are therefore transmitted though N_{T1} and N_{T2} to the MEM and $\overline{\text{MEM}}$ nodes. Regardless of the logic level stored in the SRAM bit before **WORDLINE** is high, the cross-coupled inverter latch switches to the values on **BITLINE** and $\overline{\text{BITLINE}}$ in a few nanoseconds.

Writing a Logic 0

If **BITLINE** and $\overline{\text{BITLINE}}$ are held low and high, respectively, while **WORDLINE** is high, a logic **0** is

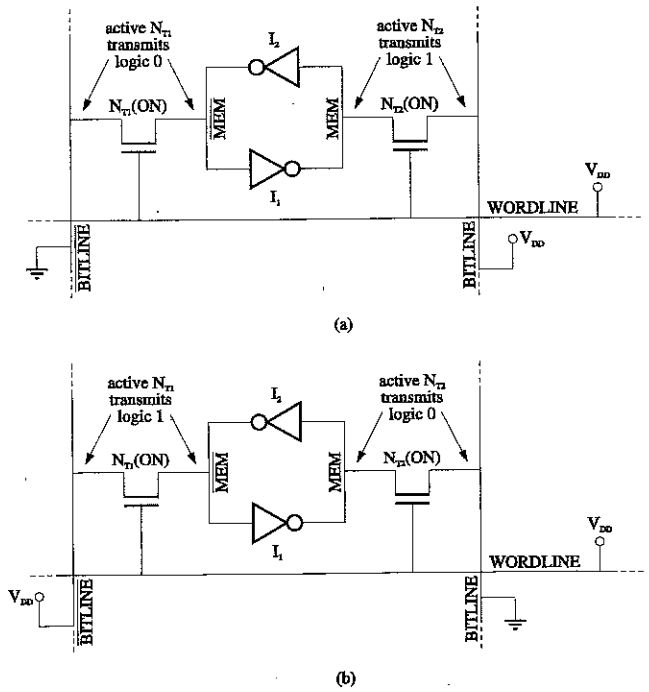

FIGURE 33.3 Writing to a RAM Cell: (a) WORDLINE brought high with BITLINE driven high writes a logic 1 into RAM bit, (b) WORDLINE brought high with BITLINE driven low writes a logic 0 into RAM bit

written into the cross-coupled inverter latch of the SRAM bit cell as illustrated in Figure 33.3b in a fashion similar to that explained for writing a logic 1.

Waveforms of Writing Logic 1s and 0s

Figure 33.4 shows the voltage waveforms describing the writing of logic 1s and 0s into a static RAM bit cell. At the beginning of the time period depicted in the section labeled (a), the RAM cell stores an initial logic value of binary 0. This is observed by noting that MEM is low and $\overline{\text{MEM}}$ is high.

In Figure 33.4b, WORDLINE is brought high, while BITLINE and $\overline{\text{BITLINE}}$ are high and low, respectively. This writes a logic high into the cross-coupled latch of the SRAM. Note that the non-zero rise and fall times of the MEM and $\overline{\text{MEM}}$ nodes are indicated.

In Figure 33.4c, WORDLINE is brought low and the SRAM cell stores the logic high value written during (b).

In Figure 33.4d, WORDLINE is brought high while BITLINE and $\overline{\text{BITLINE}}$ are low and high, respectively. This writes a logic 0 into the SRAM cell.

When WORDLINE is brought low again as in Figure 33.4e, the SRAM cell stores the logic low value written to it during part (d).

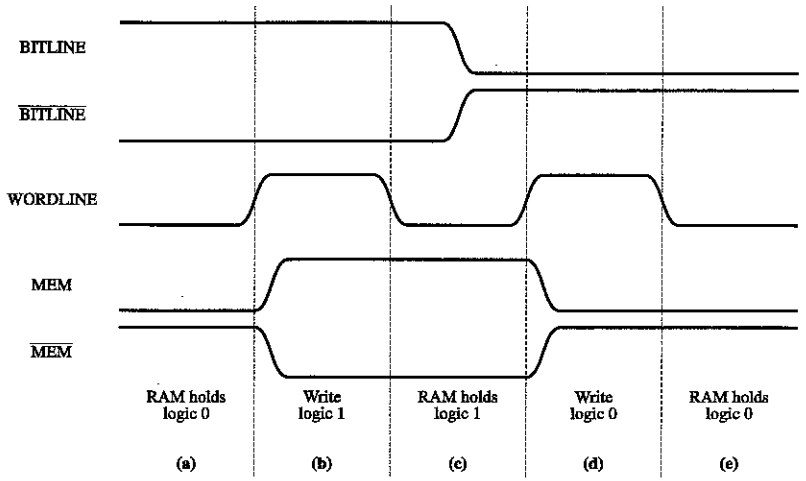

FIGURE 33.4 WRITE Into RAM Bit Cell: (a) RAM initially holds a zero, (b) WORDLINE brought active with BITLINE driven high—WRITEs logic 1 into RAM bit, (c) RAM holds logic 1 after WORDLINE brought inactive, (d) WORDLINE brought high and BITLINE driven low—WRITEs logic 0 into RAM bit, (e) RAM holds logic 0 after WORDLINE brought low

Reading from a Single-bit

Reading binary values from the MOSFET SRAM cell introduced in this section is accomplished by bringing WORDLINE high and allowing BITLINE and $\overline{\text{BITLINE}}$ to be driven by the enabled NMOS transmission gates. Since MEM and $\overline{\text{MEM}}$ are always at complementary logic levels BITLINE and $\overline{\text{BITLINE}}$ will be driven with complementary logic levels.

33.2 MOSFET STATIC RAM CELL TECHNOLOGIES

The storage, writing, and reading of binary logic levels using the MOSFET SRAM cells presented in the previous section are discussed without regard to the particular logic family making up the cross-coupled inverters. Three types of SRAM technologies are presented in this section. The choice of which to use depends upon the fabrication facilities available and/or the amount of memory required.

Enhancement-Depletion Loaded NMOS SRAM Cells

Figure 33.5 displays the single bit RAM cell of the previous section embodying the enhancement-depletion loaded NMOS inverters presented in Chapter 21.

CMOS SRAM Cells

Most modern ROM cells employ CMOS inverters discussed in Chapter 23. A CMOS single bit RAM

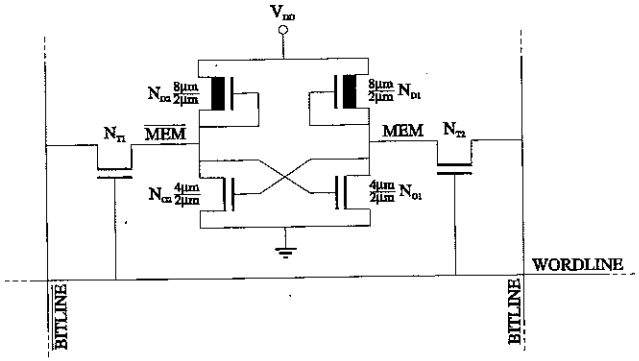

FIGURE 33.5 Enhancement-depletion Loaded NMOS Static RAM Cell

cell is shown in Figure 33.6. CMOS RAM cells provide the advantage of low power dissipation with roughly the same circuit density of the enhancement-depletion loaded NMOS RAM cell of the previous sub-section.

Resistor Loaded NMOS SRAM Cells

Figure 33.7 shows a single-bit RAM cell constructed with resistor loaded NMOS inverters. This technology utilizes specifically fabricated high value resistors.

33.3 BJT Static RAM Cell Technologies

Figures 33.8 and 33.9 display two BJT static RAM cells. These are both cross coupled BJT inverter latches similar to the MOSFET SRAM cells of the previous section.

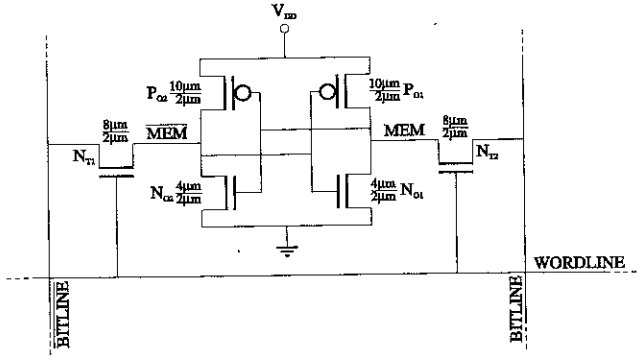

FIGURE 33.6 CMOS Static RAM Cell

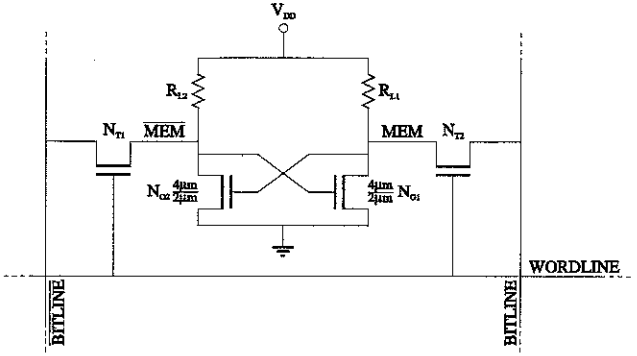

FIGURE 33.7 Resistor Loaded NMOS Static RAM Cell

Double Emitter BJT SRAM Cell

BJT SRAM cells of the type shown in Figure 33.8 connect to common bit columns through the emitters of dual emitter NPNs. Access to this type of SRAM is brought about by bringing the WORDLINE high and thus reading the base voltage of each BJT base. The MEM and $\overline{\text{MEM}}$ nodes are then one V_{BE}(FA) voltage below these base voltages.

Schottky Diode BJT Static RAM Cell

Operation of the Schottky diode BJT SRAM cell of Figure 33.9 is essentially the same as the dual emitter BJT SRAM cell. The Schottky diode BJT SRAM cell is also accessed by bringing the WORDLINE high. MEM and $\overline{\text{MEM}}$ nodes are then one Schottky diode forward voltage above the resistor midpoints on both sides of the SRAM.

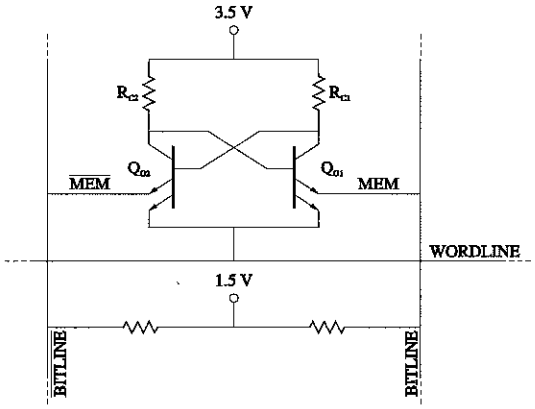

FIGURE 33.8 BJT Static RAM Cell with Dual-emitter BJTs