A Near State PWM Method With Reduced Switching Frequency And Reduced Common Mode Voltage For Three-Phase Voltage Source Inverters

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***Abstract* - The Near State PWM (NSPWM) method, which reduces the common mode voltage/current, is proposed for three-phase PWM inverter drives. The optimal voltage vectors and their sequences are determined. The voltage linearity and DC bus and AC output PWM current ripple characteristics are studied. The method is thoroughly investigated and its performance is compared to conventional methods. Theory, simulations, and experiments show that NSPWM exhibits superior common mode and satisfactory PWM ripple performance characteristics.**

Keywords - Inverter, PWM, VSI, common mode voltage, common mode current, ASD, EMI, voltage reflection, space vector, DPWM.

I. INTRODUCTION

Three-phase Voltage Source Inverters (VSI) are widely utilized to drive AC motors with high motion control quality and energy efficiency, provide clean current waveform and regenerative operation in AC-DC power converter applications, and supply high quality power in uninterruptible power supply AC-DC-AC power converter units. Pulse Width Modulation (PWM) is the standard approach to operate the inverter switches in order to generate the required output voltages. Conventional Continuous PWM (CPWM) methods such as Space Vector PWM (SVPWM) and Discontinuous PWM (DPWM) methods such as DPWM1 [1], perform satisfactorily in terms of voltage linearity, output current ripple, DC bus current ripple, average switching frequency requirements. However, they have poor Common Mode Voltage (CMV) and Common Mode Current (CMC) characteristics. The recently developed Reduced CMV PWM (RCMV-PWM) methods such as AZSPWM1 [2], RSPWM [3], AZSPWM2 [4] have marginal performance improvement and all have performance constraints prohibiting their practical utilization. This paper proposes a new CMV/CMC reduction PWM method, the Near State PWM (NSPWM) method that exhibits superior overall performance characteristics in the high modulation range. The paper describes the method, studies its performance characteristics, and via comparative evaluation exhibits its superior overall performance. Simulations and experimental results verify the performance of the method.

The CMV is defined as the potential of the star point of the load with respect to the center of the DC bus of the VSI (V_{no} in Fig.1.) and can be expressed in the following.

$$v_{no} = (v_{ao} + v_{bo} + v_{co})/3 \quad (1)$$

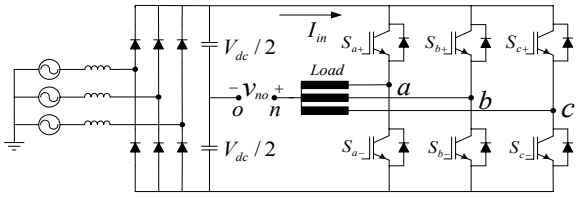


Fig. 1. A three-phase inverter drive with diode rectifier front-end.

Since the VSI can not provide sinusoidal voltages and has discrete output voltages, the CMV is different from zero and may take the values of $\pm V_{dc}/6$ or $\pm V_{dc}/2$ depending on the switch states. At higher switching frequencies and DC bus voltage levels, excessive CMVs can result in high CMCs. This may lead to bearing failure or noise that causes nuisance trip of the inverter drive. In the application field, recently such problems have been increasing due to increasing PWM frequencies (aimed for higher efficiency, control bandwidth, smaller filter size etc.) [5] and CMV reduction techniques have been gaining importance. The effect of the CMV can be actively or passively [6] reduced. The active CMV reduction method that involves controlling the PWM pulse patterns is the most economical method as it requires no extra components and cost. However, reducing the CMV via PWM pulse pattern typically degrades the other modular performance characteristics. The RCMV methods reported to date all have significant disadvantages that prohibit their application. Detailed performance evaluation of most methods is reported in [4]. This work reports the NSPWM method that has superior performance compared to other RCMV methods.

II. THE NSPWM METHOD

The Near State PWM (NSPWM) method utilizes a group of three neighbor voltage vectors to match the output and reference volt-seconds. These three voltage vectors are selected such that the voltage vector closest to reference voltage vector and its two neighbors (to the right and left) are utilized. Therefore, the utilized voltage vectors are changed in every 60^o throughout the space. As shown in Fig. 2, to apply the method, the voltage vector space is divided into six segments. Defined with indices, voltage vectors V_{i-1}, V_i, and V_{i+1} are utilized for region Bi. For example, for the region between 30^o and 90^o (B2), the applied voltage vectors are V_1, V_2, and V_3 (Fig. 3).

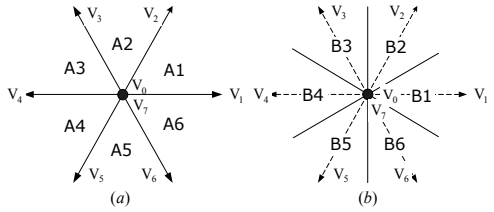


Fig. 2. Voltage space vectors and 60° sector definitions.

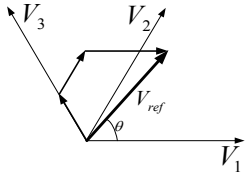


Fig. 3. Illustration of the NSPWM space vectors for B2.

Utilizing the above defined near state voltage vectors, the complex variable volt-seconds balance equation and the PWM period constraint for NSPWM are given in generalized form for region Bi (2.a, 2.b) where T_s is the PWM period.

$$V_{i-1}t_{i-1} + V_i t_i + V_{i+1}t_{i+1} = V_{ref}T_s \quad (2.a)$$

$$t_{i-1} + t_i + t_{i+1} = T_s \quad (2.b)$$

Normalizing the voltage vector on-time values, the vector duty cycles can be found as $d_k = t_k / T_s$, where k: *i-1, i, i+1*. Utilizing the above equations, the duty cycles of the required voltage vectors can be calculated for region Bi as follows.

$$d_{i-1} = 1 - \frac{2\sqrt{3}}{\pi} M_i \sin(\theta - \frac{(i-2)\pi}{3}) \quad (3)$$

$$d_i = -1 + \frac{3}{\pi} M_i \cos(\theta - \frac{(i-2)\pi}{3}) + \frac{3\sqrt{3}}{\pi} M_i \sin(\theta - \frac{(i-2)\pi}{3}) \quad (4)$$

$$d_{i+1} = 1 - \frac{3}{\pi} M_i \cos(\theta - \frac{(i-2)\pi}{3}) - \frac{\sqrt{3}}{\pi} M_i \sin(\theta - \frac{(i-2)\pi}{3}) \quad (5)$$

In the above equations $\theta = w_e t$ is the angle of the reference voltage vector and M_i is the modulation index which indicates the voltage utilization level ($M_i = V_m/(2V_{dc}/\pi)$) [1]. Equations (3), (4), and (5) yield a valid solution only in region LR shown in Fig. 4. and in the remaining regions there is no solution. Region LR, where (3), (4), and (5) have a valid solution, corresponds to per fundamental cycle voltage linearity between $M_{iL\min} = \pi/(3\sqrt{3}) \cong 0.61$ and $M_{iL\max} = \pi/(2\sqrt{3}) \cong 0.907$. For the shaded region of Fig. 4, where NSPWM has a valid solution, the three voltage vectors may be combined in various sequences to program the required output voltage.

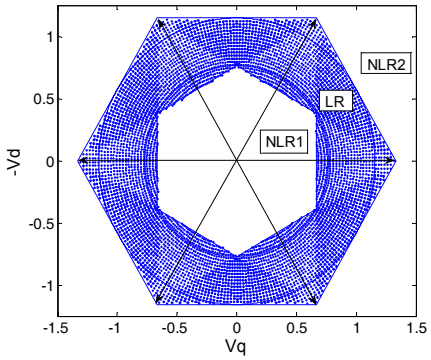


Fig. 4. Voltage linearity range of NSPWM (voltages normalized to $V_{dc}/2$).

With the constraints of minimum switching count, no simultaneous switchings of phase legs, and minimum CMV, only the sequence of V_{i+1}-V_i-V_{i-1}-V_i-V_{i+1} as a general form for region Bi remains feasible. For example, between 30° and 90° (B2), the optimal sequence is V_3-V_2-V_1-V_2-V_3. In this sequence state changes occur only between adjacent states and this is the only sequence which does not require simultaneous switching of the inverter legs. The sequence of NSPWM and other methods are shown in Table I for region definitions of Fig.2.

TABLE I.
VOLTAGE VECTOR PATTERNS OF VARIOUS PWM METHODS

	A1	A2	A3	A4	A5	A6
CPWM	7210127	7230327	7430347	7450547	7650567	7610167
AZSPWM1	3216123	4321234	5432345	6543456	1654561	2165612
	B1	B2	B3	B4	B5	B6
NSPWM	21612	32123	43234	54345	65456	16561

III. SCALAR IMPLEMENTATION

The modulation signals of DPWM1 [1] and NSPWM are exactly the same. However, in NSPWM instead of one carrier wave, two carrier waves (V_{tri} and $-V_{tri}$) must be utilized. The choice of the triangle to be compared with the modulation signals is region dependent and is given in Table II. The general switching rule is that if the reference signal is larger than the carrier signal, the upper switch associated with the specific phase is set "on". For example, as shown in Fig. 5, in B2, the modulation signals of phases "*b*" and "*c*" are compared with V_{tri} while the modulation signal of phase "*a*" is compared with $-V_{tri}$ and the pulse pattern of NSPWM in B2 results. The scalar implementation of NSPWM is possible with DSPs that have two individual comparator registers per phase (TI TMS320F2808 with 6 pairs of CompA/CompB registers).

TABLE II.
NSPWM REGION DEPENDENT CARRIER SIGNALS

	B1	B2	B3	B4	B5	B6
Phase a	V_{tri}	$-V_{tri}$	$-V_{tri}$	V_{tri}	V_{tri}	V_{tri}
Phase b	V_{tri}	V_{tri}	V_{tri}	$-V_{tri}$	$-V_{tri}$	V_{tri}
Phase c	$-V_{tri}$	V_{tri}	V_{tri}	V_{tri}	V_{tri}	$-V_{tri}$

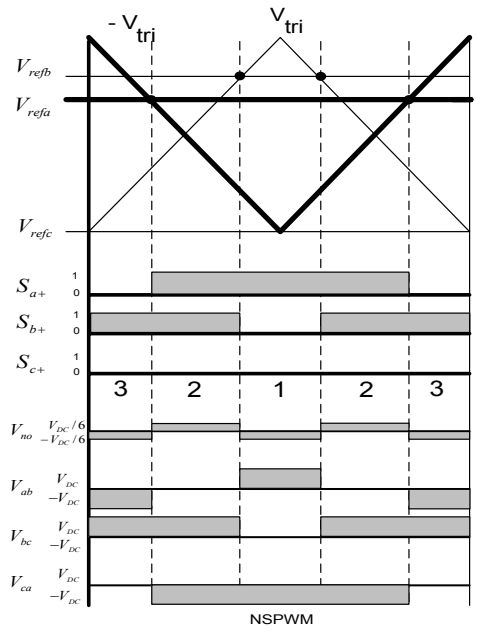


Fig. 5. Scalar implementation of NSPWM (region B2).

IV. THE PWM RIPPLE PERFORMANCE OF NSPWM

The PWM ripple performance of NSPWM is investigated both on the inverter output and DC link side. For the AC output current ripple, the standard measure of Harmonic Distortion Factor (HDF) is utilized and for the DC link current ripple, the standard measure of the DC link current ripple factor (K_{dc}) is utilized in order to evaluate the performance of NSPWM [1]. The study is investigated in comparison with the classical PWM methods. When evaluating HDF and K_{dc}, all PWM methods are considered with equal average switching frequency and the carrier frequency of each method is adjusted accordingly. The HDF characteristics of all methods but NSPWM are given in [4] and that of NSPWM is numerically evaluated. The K_{dc} characteristics of all methods but NSPWM are given in [4]. That of NSPWM is calculated as follows.

$$K_{dc}^{NSPWM} = 1 + (M_i \frac{24}{\pi^2} - \frac{3\sqrt{3}}{2\pi}) \cos 2\varphi - M_i^2 \frac{18}{\pi^2} \cos^2 \varphi \quad (6)$$

HDF(M_i) characteristics of all methods are shown in Fig. 6. Within its linearity range, NSPWM has the least harmonic distortion among all RCMV methods. In the lower range of its voltage linearity range, NSPWM has higher harmonic content than the conventional PWM methods. However, the difference is about 50%. In the higher linear modulation range, NSPWM performs better than CPWM methods and comparably with DPWM methods. In Fig. 7, $K_{dc}=f(M_i)$ of various methods including NSPWM are shown with the load Power Factor (PF) as parameter. The DC link harmonic content of NSPWM is strongly dependent on PF and M_i. Its behavior is similar to AZSPWM1, such that the performance improves with increasing M_i and PF. For PF=1, NSPWM has lower DC link harmonic content than all other PWM methods. For PF of 0.8-0.9, K_{dc} of all PWM methods are similar. However, at PF lower than 0.6, K_{dc} of NSPWM is inferior to all other PWM methods.

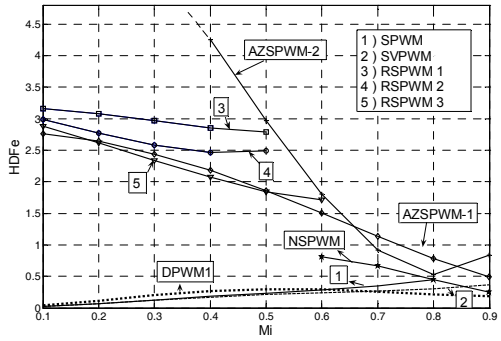


Fig. 6. $HDF_e=f(M_i)$ for various PWM methods.

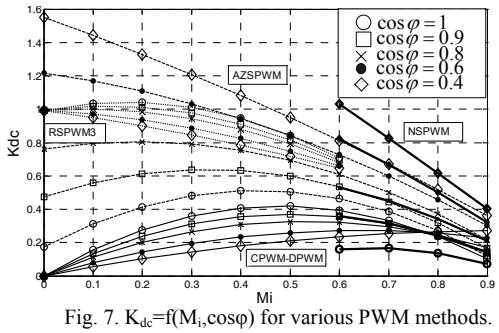


Fig. 7. $K_{dc}=f(M_i,\cos\varphi)$ for various PWM methods.

V. CMV/CMC AND LINE-TO-LINE VOLTAGE PULSE PATTERNS

There are fundamental differences between the pulse patterns of the conventional methods and NSPWM. Specifically, the CMV and line-to-line voltage patterns influence the inverter performance significantly in terms of switching transients and high frequency behavior. The inverter leg upper switch logic, CMV, and line-to-line voltage patterns for NSPWM, SVPWM, DPWM1, and AZSPWM1 are shown in Fig. 8. SVPWM and DPWM1 have high CMVs (limits: $\pm V_{dc}/2$). NSPWM and AZSPWM1 reduce the CMV (limits: $\pm V_{dc}/6$). This is the main advantage of RCMV-PWM methods. Although CMV of RCMV-PWM methods is less than those of the conventional methods, the rate of change of CMV is the same for all methods. During a switching transition CMV always changes by $|\Delta V|=V_{dc}/3$. Thus the capacitive CMC during the switching transition is similar. Therefore, during switching transient CMC is high and comparable in all PWM methods, while between switching instants the CMC of RCMV-PWM methods is significantly lower than other methods.

The CMV pattern alone is not sufficient to determine the feasibility of a PWM method. AZSPWM1 and other RCMV-PWM methods have problematic line-to-line output voltage pulse patterns prohibiting their practical use. As Fig. 8 shows, the inverter output line-to-line voltage patterns of CPWM/DPWM methods are unipolar such that the polarity of the line-to-line voltage does not change within a PWM cycle (there is pulse-polarity-consistency). Both AZSPWM1 and NSPWM have bipolar patterns that generate undesirable effects such as high PWM ripple current and overvoltage transients. As illustrated in the previous section, the PWM ripple current of NSPWM is tolerably small in the high M_i range.

In motor drive applications involving long cables, two consecutive voltage pulses with opposite polarity must be separated by a sufficient time interval to damp the switching induced overvoltage due to voltage reflection [7]. Methods with bipolar pulse pattern are not favorable unless the pulses are safely distant from each other. In NSPWM, the zero-voltage time interval between the two bipolar pulses is always greater than the AZSPWM1 case and sufficiently large for most of the NSPWM voltage linearity range. Thus, NSPWM differs in performance compared to other RCMV-PWM methods. For NSPWM, within each 60^o segment, only one line-to-line voltage has bipolar voltage pulses and the duration of that zero-voltage time interval $t_{z\text{-}nspwm}$ can be calculated. For example, for region B2 it is given as in (7). For AZSPWM1 for each 60^o segment two line-to-line voltages have bipolar pattern. Therefore, two different zero-voltage time intervals $t_{z\text{-}azspwmx}$ and $t_{z\text{-}azspwmy}$ are defined. For example, for region A1, they are given as in (8) and (9), respectively. Normalizing the zero-voltage time intervals with the carrier cycle, the duty cycles of the zero-voltage time invervals can be found.

$$t_{z-nspwm} = \left[-1/2 + (3/\pi) \cdot M_i \cos(60-\theta)\right] T_s \quad (7)$$

$$t_{z-azspwmx} = \left[(\sqrt{3}/\pi) \cdot M_i \sin(60-\theta)\right] T_S \quad (8)$$

$$t_{z-azspwmy} = \left[(\sqrt{3}/\pi) \cdot M_i \sin\theta\right] T_S \quad (9)$$

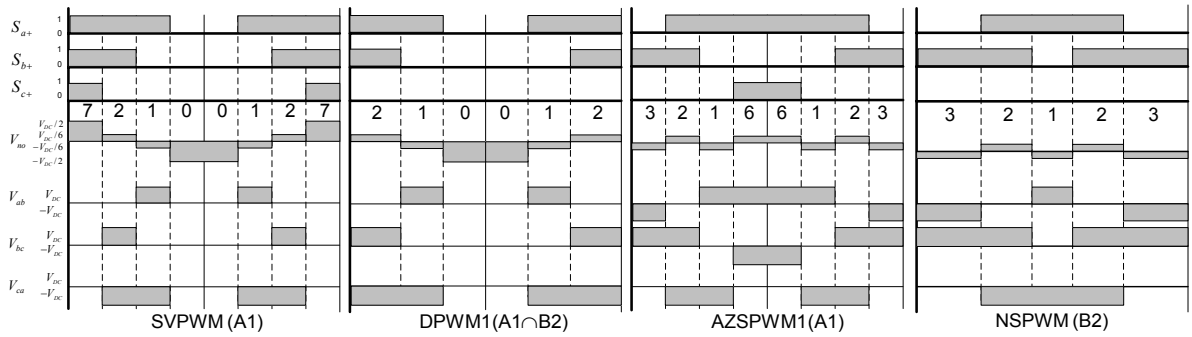


Fig. 8. PWM pulse pattern of SVPWM, DPWM1, AZSPWM1, and NSPWM methods.

In Fig. 9, the zero-voltage time interval duty cycle (d_z) variation with respect to θ over a half fundamental cycle (d_z is periodic at π) for the line-to-line inverter output voltage V_{ab} is illustrated for both NSPWM and AZSPWM1. Both unipolar (light) and bipolar (bold) voltage sections are considered. As the figure illustrates, for NSPWM the bipolar line-to-line voltage has zero-voltage time intervals for a total of 2x60°, while for AZSPWM1 the total is 2x120°. Also the figure indicates that the unipolar line-to-line voltage pulses of NSPWM are more distant from each other than those of AZSPWM1. The narrowest zero-voltage time intervals of bipolar pulses are most problematic in the application as they cause the largest overvoltage stresses. The narrowest d_z can be calculated from (7), (8), and (9) and are shown in Fig. 10 with respect to M_i. For AZSPWM1 $d_{zmin}=0$ regardless M_i. For NSPWM the relation is linear with M_i. For example, for M_i=0.65 the duty cycle is 3%, corresponding to a sufficiently long time interval for the voltage pulses to settle. Thus, overvoltages are avoided. Given a minimum d_z constraint, the applicable M_i range of NSPWM can be found from the figure.

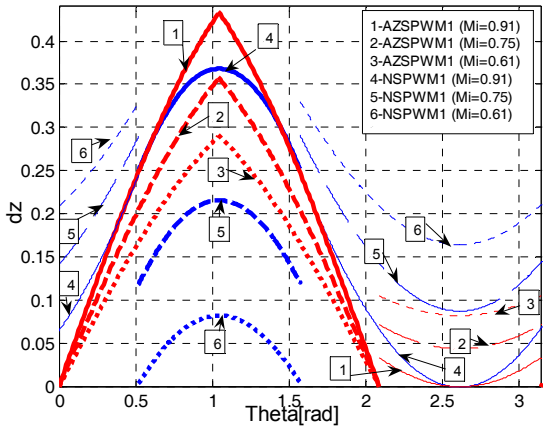


Fig. 9. Variation of zero-voltage time interval duty cycle of the line-to-line voltages with respect to M_i and θ (Blue: NSPWM, Red: AZSPWM1).

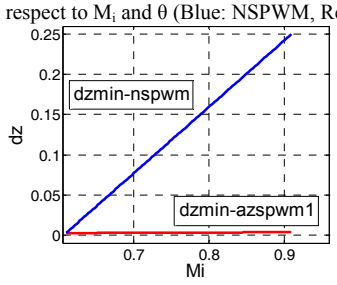


Fig. 10. Minimum zero-voltage time duty cycle of NSPWM and AZSPWM1.

VI. Computer Simulations

To verify the analytical results, a 4-kW, 380-V, 4-pole, 1440-min^{-1} induction motor driven by an inverter has been simulated. The drive is at no-load, and constant V/f algorithm is employed (176.7 V_{rms}/50 Hz). The DC bus voltage is fixed at 500 V. The PWM ripple performance of NSPWM is investigated and compared to various PWM methods. The carrier frequency is 6.66 kHz for SVPWM and AZSPWM1. For NSPWM and DPWM1 10 kHz is utilized ($f_{s\text{-}ave}$=6.66 kHz). All methods are simulated for various M_i values and the motor phase current waveforms at M_i=0.9 (201.4 V_{rms}/57.3 Hz) that correspond to the upper voltage linearity boundary of NSPWM are shown in Fig. 11. At M_i=0.9, where the maximum linearity point is approached, DPWM1 and NSPWM are comparable and superior to the other methods in terms of current ripple.

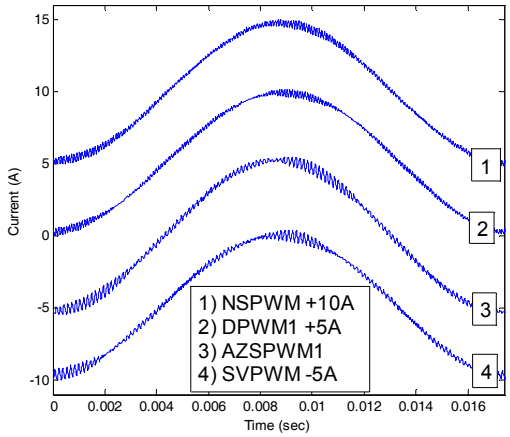


Fig. 11. Output current waveforms various PWM methods and M_i = 0.9.

VII. Experimental Results

In order to evaluate the CMV/CMC and PWM ripple performance of various PWM methods an experimental set-up is established and an induction motor drive is operated at various speed (M_i) levels. The motor ratings are the same as in the simulations. To measure the CMV/CMC values properly, the experimental set-up shown in Fig. 12 is established where the motor is placed on an insulation base plate and a Y-Y transformer is utilized to feed the rectifier and thus the drive. With the neutral point of the transformer secondary isolated from the primary, but connected to the chasis of the motor

through a cable, the cable current becomes the common mode current i_{cm} (the leakage current). The CMC is then correctly measured via a high bandwidth current transducer (LeCroy CP150, 150 A, 10 MHz). Also the CMV which is the motor neutral point to the DC bus midpoint voltage is measured with a high bandwidth differential voltage probe (LeCroy ADP305, 1000 V, 25 MHz). The inverter is operated in the constant V/f mode (176.7 Vrms 50 Hz) and the induction motor is operated at no-load. A DSP (TMS320F2808) is utilized to control the motor speed and program the PWM pulse pattern.

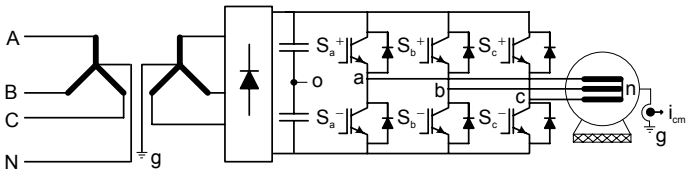


Fig. 12. Experimental setup for CMV/CMC measurement.

All methods are tested at an average switching frequency of 6.66 kHz. Operation at various M_i values is tested and only the results for M_i=0.8 (180.3 V_{rms}/51 Hz) are discussed. Figure 13 shows the phase current, CMC, CMV and the modulation signal for DPWM1, NSPWM, SVPWM, and AZSPWM1. LeCroy Waverunner 6050A oscilloscope has been utilized and the modulation signals have been measured with the PMA2 software. The phase current waveforms are sinusoidal and the PWM current ripple is comparable in all the methods as predicted in the simulations. The CMV comparison indicates that both DPWM1 and SVPWM have high CMV compared to others. NSPWM and AZSPWM1 have similar CMV values. Comparing the CMC characteristics, the difference is not as emphasized as the CMV characteristic, because dv/dt is the same. The switching instants result in sharp edge voltage pulses that cause high frequency currents through the capacitive paths and these current pulses have high magnitude in all methods. However, differences are still notable in terms of rms and peak CMC values and the CMC of SVPWM (107 mArms) and DPWM1 (108 mArms) are higher than the CMC of NSPWM (95 mArms) and AZSPWM1 (98 mArms). The CMC current peak values are 1.35 A for DPWM1, 1.10 A for SVPWM, 1.02 A for AZSPWM1 and 950 mA for NSPWM.

The microscopic view reveals the details. Figures 14 through 17 show the PWM cycle CMV/CMC waveforms. Since the PWM pulse pattern varies over a fundamental cycle, the PWM characteristics are θ dependent. As a result, the CMV/CMC characteristics also vary in space. When comparing the CMV/CMC characteristics, the worst CMV/CMC points are selected for each method and shown in the oscillograms. It can be seen that the CMV of DPWM1 (151.2 Vrms) and SVPWM (151.1 Vrms) are quite larger than those of NSPWM (98.3 Vrms) and AZSPWM1 (98.5 Vrms). NSPWM and AZSPWM1 have nearly the same RMS value. The CMC waveforms are better performance indicators. The peak values of CMC for all the methods are similar (950 mA for DPWM1, 1.02 A for SVPWM, 928mA for AZSPWM1, and 862 mA for NSPWM). The RMS value of CMC is slightly better for NSPWM compared to other methods.

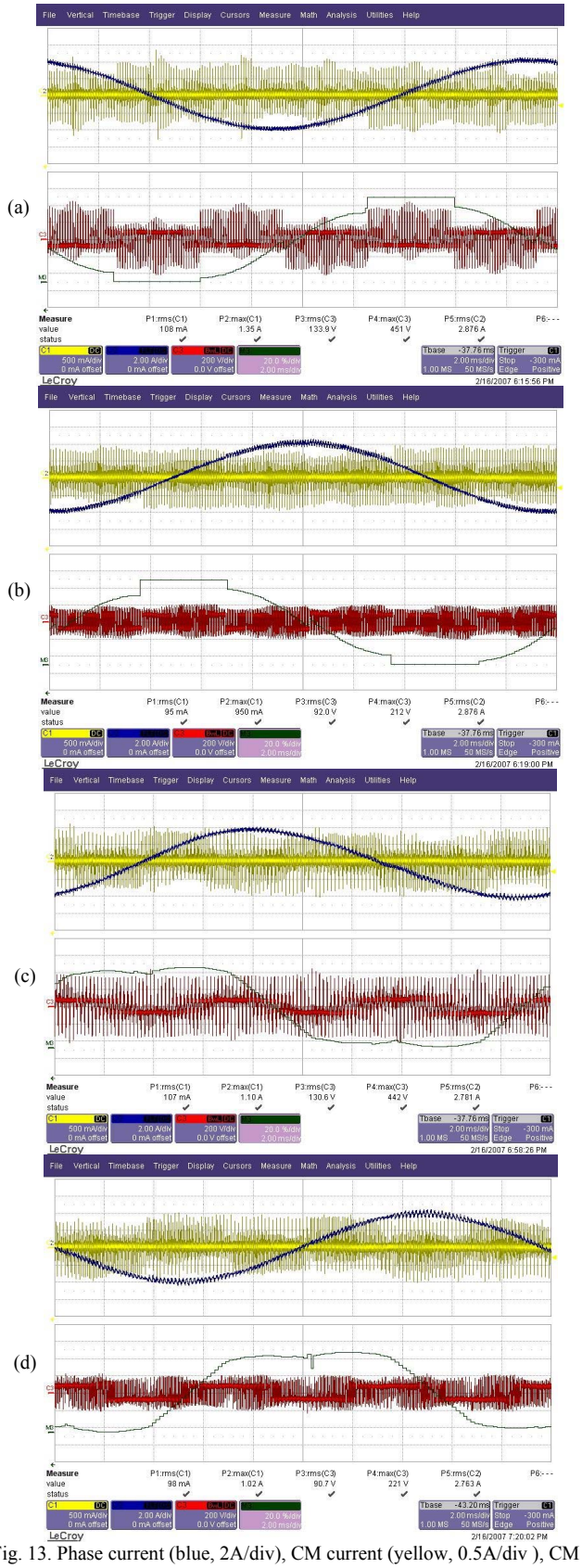


Fig. 13. Phase current (blue, 2A/div), CM current (yellow, 0.5A/div), CM voltage (red, 200V/div), and modulation signal (green, 0.2unit/div) waveforms for various PWM methods: (a) DPWM1, (b) NSPWM, (c) SVPWM, (d) AZSPWM1 (M_i=0.8 and f_s=10kHz).

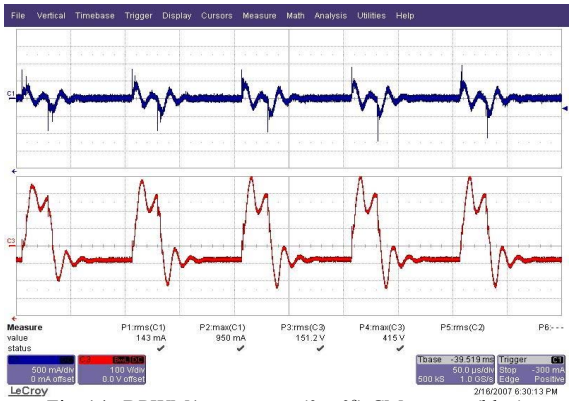


Fig. 14. DPWM1 worst case ($\theta \approx 0^o$) CM current (blue) and CM voltage (red) waveforms for M_i=0.8.

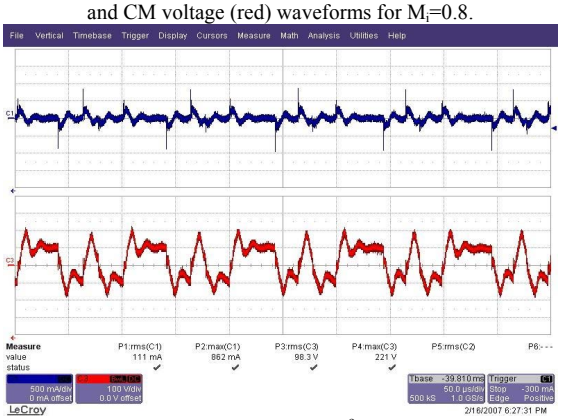


Fig. 15. NSPWM worst case ($\theta \approx 15^o$) CM current (blue) and CM voltage (red) waveforms for M_i=0.8.

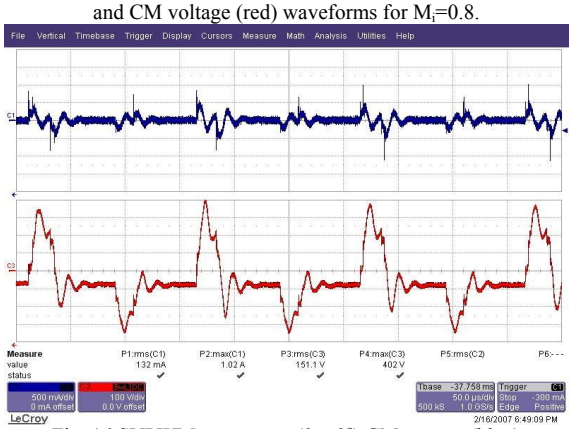


Fig. 16 SVPWM worst case ($\theta \approx 0^o$) CM current (blue) and CM voltage (red) waveforms for M_i=0.8.

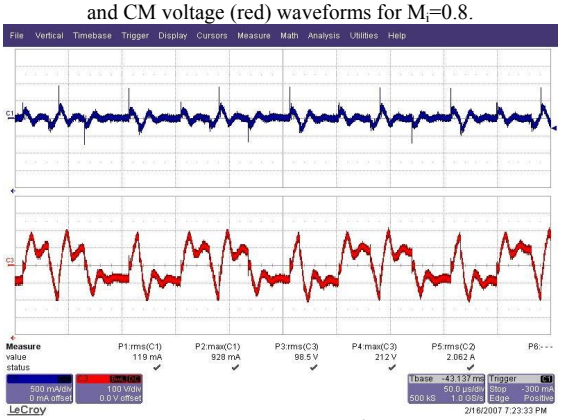
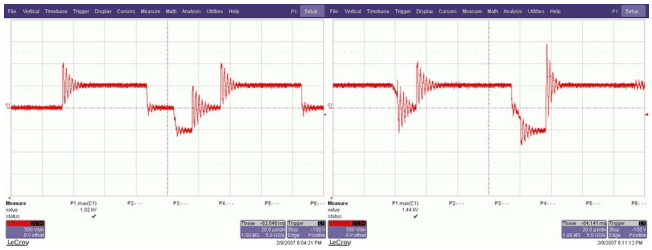


Fig. 17. AZSPWM1 worst case ($\theta \approx 20^o$) CM current (blue) and CM voltage (red) waveforms for M_i=0.8.

The line-to-line voltage pulse pattern of NSPWM is superior to AZSPWM1 (section V). Figure 18 shows that NSPWM places sufficient zero voltage time interval before pulse reversal occurs while the AZSPWM1 method experiences rapid change with nearly zero time interval between pulses. In long cable applications (70m), the AZSPWM1 method exhibits overvoltages (>1400V) while NSPWM performs satisfactorily.



(a) (b)

Fig. 18. Worst case line-to-line voltage pulse reversal for M_i=0.8 and f_s=10kHz: (a) NSPWM, (b) AZSPWM1, (500 V/div).

VIII. Conclusions

A near state (NS) PWM method with reduced CMV/CMC is introduced. The pulse pattern of NSPWM is defined and a simple scalar implementation is given. The output phase current and DC link current harmonic content, CMV/CMC, and line-to-line voltage pulse patterns are theoretically and analytically studied and compared with other PWM methods. The harmonic content on both DC and AC side currents is less than that of any other RCMV-PWM method and comparable with those of standard PWM methods. Although the line-to-line voltage pulse pattern is partially bipolar, there is always sufficient distance between the voltage pulses such that voltage reflection does not cause significant overvoltages (unlike AZSPWM1). Simulations and experiments verify the theory. The NSPWM method exhibits superior overall performance for $M_i > 0.6$. The method must be combined with a method with high CMV/CMC performance for $M_i<0.6$ for practical use.

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