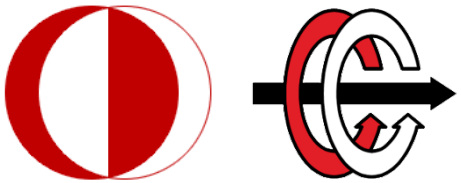
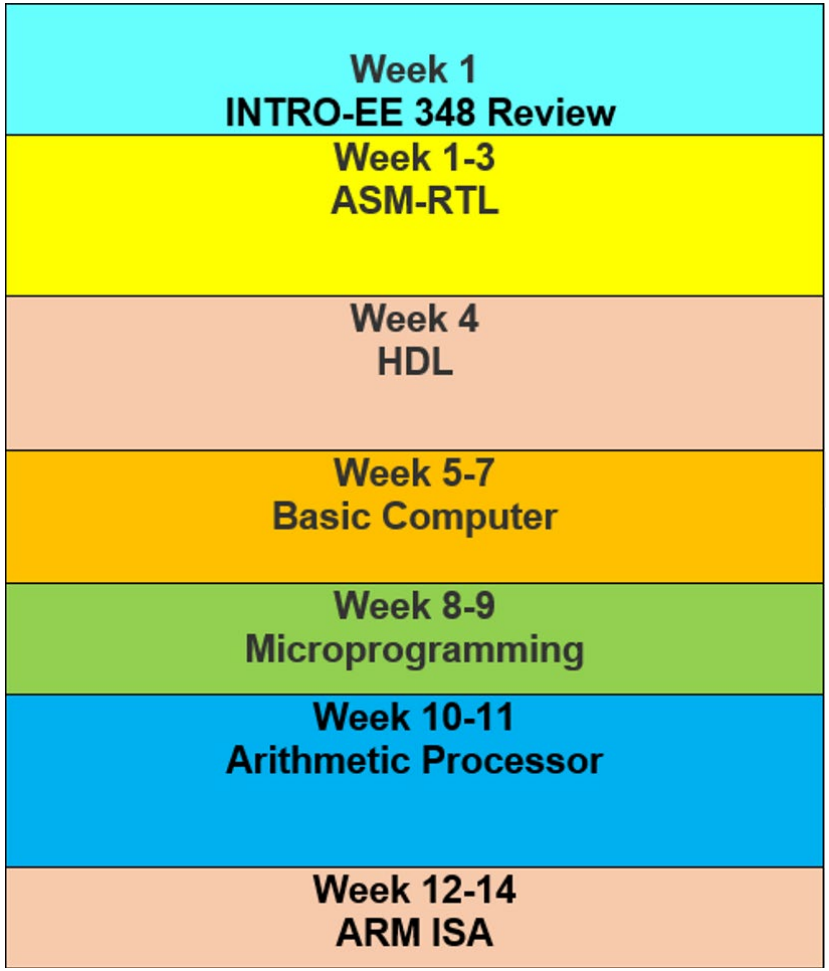


EE 445 Computer Architecture I

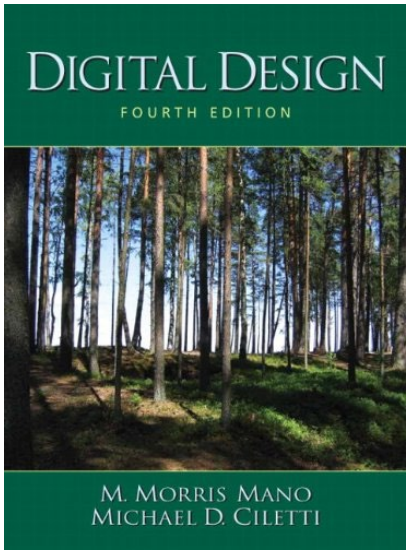
Schedule

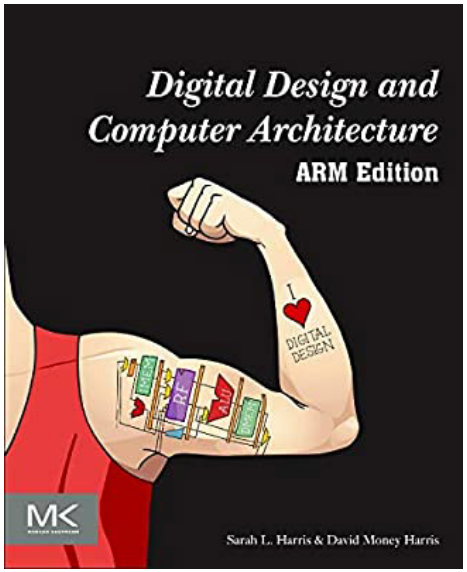

Week 1
INTRO-EE 348 Review
Week 1-3
ASM-RTL
Week 4
HDL
Week 5-7
Basic Computer
Week 8-9
Microprogramming
Week 10-11
Arithmetic Processor
Week 12-14
ARM ISA

Text Books

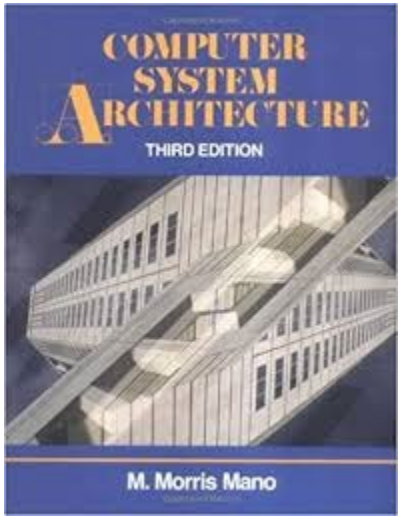
Copyright notice: Lecture Note Slides are compiled from the teaching material of these books, previous lecture notes of EE445 and additional resources. Part of the slides are entirely created by the instructors.

Digital Design (4th Edition)
M. Morris Mano, Michael D. Ciletti
Published by Prentice Hall, 2006





Computer System Architecture 3rd Ed.,
M. Morris Mano Prentice Hall, 1992
Computer System Architecture 2nd Ed.,
M. Morris Mano Prentice Hall, 1982



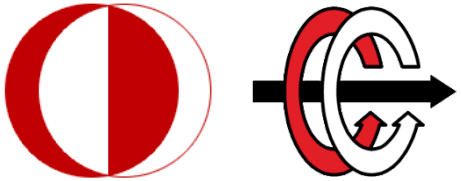
Harris & Harris, "Digital Design and Computer Architecture. ARM Edition", 1st Ed., Kaufmann, 2015.
We go on with this text book for EE446

Course Objective (Why should you take this course?)

- A smooth extension of EE348
- Describes how a computer works at EE348 level of detail on a simple fictitious Basic Computer
- Preparation for the advanced topics: pipelining, memory and I/O organization that are covered in EE446

Course Outline

- Introduction to Computer Architecture
- EE348 review
- Algorithmic State Machine
- Register Transfer Language
- HDL
- Basic Computer Architecture
- Computer Organization and Microprogramming
- Arithmetic Processor Design
- ARM Instruction Set Architecture

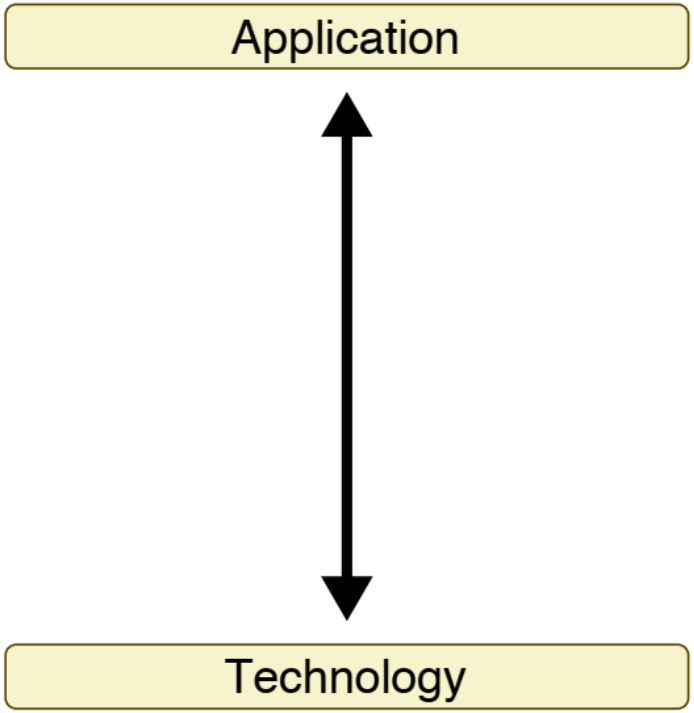


Introduction to Computer Architecture

Resources:

http://www.csl.cornell.edu/courses/ece4750
https://safari.ethz.ch/digitaltechnik/spring2020/doku.php
Computer Architecture
A Quantitative Approach, Sixth Edition

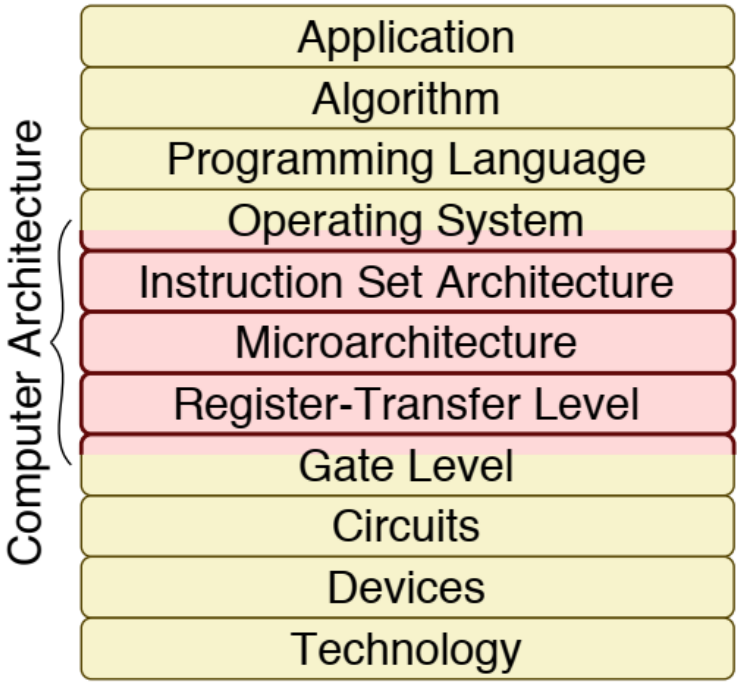
Computer Architecture



- abstraction/implementation layers
  - to execute information processing applications
  - efficiently using available manufacturing technologies

https://www.csl.cornell.edu/courses/ece4750/handouts/ece4750_overview.pdf

Computer Architecture



https://www.csl.cornell.edu/courses/ece4750/handouts/ece4750_overview.pdf

Sort an array of numbers

2,6,3,8,4,5 -> 2,3,4,5,6,8

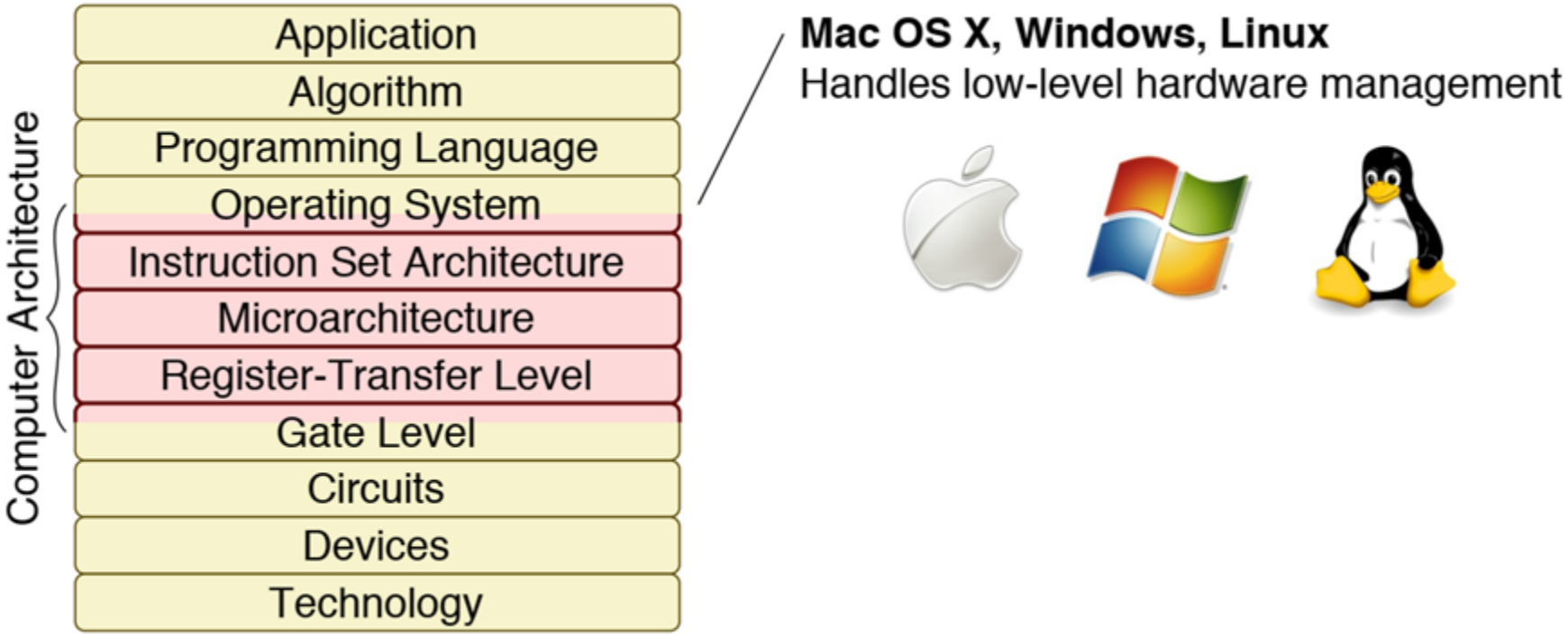
Out-of-place selection sort algorithm

1. Find minimum number in array
2. Move minimum number into output array
3. Repeat steps 1 and 2 until finished

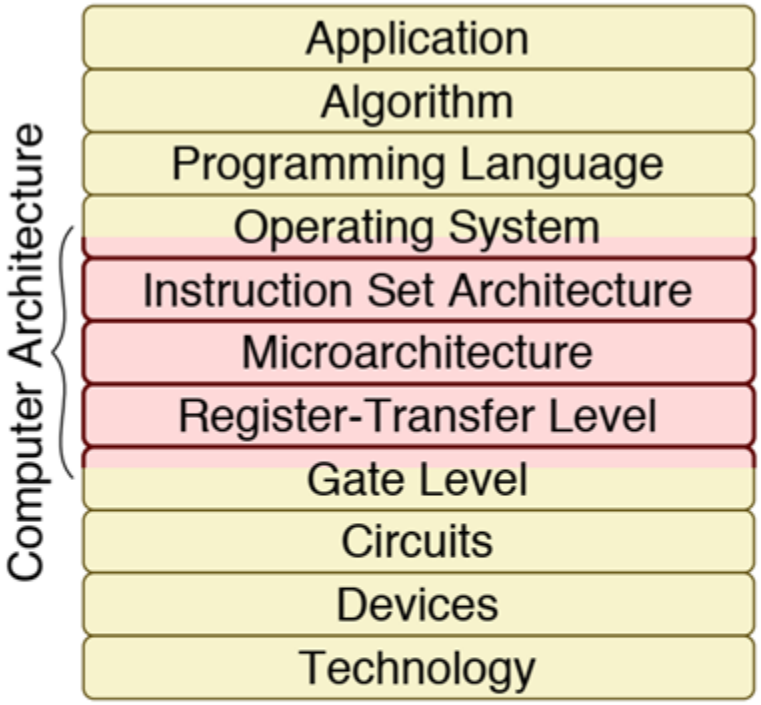
C implementation of selection sort

```
void sort( int b[], int a[], int n ) {
  for ( int idx, k = 0; k < n; k++ ) {
    int min = 100;
    for ( int i = 0; i < n; i++ ) {
      if ( a[i] < min ) {
        min = a[i];
        idx = i;
      }
    }
    b[k]   = min;
    a[idx] = 100;
  }
}
```

Computer Architecture



Computer Architecture



- Instruction Set Architecture (ISA):
  - Structure and behavior of the computer as seen by the programmer
  - There can be many implementations of the same ISA

MIPS32 Instruction Set

Instructions that machine executes

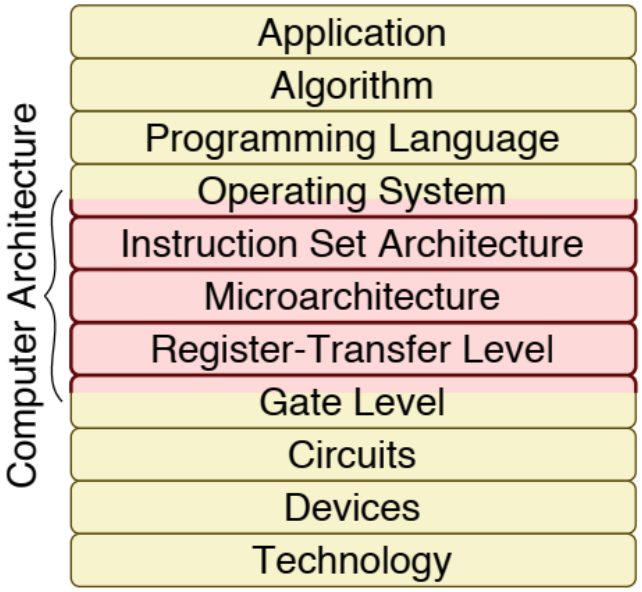
```
blez  $a2, done
move  $a7, $zero
li    $t4, 99
move  $a4, $a1
move  $v1, $zero
li    $a3, 99
lw    $a5, 0($a4)
addiu $a4, $a4, 4
slt   $a6, $a5, $a3
movn  $v0, $v1, $a6
addiu $v1, $v1, 1
movn  $a3, $a5, $a6
```

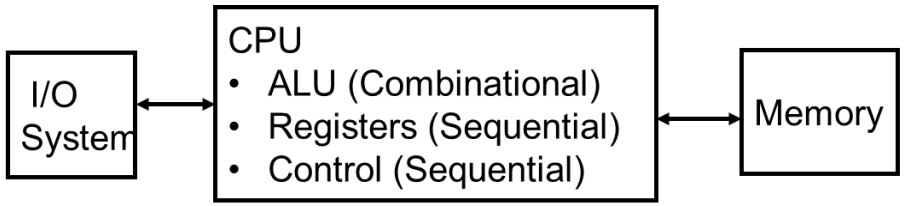
Instruction Set Architecture (ISA)

- Represents
  - all the information necessary to write a machine language program that will run correctly on the machine
  - the conceptual structure and functional behavior
- Abstracts away
  - the organization of the data flows and controls
  - the logic design
  - the physical implementation.
- Enables implementations of varying cost and performance to run identical software
- Includes
  - Addressing modes
  - Operand specifications
  - Operation specifications
  - Control flow instructions

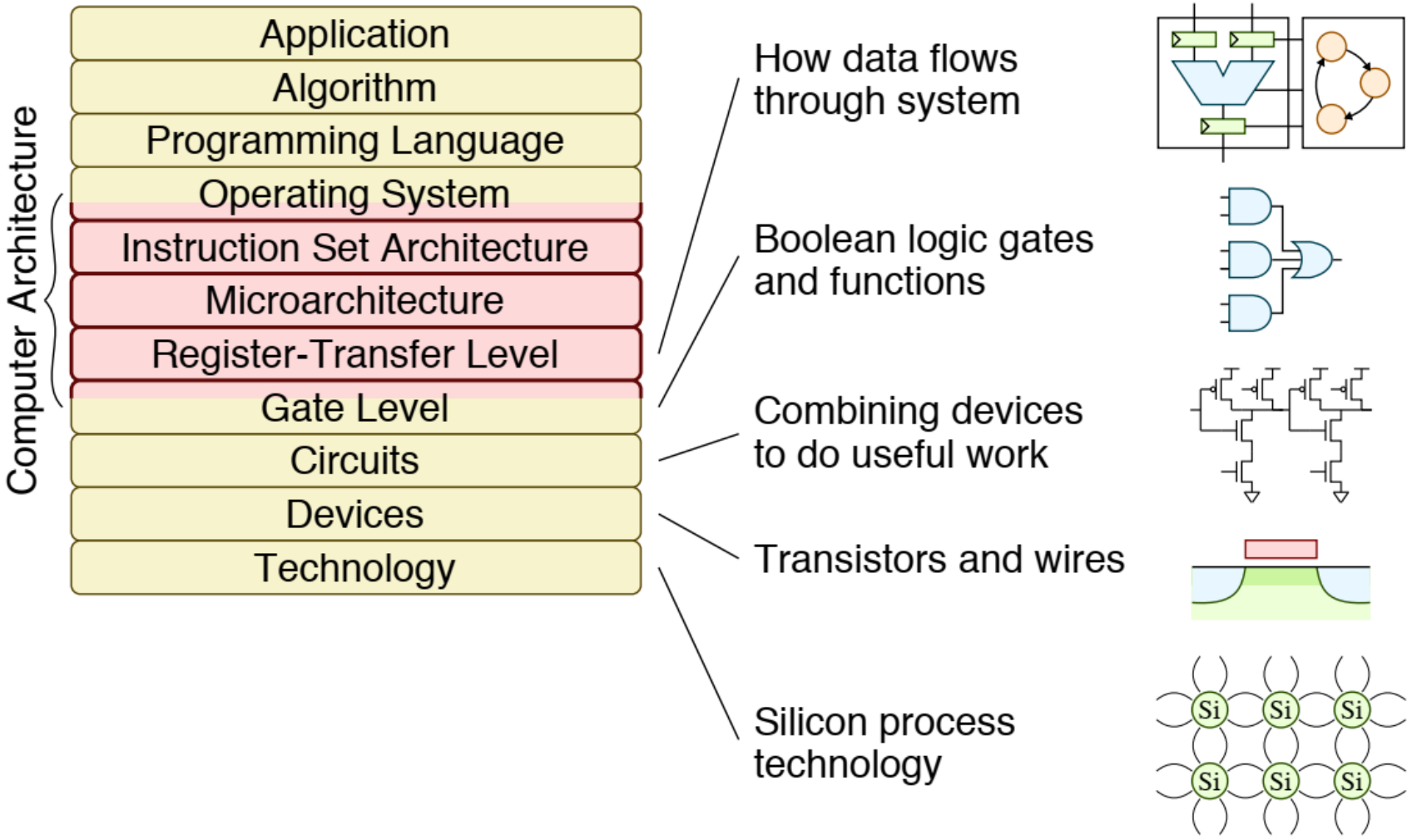
Microarchitecture

- Microarchitecture/Organization: The specific arrangement of registers, ALUs, finite state machines (FSMs), memories, and other logic building blocks needed to implement an ISA.
- Example: AMD Opteron and the Intel Core i7 implement the 80x86 instruction set with very different pipeline and cache organizations

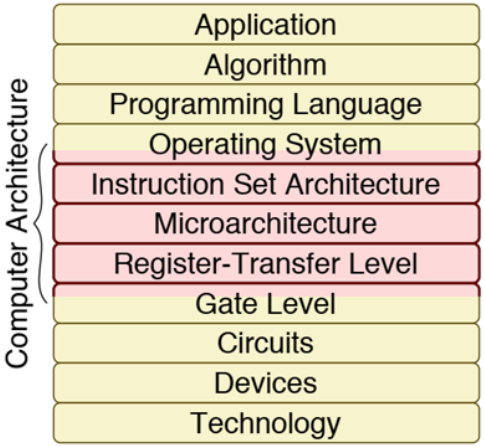




Computer Architecture



EE445 Coverage

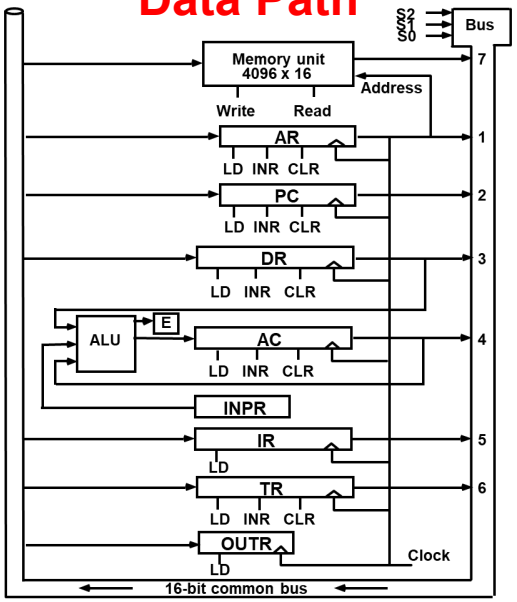


EE445 focuses on these layers using a fictitious Basic Computer

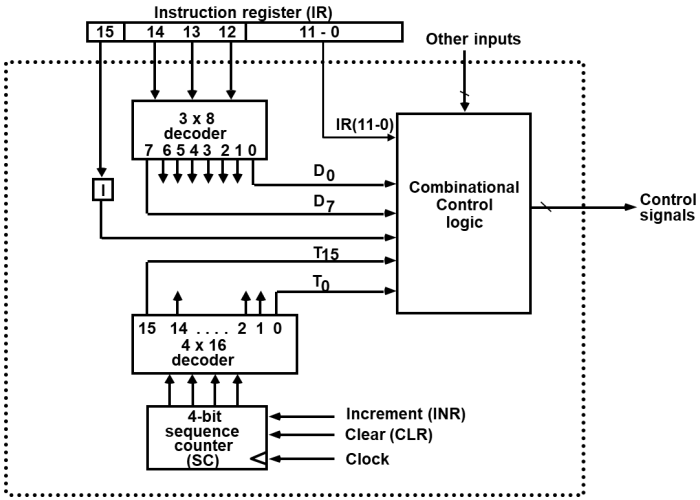
Instruction Set

Symbol	Hex Code I = 0	Hex Code I = 1	Description
AND	0xxx	8xxx	AND memory word to AC
ADD	1xxx	9xxx	Add memory word to AC
LDA	2xxx	Axxx	Load AC from memory
STA	3xxx	Bxxx	Store content of AC into memory
BUN	4xxx	Cxxx	Branch unconditionally
BSA	5xxx	Dxxx	Branch and save return address
ISZ	6xxx	Exxx	Increment and skip if zero
CLA	7800		Clear AC
CLE	7400		Clear E
CMA	7200		Complement AC
CME	7100		Complement E
CIR	7080		Circulate right AC and E
CIL	7040		Circulate left AC and E
INC	7020		Increment AC
SPA	7010		Skip next instr. if AC is positive
SNA	7008		Skip next instr. if AC is negative
SZA	7004		Skip next instr. if AC is zero
SZE	7002		Skip next instr. if E is zero
HLT	7001		Halt computer
INP	F800		Input character to AC
OUT	F400		Output character from AC
SKI	F200		Skip on input flag
SKO	F100		Skip on output flag
ION	F080		Interrupt on
IOF	F040		Interrupt off

Data Path

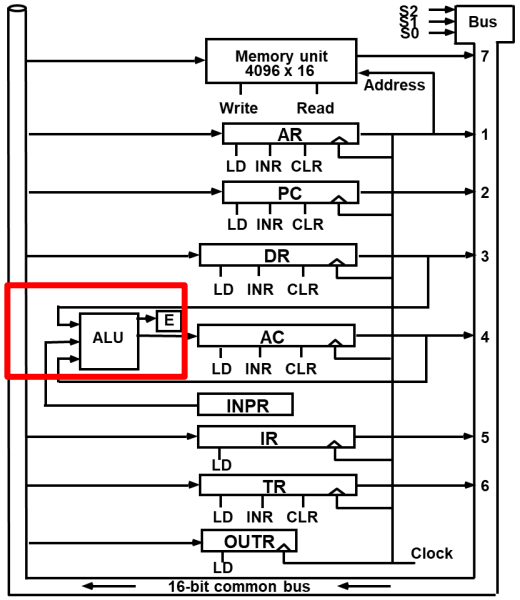


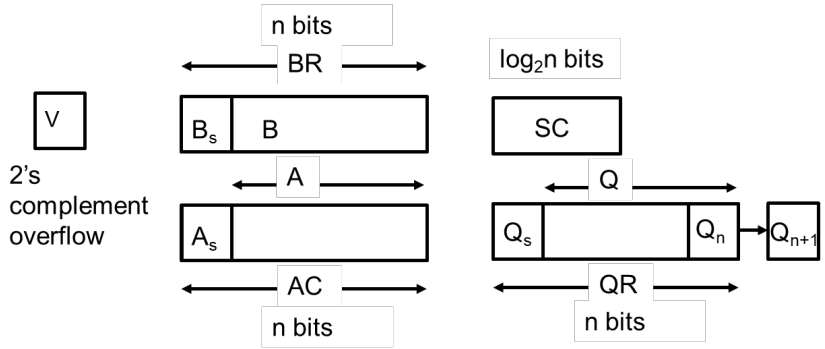
Controller



EE445 Coverage

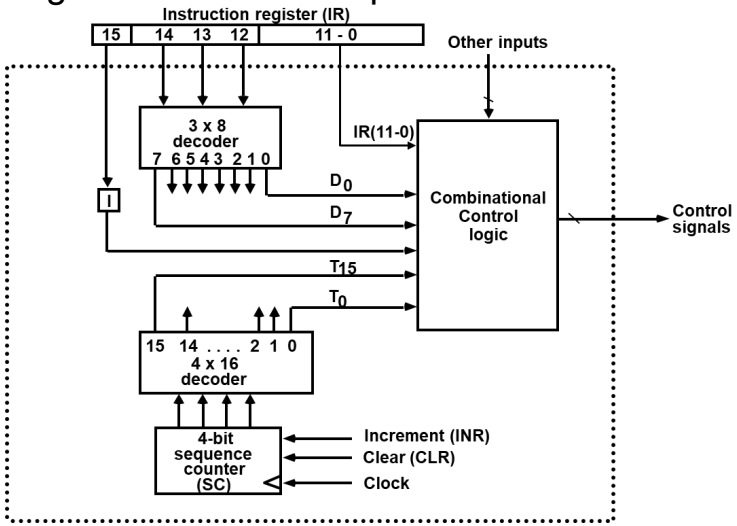
Data Path





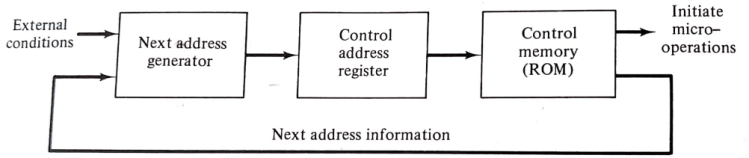
Hardwired control

Control signals are circuit outputs



Microprogrammed Control

Control signals are the control memory word contents



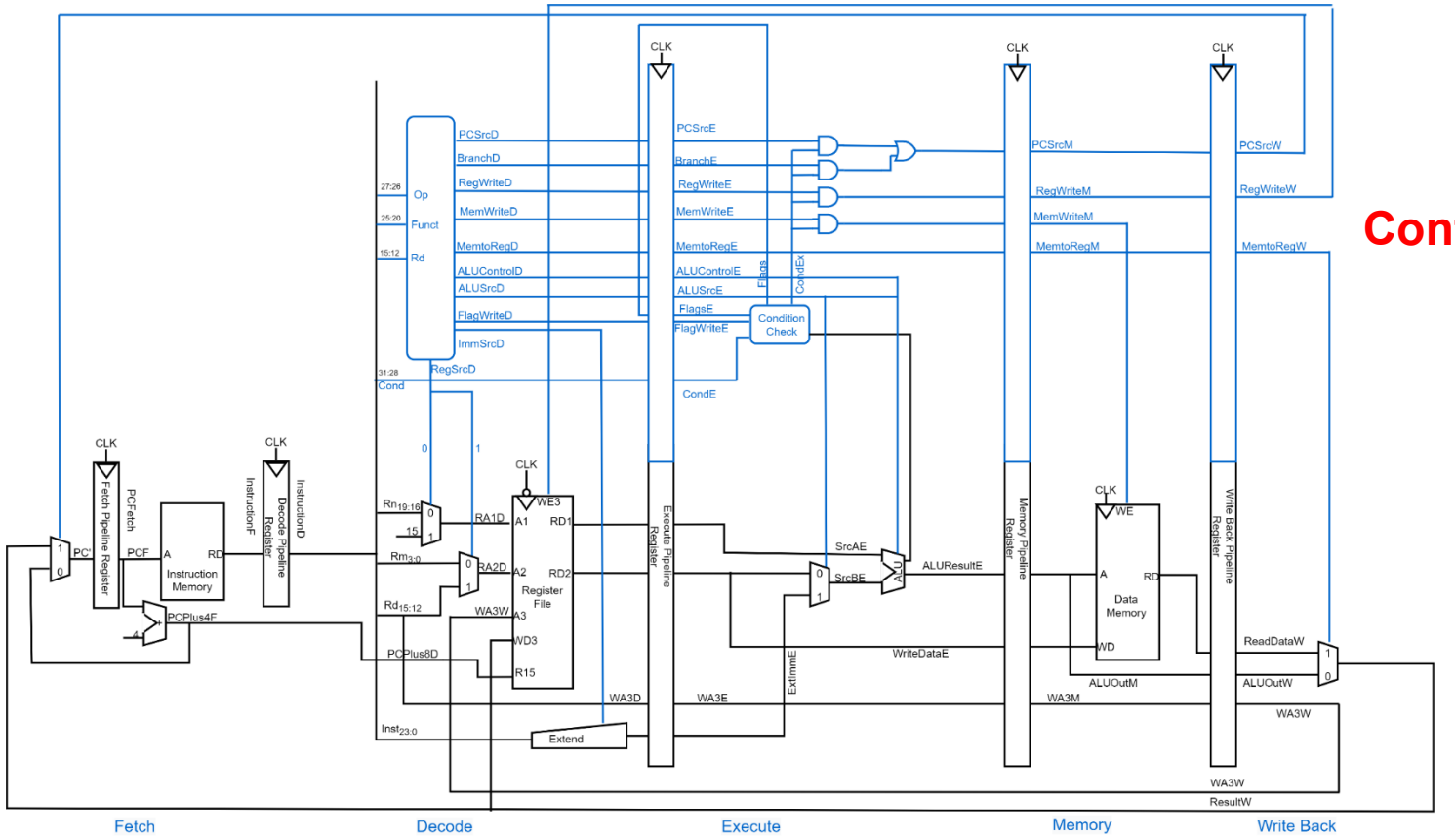
ALU implementation, hardware algorithms for multiplication and division➔ Needs EE348 refresher ☺

A Sneak Peek into EE446 ☺

A Pipelined Microarchitecture for a *representative* subset of ARM ISA

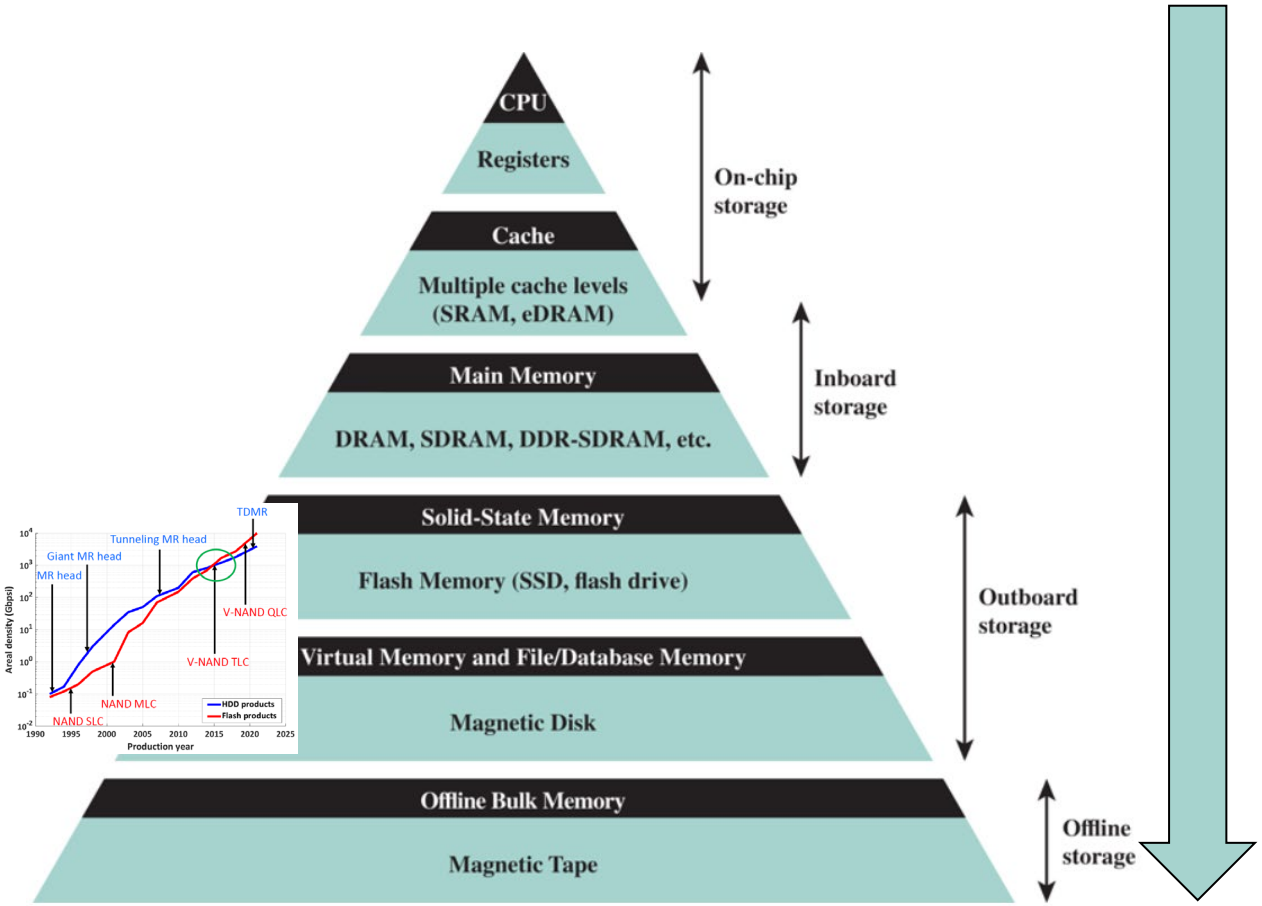
```
LDR Rd, [Rn, imm12]
STR Rd, [Rn, imm12]
ADD Rd, Rn, imm8
B BTA
```

Instruction Set



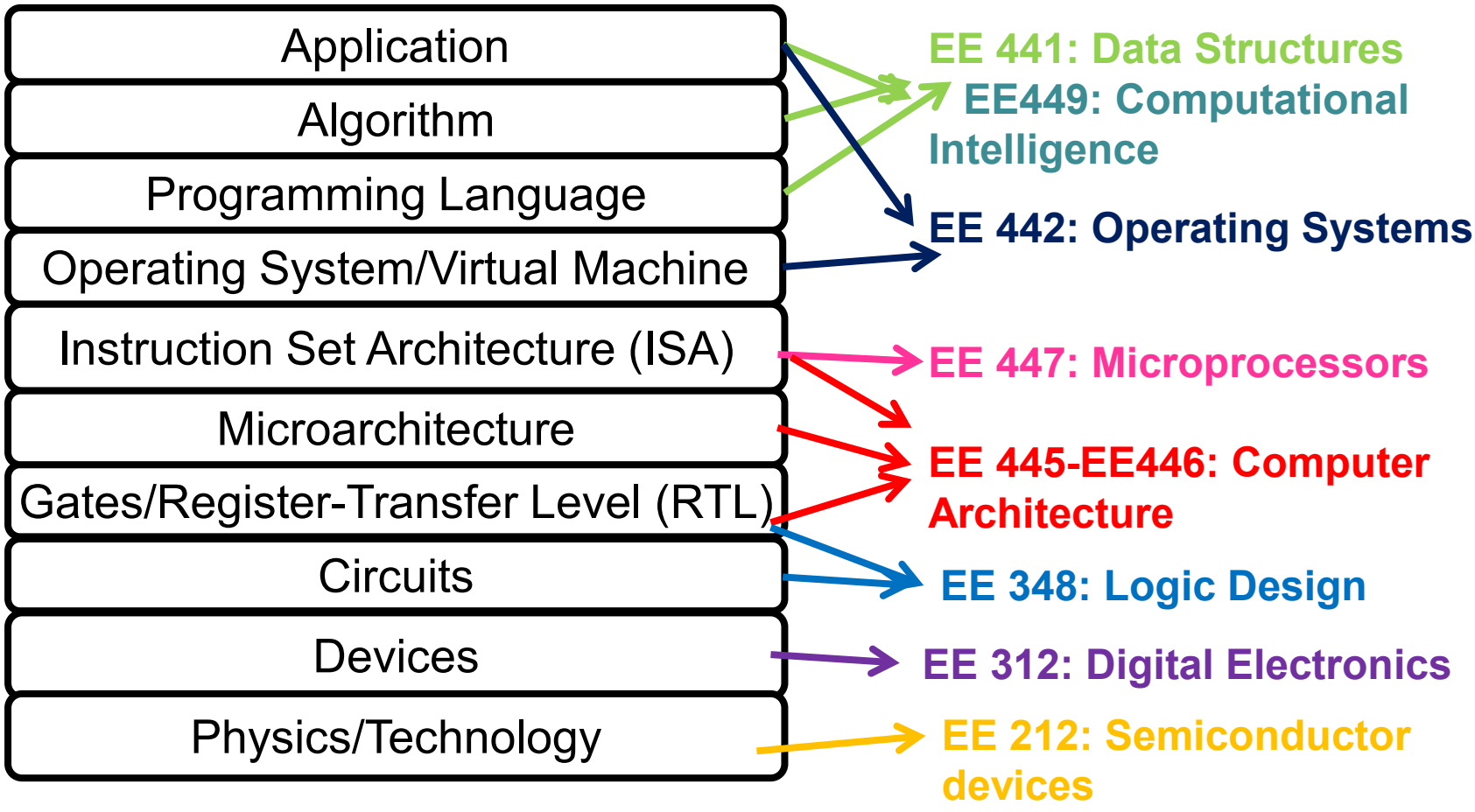
A Sneak Peek into EE446 ☺

Memory Hierarchy



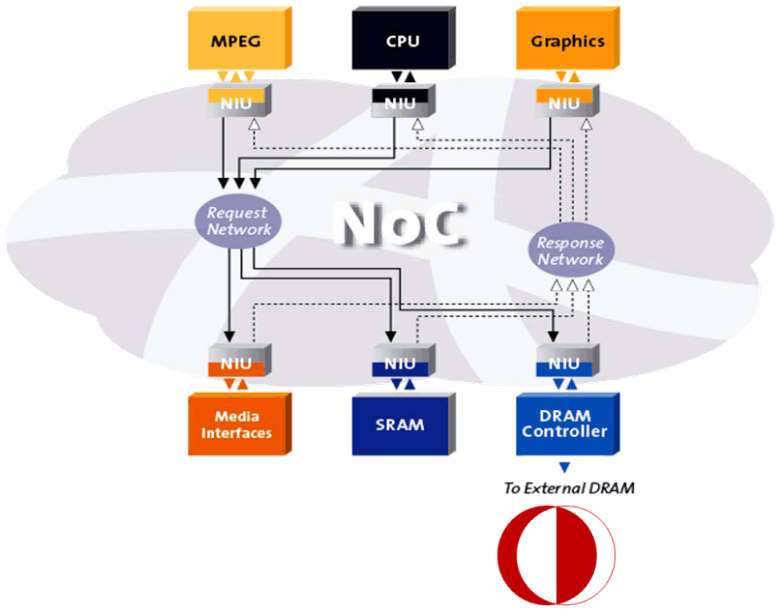
- Cost per byte decreases
- Average access time increases
- Average data transfer rate decreases
- Total memory size increases
- Frequency of access decreases ➔Principle of locality
- Data contained in a lower level are a superset of the next higher level ➔ Inclusion property

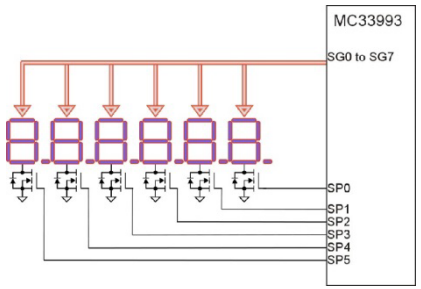
Computer Architecture in METU EE



Computers/Computer Architecture in METU EE

EE 444: Computer Networks



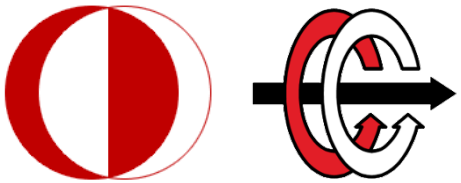


EE 447: Microprocessors: I/O device interfacing

Many computing Devices

Grading

- 4 Short Exams: 52% (13% each)
- Final exam: 36%
- HDL Homeworks: 12%
- 5% bonus for attendance >=80%



Introduction to Computer Architecture