

# EE 446 Computer Architecture II

Spring 2026

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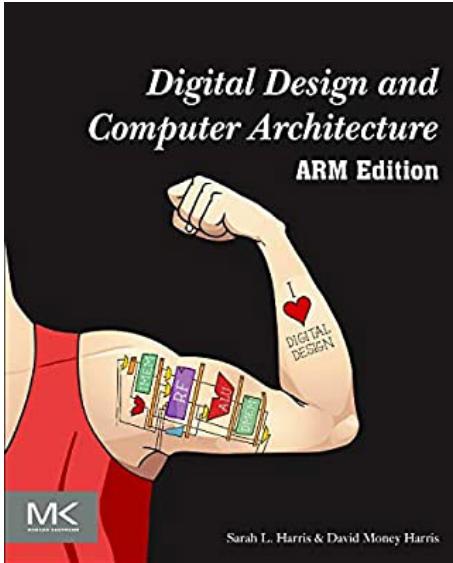
# Administrative Details

- Instructor Ece Güran Schmidt
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  - Web page: <http://users.metu.edu.tr/eguran/>
- Teaching assistants:
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- Schedule:
  - Tuesday, 13:40 - 14:30, Thursday, 09:40 - 11:30 @EA208
- Follow
  - <https://odtuclass.metu.edu.tr/>  
for lecture slides, all class material and announcements
  - Your [e123456@metu.edu.tr](mailto:e123456@metu.edu.tr) email

# Required

- Prerequisite(s): EE445
- Core course for Computer Option

Copyright notice: Lecture Note Slides are compiled from the teaching material of these books, previous lecture notes of EE446 and additional resources. Part of the slides are entirely created by the Instructors



Harris & Harris, "Digital Design and Computer Architecture. ARM Edition", 1st Ed., Kaufmann, 2015.

2/9/2026

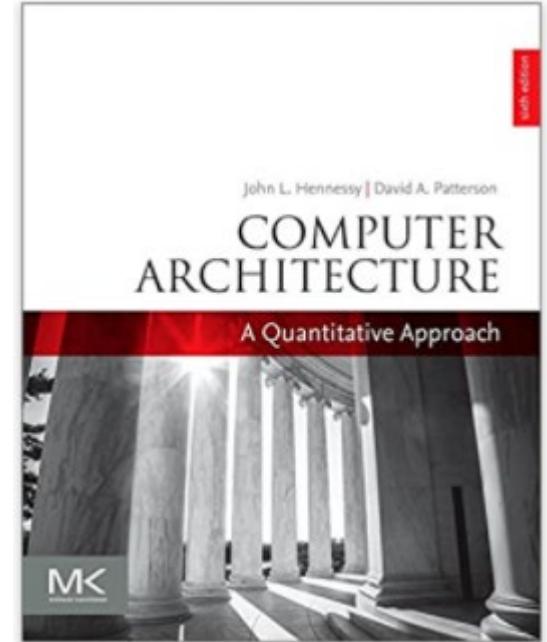


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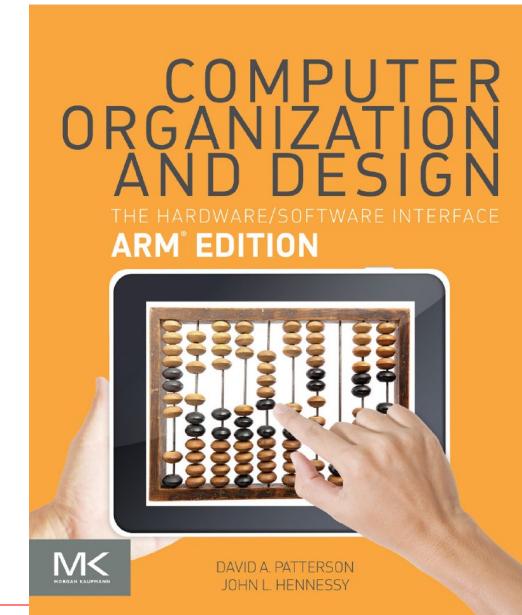


# Text Books

Computer Architecture, A Quantitative Approach, 6th Edition, John Hennessy, David Patterson



Computer Organization and Design ARM Edition: The Hardware Software Interface (The Morgan Kaufmann Series in Computer Architecture and Design) 1st Edition by David A. Patterson, John L. Hennessy



# Course Coverage: EE445

In **EE-445** we studied:

- Computer System components
- Instruction Set Architecture (ISA) design and tradeoffs
- Hardwired and microprogrammed control for basic multi-cycle machines
- Arithmetic algorithms and implementation in hardware

# Course Coverage: EE446

- Will complete the missing theoretical pieces to obtain a solid Computer Architecture/Organization background:
  - Single-Cycle datapath/controller design
  - Multi-cycle datapath/controller design
  - Pipelining, superscalar operation, and parallel processing
  - Advanced memory hierarchies, and multiprocessor buses
  - Software interactions
- In addition you will get some practical experience in the lab by applying what you learnt in EE-445/446 sequence.

# Course Outline

- Introduction to Computer Architecture
- Part I: Implementations of ARM Microarchitecture: Single cycle, multi cycle, pipelined. A more comprehensive coverage of pipelining, branch prediction
- Part II: Memory Hierarchy: Memory, Virtual Memory, Cache
- Part III: Advanced Topics: Superscalar Processors, possibly more topics

# Grading

- Laboratory Work+ Class Project: 40%
- 3 Short Exams: 30%
- Final exam: 30%
- 5% bonus for attendance  $\geq 80\%$ .
- Students who do not attend or get zero performance grade from 2nd, 3rd and 4th experiments will get N/A from the EE446 course.

# Attendance beyond 5% Bonus

- What do you get if you attend:
  - Some explanations, examples, and problem-solving approaches are developed only during live lectures.
  - My experience and research outputs in this subject
- Problem solving
  - The discussions in the class may be reflected in the exams
  - Exams may include questions based on material explained or developed during lectures, including examples and reasoning that are not explicitly written on the slides.
  - New Problems solved in class addition to the posted ones. Their solutions will not be separately posted.
- Attendance is not mandatory; there is no penalty
  - Students can pass and get an AA the course without attending lectures; however, students who attend regularly typically perform better.
  - All exam questions are derived from topics officially covered in the course.

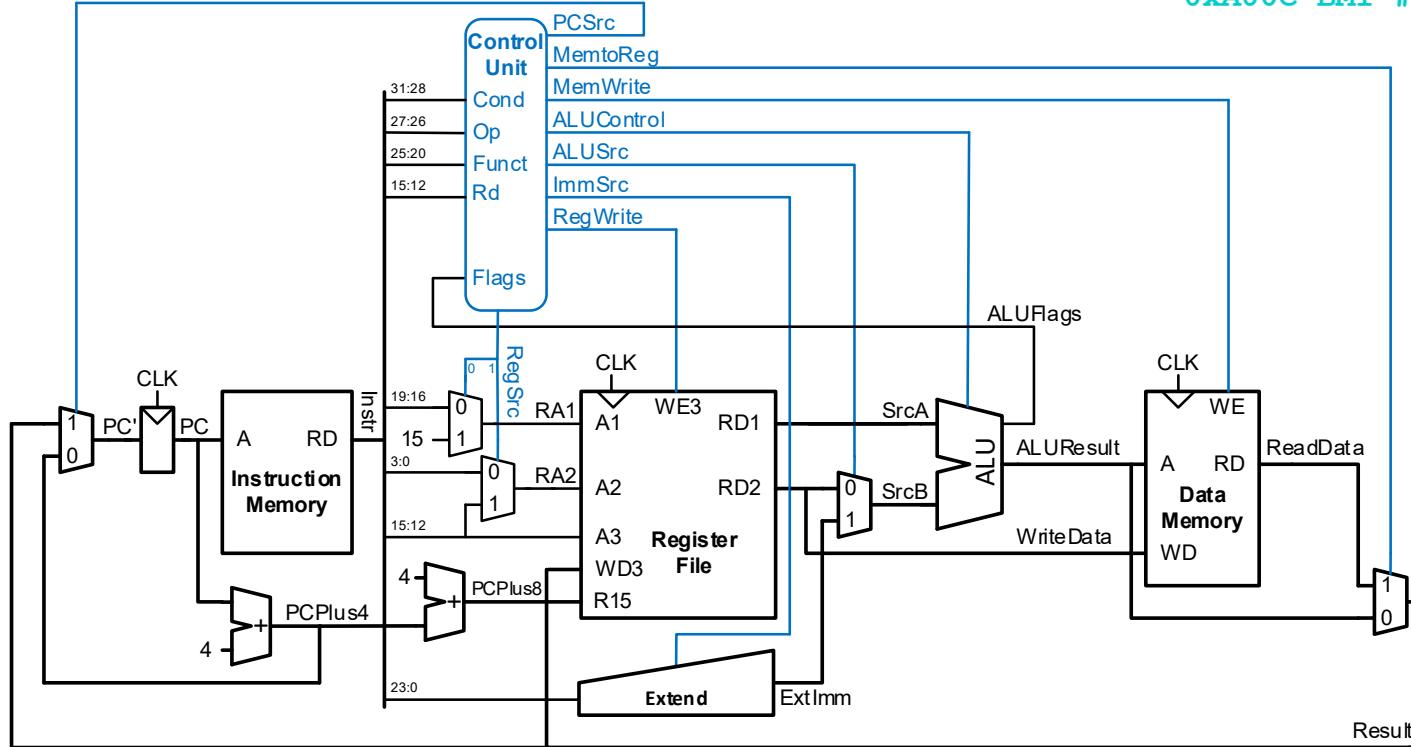
# LAB 2 Single Cycle Processor

0xA000 LDR R2, R0, #40

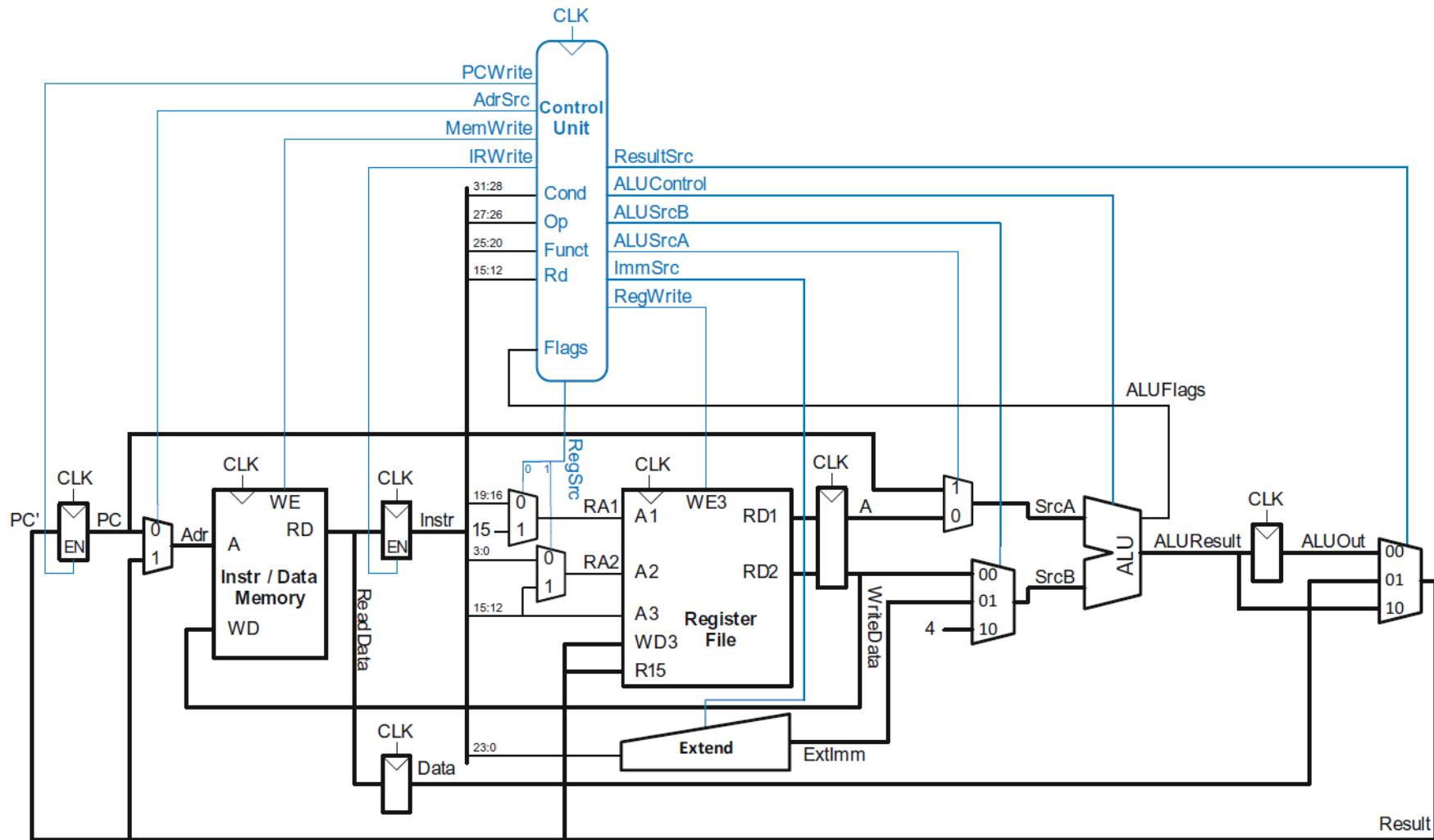
0xA004 AND R3, R9, R10

0xA008 STR R4, R1, #20

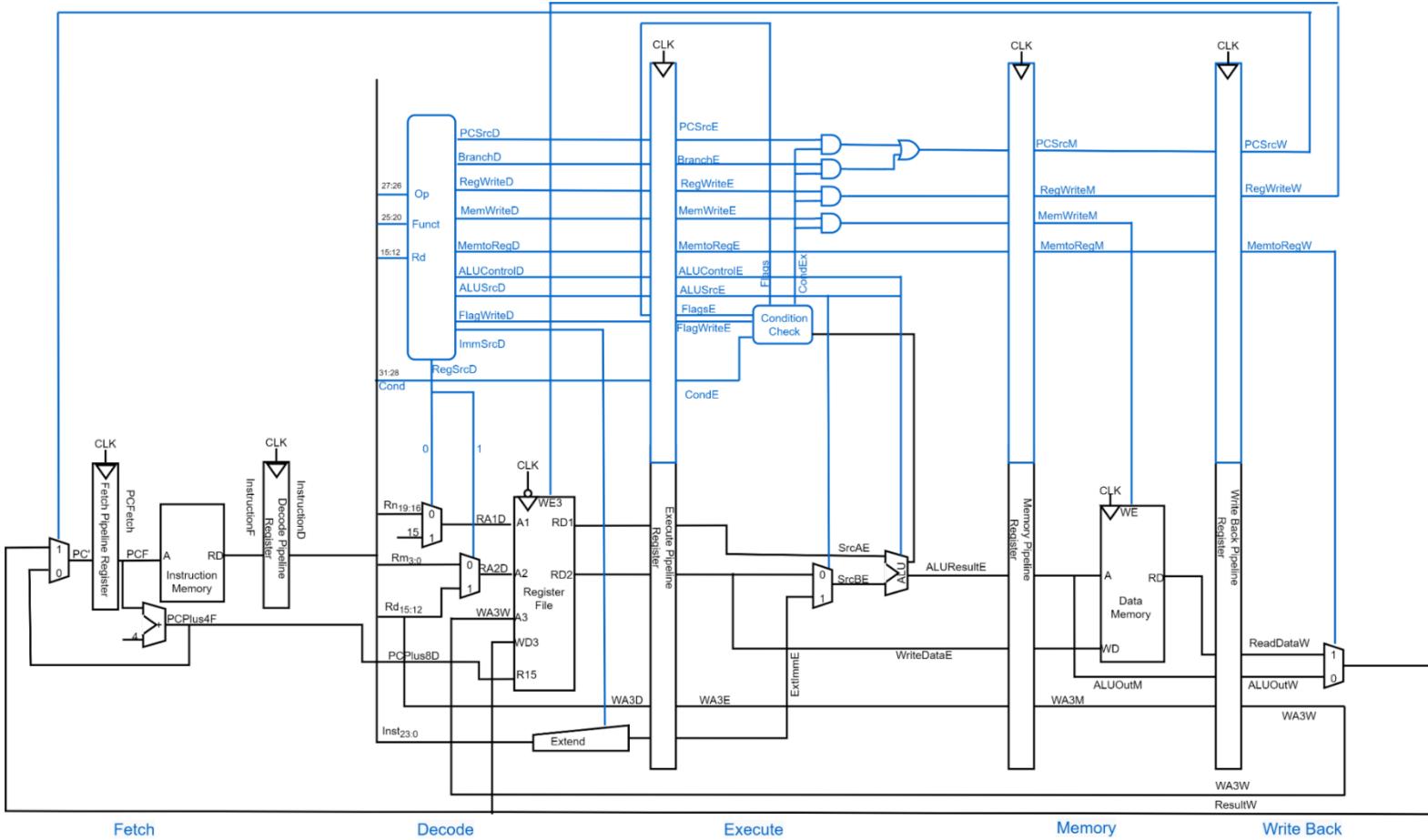
0xA00C BMI #10



# LAB 3 Multi Cycle Processor



# LAB 4 Pipelined Processor



Fetch

Decode

Execute

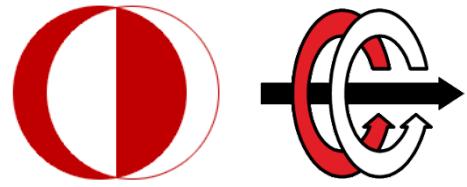
Memory

Write Back



# A note about plagiarism

- Copying work from any other resource (web page, your friend's report, older resources you have found,etc.) during preliminary work or sharing information or code files during sessions is considered cheating.
- Automated tools such as ChatGPT are allowed if the output is changed sufficiently to be different from other students; otherwise, it will count as plagiarism.
- All laboratories and preliminary works must be done individually unless said otherwise.



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