

COURSE OUTLINE

EE 445 COMPUTER ARCHITECTURE I 2020-21 Fall Term

Instructors:

Ece Güran Schmidt
Rm EA-402 Ph: 210 2339, e-mail: eguran@metu.edu.tr

Teaching assistants:

Can Çakıröz	Rm EA-405,	e-mail: cakirgoz@metu.edu.tr
Kamil Sert	Rm EA-405,	e-mail: ksert@metu.edu.tr
Fatih Yazıcı	Rm EA-405,	e-mail: fyazici@metu.edu.tr

Schedule:

Asynchronous video lectures

Synchronous Q & A group sessions, Quizzes Tuesday: 13:40 to 15:30, Thursday: 13:40

Course objective: Computers are integrated to our daily life and jobs. As a first step in becoming a computer designer or in writing better software, understanding the hardware layers together with software interface of a computer is critical. In this course, we will first review digital design fundamentals and introduce RTL, ASM, HDL concepts. Then we will study the basics of computer system organization, performance and energy issues, and instruction set architectures. We will study macro-coding concepts, hardware and micro programmed control for single- and multi-cycle datapath designs.

EE-446 Computer Architecture II will follow to study more advanced computer architecture concepts such as arithmetic processor design, pipelining, memory and I/O organization, multiprocessors, etc.

Topics: RTL. Algorithmic state machines. CPU organization. Arithmetic logic unit. Process control architectures. Instruction modalities. Microprogramming.

Pre-requisite: EE348

Some references:

Mano & Kime, "Logic and Computer Design Fundamentals", 4th Ed., Prentice Hall, 2008.

Mano "Digital Design", 4th Ed., Prentice Hall, 2008.

Mano, "Computer System Architecture", 3rd Ed., Prentice Hall, 1992

Harris & Harris, "Digital Design and Computer Architecture. ARM Edition", 1st Ed., Kaufmann, 2015.

Patterson & Hennessy, "Computer Organization and Design" (4th/5th Ed.), Kaufmann, 2014

Stallings, "Computer Organization & Architecture" (7th Ed. or later), Pearson, 2006.

Grading:

- Programming and Handwritten Assignments: 30%
- Quizzes: 30%
- Final exam: 40%
- Students who miss all the quizzes or who do not submit any homework will be graded as NA ("Not Available").

Homework: Verilog projects, written assignments will be assigned throughout the term. Details of the homework policy will be announced later.

Policy:

We will have proctored synchronous examinations (Quizzes and Final). The examinations will be conducted according to the METU Department of Electrical and Electronics Engineering Principles of Online Exam with Audiovisual Equipment.

Sunday	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday
	12.10. ASM video 1	13.10. Synchronous Lecture INTRO	14.10.	15.10.	16.10.	17.10.
18.10.	19.10. ASM video 2 RTL video 1	20.10. Q&A	21.10.	22.10.	23.10.	24.10.
25.10.	26.10. RTL video 2	27.10. Synchronous Lecture ASM-RTL	28.10.	29.10. Public Holiday	30.10.	31.10.
01.11. ASM-RTL Assignment Due	02.11. HDL video 1	03.11. Q&A	04.11.	05.11. ASM RTL Quiz	06.11.	07.11.
08.11.	09.11. HDL video 2	10.11. Synchronous Lecture HDL	11.11.	12.11.	13.11.	14.11.
15.11.	16.11. BC video 1	17.11. Q&A	18.11.	19.11. HDL Quiz	20.11.	21.11.
22.11.	23.11. BC video 2	24.11. Synchronous Lecture BC	25.11.	26.11.	27.11.	28.11.
29.11.	30.11. BC video 3	01.12. Synchronous Lecture BC	02.12.	03.12. BC Quiz	04.12.	05.12.
06.12. BC Problem Assignment due	07.12. MP video	08.12. Synchronous Lecture MP	09.12.	10.12.	11.12.	12.12.
13.12. BC Verilog Assignment due	14.12. Arithmetic video 1	15.12.	16.12.	17.12. BC MP Quiz	18.12.	19.12.
20.12.	21.12. Arithmetic video 2	22.12. Q&A	23.12.	24.12.	25.12.	26.12.
27.12.	28.12. Arithmetic video 3	29.12. Synchronous Lecture Arithmetic	30.12.	31.12. New Year's Eve	01.01. Public Holiday	02.01.
03.01.	04.01. ARM ISA video 1	05.01.	06.01.	07.01. Arithmetic Quiz	08.01.	09.01.
10.01. Arithmetic Verilog Assignment due	11.01. ARM ISA video 2	12.01. Synchronous Lecture ARM ISA	13.01.	14.01.	15.01. Last day of lectures	16.01.