```
+ CBD=3.1E-15 CBS=3.1E-15)
MPA 4 1 5 5 PMOSFET W=20U L=2U
MPB 2 3 4 5 PMOSFET W=20U L=2U
MNB 2 3 0 0 NMOSFET W=4U L=2U
MNA 2 1 0 0 NMOSFET W=4U L=2U
VINA 1 0 PULSE(0V 5V 0 0 0 10NS
+ 20NS)
VINB 3 0 DC 0V PULSE(0V 5V 0 0
+ 0 20NS 40NS)
.DC VINA 0 5 0.1
.PLOT DC V(4)
.TRAN 1NS 40NS
.PRINT TRAN V(VINA) V(VINB)
+ V(4)
.END
```

Note that VINB has a default DC value of 0 V so that the .DC sweep over VINA will produce both output logic states.

The result of the .DC sweep is the voltage transfer characteristic shown in Figure 24.12a. Note the voltage transfer characteristic is slightly displaced from the center. The results of the .TRAN time sweep are shown in Figure 24.12b. The logical NOR function is easily recognized, the output is high when both inputs are low and low for any input high. Note that the output fall time is approximately equal to the output rise time.

24.4 CMOS AND AND OR GATE

AND and OR gates in CMOS digital circuits are obtained by simply feeding the output of CMOS NAND and NOR gates into CMOS inverters, as shown in Figures 24.13 and 24.14, respectively. Note the intermediate NAND and NOR outputs can be used to drive logic gates other than their respective inverters and thus applications requiring complementary logic signals are easily facilitated.

24.5 CMOS COMPLEX LOGIC GATES (AOIs AND OAIs)

The previous sections show that ANDing of signals is naturally performed with CMOS circuitry by series connection of N-channel MOSFETs and parallel connection of complementary P-channel MOSFETs. Also, ORing of signals is performed in CMOS circuitry by parallel connection of NMOS transistors and series connection of the complementary PMOS transistors. Combining NMOS devices in series combinations with the corresponding PMOS devices in parallel and other NMOS transistors in parallel with their corresponding PMOS transistors in series within the same CMOS circuit, allows realization of more complex logic functions such as AND-OR-inverts or AOIs.

Modification of CMOS NOR Gate Block Diagram to Perform AND-OR-Inverting

Before introducing a CMOS AND-OR-invert gate, reexamine the two-input CMOS NOR gate of Figure 24.9a. As discussed, the NOR function is realized by parallel combinations of NMOS transistors and series combinations of the complementary PMOS transistors. Figure 24.15 shows a block diagram representing the parallel and series combinations of N- and P-channel devices. This block diagram represents the logic function

$$V_{OUT} = V_A \; NOR \; V_B$$

If the blocks dedicated to accommodate V_A are modified to perform V_A AND V_C and the blocks dedicated to V_B are modified to perform V_B AND V_D, as in Figure 24.16, the logical function

$$V_{OUT} = (V_A \; AND \; V_C) \; NOR \; (V_B \; AND \; V_D)$$

is performed. The circuitry needed to realize V_A AND V_C is a series combination of NMOS devices for the block labeled N_A AND N_C and a parallel combination of complementary PMOS devices for the block labeled P_A AND P_C. Likewise, the blocks labeled N_B AND N_D and P_C AND P_D are represented by series combinations of N-channel MOSFETs and parallel combinations of complementary P-channel MOSFETs, respectively. Figure 24.17a shows the circuitry for such a gate. This is a CMOS AND-OR-invert gate.

Input ANDing Sections

Examining the complex CMOS logic circuit of Figure 24.17a, two series NMOS branches appear between the output and ground. Either of these can serve as an output pull-down path to ground when the corresponding two inputs are high. That is, an output pull-down path exists through N_A and N_C if V_A and

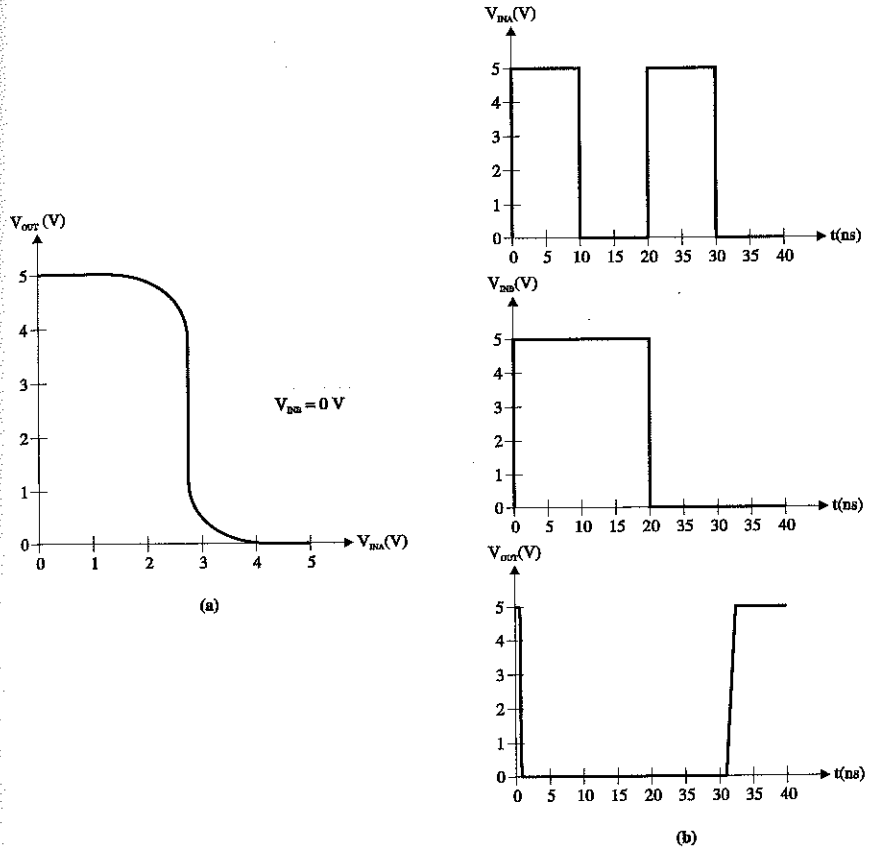


FIGURE 24.12 SPICE Simulation Results of Example 24.2: (a) Voltage transfer characteristic, (b) Transient response verifying realization of logical NOR function

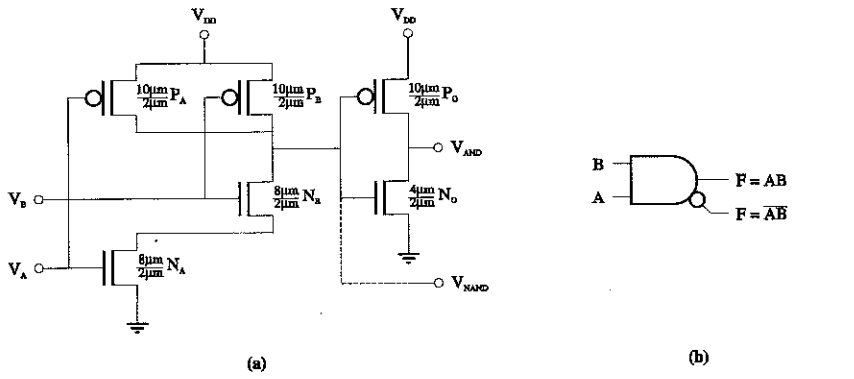


FIGURE 24.13 CMOS AND/NAND Gate: (a) NAND fed inverter, (b) Circuit symbol indicating both AND and NAND functions are available

V_C are both high. Alternately, an output pull-down path exists through N_B and N_D, if V_B and V_D are both high. Note that for the series combination of the N-channel MOSFETs N_A and N_C, there is the corresponding parallel combination of complementary P-channel MOSFETs P_A and P_C. Likewise, for the series combinations of NMOS transistors N_B and N_D, there is a corresponding parallel combination of complementary PMOS transistors P_B and P_D.

Output is NORing of the ANDings

As discussed earlier in this section, parallel combinations of the NMOS pull-down paths and series combinations of the complementary parallel PMOS pairs provides an ORing of the ANDing of inputs. As with all CMOS gates, the output is then naturally complemented and the ORing is in essence a NORing and the logic gate of Figure 24.17a does indeed realize the logic function

$$V_{OUT} = (V_A \text{ AND } V_C) \text{ NOR } (V_B \text{ AND } V_D)$$
$$= NOT[(V_A \text{ AND } V_C) \text{ OR } (V_B \text{ AND } V_D)]$$
$$= \overline{AC + BD}$$

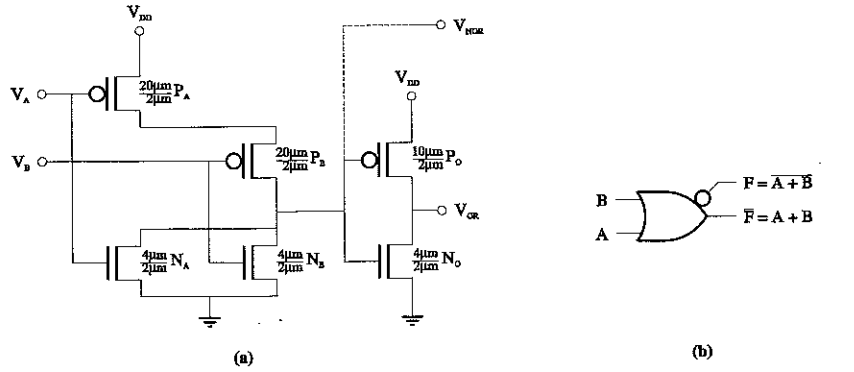


FIGURE 24.14 CMOS OR/NOR Gate: (a) NOR fed inverter, (b) Circuit symbol indicating both OR and NOR functions are available

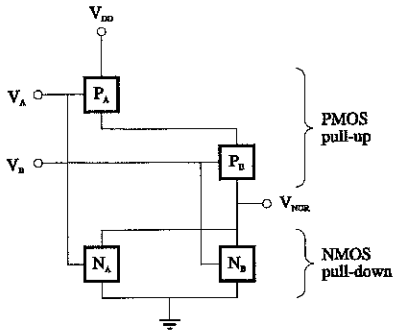


FIGURE 24.15 Block Diagram Representing Transistor Configuration of Two-input CMOS NOR Gate

Verification of AND-OR-Invert Logic Function

Table 24.3 is a detailed truth table for the four-input AOI circuit of Figure 24.17a. We shall now verify all combinations of low and high inputs as listed in Table 24.3 along with the states of all N- and P-channel MOSFETs. The ANDing of the individual pairs of inputs along with the expected output logic states are also included in Table 24.3.

Output Low State

V_A AND V_C High

As discussed previously in this section, an output pull-down path to ground exists through the channels of N_A and N_C if V_A and V_C are both high. With V_A and V_C high, P_A and P_C are both cutoff and no output pull-up path to V_{DD} is available. Thus, the circuit of Figure 24.17a is in the output low state for V_A AND V_C high. This verifies the output low state specified in lines 13 through 16 of Table 24.3.

V_B AND V_D High

Similarly, N_B and N_D are active when V_B and V_D are high and an active pull-down path to ground is available. With V_B and V_D high, P_B and P_D are cutoff and no output pull-up path to V_{DD} is present. Therefore, the circuit of Figure 24.17a is also in the output low state for V_B AND V_D high. Thus, the output low

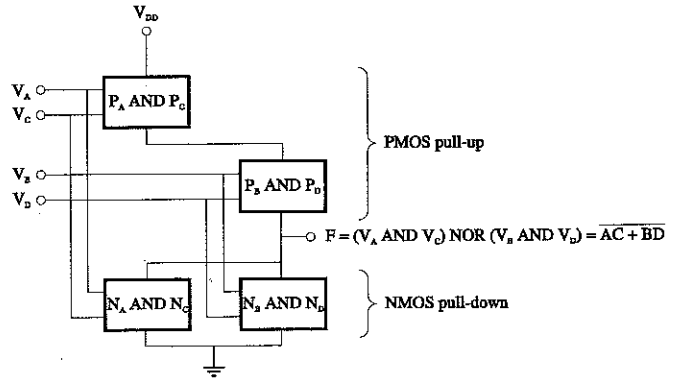


FIGURE 24.16 Block Diagram Representing NORing of Sub-logic Sections for an AND-OR-invert Logic Gate

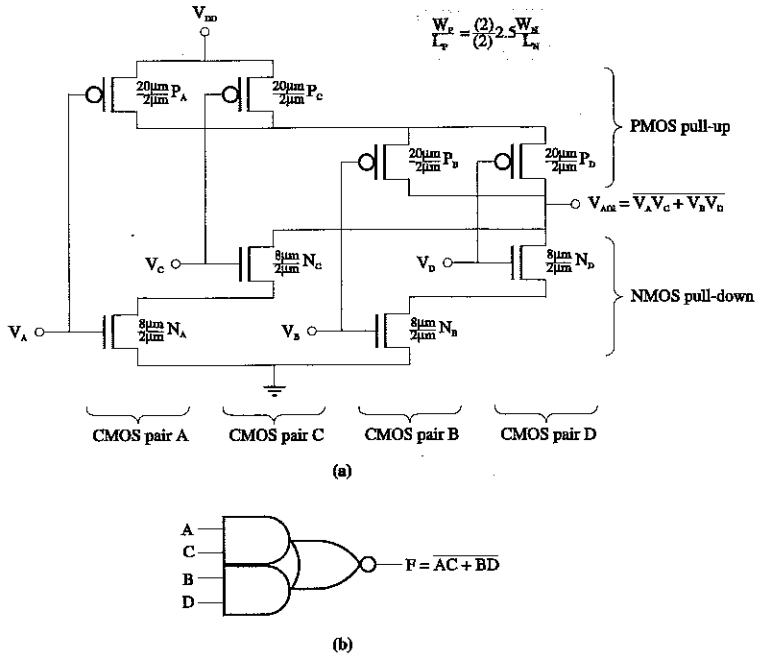


FIGURE 24.17 Four-input CMOS AND-OR-invert: (a) Circuit schematic, (b) Logic schematic

states tabulated in lines 4, 8, and 12 and again line 16 of Table 24.3 are verified.

Output Low Voltage = V_{OL}

With P_B and P_D cutoff, the sum of the PMOS drain currents $I_{D,PB}(off) + I_{D,PD}(off)$ is zero. Since the sum of the NMOS drain currents of N_C and N_D is equal to the sum of the PMOS drain currents, these are also zero. Hence,

$$I_{D,NC}(ON) + I_{D,ND}(ON) = I_{D,PB}(OFF) + I_{D,PD}(OFF) = 0$$

Since zero drain current active MOSFETs have a drain-to-source voltage of zero (as discussed in section 17.2), the NMOS transistors providing the output pull-down path to ground both have $V_{DS} = 0$. Thus, the output low voltage for the complex AOI logic gate of Figure 24.17a is the same as that for the CMOS inverter, NAND, and NOR gates with

$$V_{OL} = 0$$

This was the output low voltage found for the simpler CMOS NAND and NOR gates of the previous sections. V_{OL} is also zero for even more complex CMOS logic gates.

Output High State

V_A AND V_B Low

With V_A and V_B low, P_A and P_B are active and an output pull-up path to V_{DD} is available through their drain-to-source channels. Also, N_A and N_B are cutoff and no output pull-down path to ground is present. Thus, the complex CMOS logic gate of Figure 24.17a is in the output high state and lines 1, 2, 5, and 6 of Table 24.3 are verified.

TABLE 24.3 States of Each N-Channel and P-Channel MOSFET and Presence of Output Pull-Up and Pull-Down Paths in the Four Input CMOS AND-OR-Invert Gate of Figure 24.17a for All Combinations of Low and High Inputs

	V_A	V_C	V_B	V_D	N_A	N_C	N_B	N_D	P_A	P_C	P_B	P_D	V_A AND V_C	V_B AND V_D	Pull-Up Path	Pull-Down Path	$\frac{V_{OUT}}{V_{AOI}}$
1	low	low	low	low	off	off	off	off	on	on	on	on	low	low	yes	no	high
2	low	low	low	high	off	off	off	on	on	on	on	off	low	low	yes	no	high
3	low	low	high	low	off	off	on	off	on	on	off	on	low	low	yes	no	high
4	low	low	high	high	off	off	on	on	on	on	off	off	low	high	no	yes	low
5	low	high	low	low	off	on	off	off	on	off	on	on	low	low	yes	no	high
6	low	high	low	high	off	on	off	on	on	off	on	off	low	low	yes	no	high
7	low	high	high	low	off	on	on	off	on	off	off	on	low	low	yes	no	high
8	low	high	high	high	off	on	on	on	on	off	off	off	low	high	no	yes	low
9	high	low	low	low	on	off	off	off	off	on	on	on	low	low	yes	no	high
10	high	low	low	high	on	off	off	on	off	on	on	off	low	low	yes	no	high
11	high	low	high	low	on	off	on	off	off	on	off	on	low	low	yes	no	high
12	high	low	high	high	on	off	on	on	off	on	off	off	low	high	no	yes	low
13	high	high	low	low	on	on	off	off	off	off	on	on	high	low	no	yes	low
14	high	high	low	high	on	on	off	on	off	off	on	off	high	low	no	yes	low
15	high	high	high	low	on	on	on	off	off	off	off	on	high	low	no	yes	low
16	high	high	high	high	on	on	on	on	off	off	off	off	high	high	no	yes	low

V_A AND V_D Low

P_A and P_D are active for V_A and V_D low and an output pull-up path to V_{DD} is available through their drain-to-source channels. N_A and N_D are simultaneously cutoff and no output pull-down path to ground exists. Thus, the CMOS logic gate of Figure 24.17a is in the output high state and lines 1, 3, 5, and 7 of Table 24.3 are verified.

V_C AND V_B Low and V_C AND V_D Low

An analogous situation results from either V_C and V_B low verifying lines 1, 2, 9, and 10 of Table 24.3. Lines 1, 3, 9, and 11 of Table 24.3 are verified in the same manner for V_C and V_D low.

Output High Voltage = V_{OH}

With N_C and N_D cutoff, the sum of the NMOS drain currents is zero. With the output pull-up path to V_{DD} provided through the two complementary PMOS devices and equal drain currents of the cutoff NMOS devices given by

$$I_{D,NC}(ON) + I_{D,ND}(ON) = I_{D,PB}(OFF) + I_{D,PD}(OFF) = 0$$

The drain-to-source voltages of the (active) pull-up PMOS transistors are $V_{DS,Pi} = 0$. Thus, as with the CMOS inverter, NAND, and NOR gates, the output high voltage is

$$V_{OH} = V_{DD}$$

Pull-Up and Pull-Down Paths are Exclusive

As demonstrated with the CMOS inverter of the previous chapter and the CMOS NAND and NOR gates of the previous sections, static operation (all inputs held constant at V_{OL} and/or V_{OH}) of the CMOS AND-OR-invert gate of Figure 24.17a always provides either an output pull-up path to V_{DD} or an output pull-down path to ground. As with the previously discussed CMOS logic gates, output pull-

up and pull-down paths are never simultaneously available.

Channel Width/Length Ratios

The channel width/length ratios of the NMOS and PMOS transistors in a complex CMOS logic gate must be scaled. This accommodates for the relative mobilities of electrons and holes in silicon

$$\mu_N = 2.5\mu_P \quad \textit{(in silicon)}$$

and the relative lengths of the output pull-up paths to V_{DD} and pull-down paths to ground. The widths of the N-channel MOSFETs are simply those found for the inverter with the same desired VTC multiplied by the maximum number of NMOS transistors required for an output pull-down path to ground. That is, for the complex CMOS AOI gate of Figure 24.17a, the longest output pull-down path to ground is through the drain-to-source channels of two NMOS transistors. The W_N/L_N ratio should therefore be twice that found in a CMOS inverter with the same desired VTC.

The widths of the PMOS channels are scaled in a similar fashion. W_P/L_P should be equal to that found in an inverter with the same desired VTC multiplied by the maximum number of PMOS transistors required for an output pull-up path to V_{DD}. Examining the CMOS gate of Figure 24.17a, the longest pull-up path from the output to V_{DD} is through the drain-to-source channel of two PMOS devices. The W_P/L_P ratio should therefore be twice that found in a CMOS inverter with the same desired VTC.

The following example demonstrates sizing of MOSFETs for the complex CMOS AOI circuit of Figure 24.17a.

Example 24.3 ***Size of MOSFETs in a Complex CMOS Logic Circuit***

Design the channel widths and lengths of the complex CMOS logic circuit of Figure 24.17a so that it has the same VTC of the CMOS inverter of Example 23.2 (shown in Figure 23.3).

Solution As mentioned in this section, the longest output pull-down path to ground found in the CMOS logic gate of Figure 24.17a is through two NMOS channels. The W_N/L_N ratio should therefore be twice that of the inverter in Example 23.2. Keeping the same channel length yields

$$\left.\frac{W_N}{L_N}\right|_{AOI} = 2\left.\frac{W_N}{L_N}\right|_{inverter} = 2\frac{(4\mu)}{(2\mu)} = \frac{8\mu m}{2\mu m}$$

Also mentioned, the longest pull-up path to V_{DD} is through two PMOS drain-to-source channels. The W_P/L_P ratio should also be twice that of the inverter in Example 23.2. Keeping the same PMOS channel length yields

$$\left.\frac{W_P}{L_P}\right|_{AOI} = 2\left.\frac{W_P}{L_P}\right|_{inverter} = 2\frac{(10\mu)}{(2\mu)} = \frac{20\mu m}{2\mu m}$$

Non-Inverting AND-OR Gates

Non-inverting AND-OR gates are obtained in CMOS in the same fashion as NMOS AND and OR gates. Namely, by connecting an inverter at the output. Figure 24.18a shows the CMOS AND-OR-invert gate of Figure 24.17a with a CMOS inverter connected to the output. This new circuit performs the logic function

$$V_{OUT} = (V_A \textit{ AND } V_C) \textit{ OR } (V_B \textit{ AND } V_D)$$
$$= AC + BD$$

Thus, the inverted AOI output node can be used to drive gates other than the cascaded inverter to provide complementary logic signals.

Recipe for Other Complex CMOS Logic Gates

Additional multi-input complex logic gates can be constructed using CMOS obeying the following general design connections:

1. ANDing of signals is performed by series stacked combinations of NMOS transistors with complementing PMOS transistors in parallel.
2. ORing of signals is accomplished by parallel connection of NMOS devices with the complementing PMOS devices stacked in series.
3. The gate terminal of each NMOS transistor is tied to the gate terminal of the complementing PMOS transistor and used as a signal input.
4. ORing of ANDed signals is realized by parallel connection of the series NMOS devices and series connection of the complementing parallel PMOS devices.

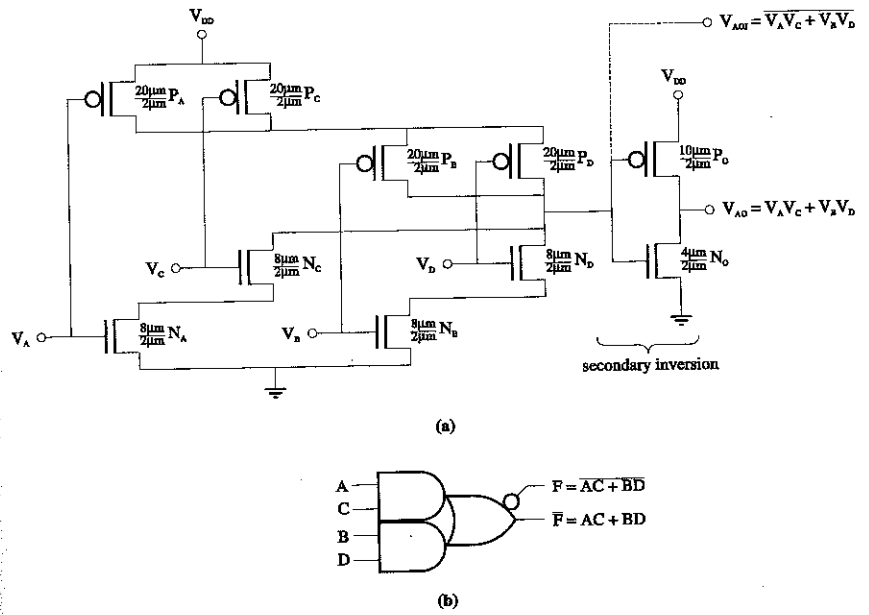


FIGURE 24.18 Four-input CMOS AND-OR gate: (a) Circuit with cascaded inverter, (b) Logic schematic

5. ANDing of ORed signals is realized by series connection of the parallel NMOS devices and parallel connection of the complementing series PMOS devices.
6. If a non-inverting AND-OR signal is desired, connect the output of the AND-OR-inverting circuitry to an inverter (the NOTed AND-OR node can be used to drive other logic gates).
7. A practical limitation for most CMOS digital integrated circuits is that no output pull-down path to ground or output pull-up path to V_{DD} should exceed traversing four MOSFETs.
8. The channel widths and lengths should be scaled as described earlier in this section.

When designing complex CMOS logic circuits, it is recommended that a corresponding truth table be verified for all combinations of low and high inputs. An output pull-up path to V_{DD} or output pull-down path to ground must be available for every combination of inputs and pull-up and pull-down paths should never be present simultaneously. Sketching block diagrams of the sub-logic sections provides a useful preliminary step in designing of complex CMOS logic circuits.

One final note should be made about the output voltage range. As with the CMOS inverter, NAND gate, and NOR gate, the output voltage operates *rail-to-rail*. That is, the output voltage varies from V_{OL} = ground = 0 to $V_{OH} = V_{DD}$.

Example 24.4 ***Complex CMOS OR-AND-Invert Logic Gate***

Design a five-input complex CMOS logic gate that provides the logic functions

$$F = \overline{(A + B)(C + D)E}$$

and

$$F = (A + B)(C + D)E$$

(Channel W/L ratios are calculated in the following example.)

Solution (Block Diagram) To design the five-input inverting logic section, note that the desired logic function is a NANDing of two ORings and an individual signal or

$$V_{OAI} = \overline{(V_A + V_B)(V_C + V_D)V_E}$$
$$= (V_A \; OR \; V_B) \; NAND \; (V_C \; OR \; V_D) \; NAND \; V_E$$

The overall NANDing of the sub-logic sections V_A OR V_B, V_C OR V_D, and V_E can be represented by the block diagram shown in Figure 24.19a. NANDing of signals requires series combinations of NMOS sections and parallel combinations of PMOS sections.

Solution (ORing Sub-logic) To perform the ORing logic V_A OR V_B and V_C OR V_D, the blocks in Figure 24.19a labeled N_A OR N_B and N_C OR N_D should be replaced with parallel combinations of NMOS transistors. The blocks labeled P_A OR P_B and P_C OR P_D should be replaced by series combinations of PMOS transistors.

Solution (Input E) The input for signal V_E is connected to a single N-channel MOSFET in place of the block labeled N_E and single P-channel MOSFET in place of the block labeled P_E.

Solution (Inverting) To provide the OR-ANDing of the non-inverting logic desired, a CMOS inverter should be connected to the output of the multi-input complex CMOS logic gate.

Figure 24.19b shows the CMOS circuit that provides the desired logic functions with each block of Figure 24.19a replaced with the constituent MOSFET representations and cascaded CMOS inverter to provide complementing of the initial logic function. As mentioned, the input node to the cascaded inverter may be used to drive other gates.

The truth table for this logic gate should be verified for all $2^5 = 32$ combinations of low and high inputs to verify proper logic realization. This is left as a homework exercise in Problem 24.40.

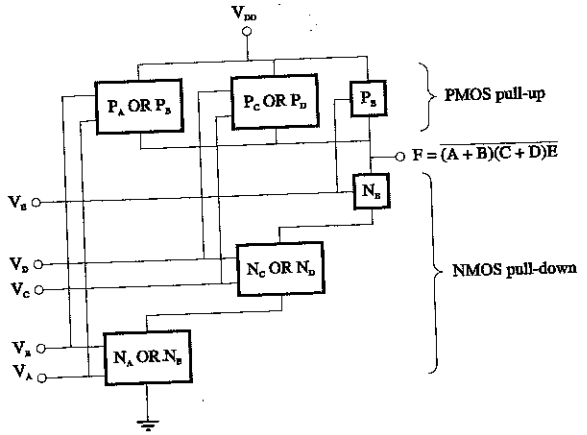


FIGURE 24.19 Five-input Complex CMOS OR-AND-invert/OR-AND Gate of Examples 24.4 and 24.5: (a) Block diagram representing NANDing of sub-logic sections

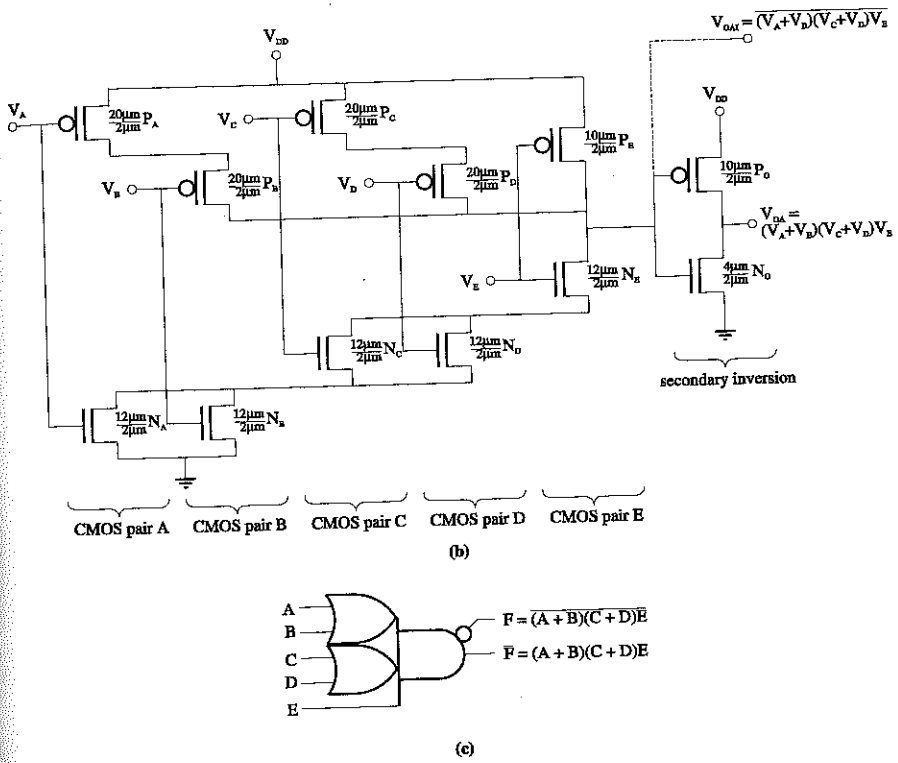


FIGURE 24.19 (continued) (b) Circuit schematic, (c) Logic schematic

Example 24.5 ***Complex CMOS Logic Gate Channel Width/Length Ratios***

Calculate the channel width/length W/L ratios for all MOSFETs in the logic gate of the previous example (Figure 24.19b). Both the multi-input and cascaded inverting stages should have the VTC and transient response of the CMOS inverter in Example 23.2.

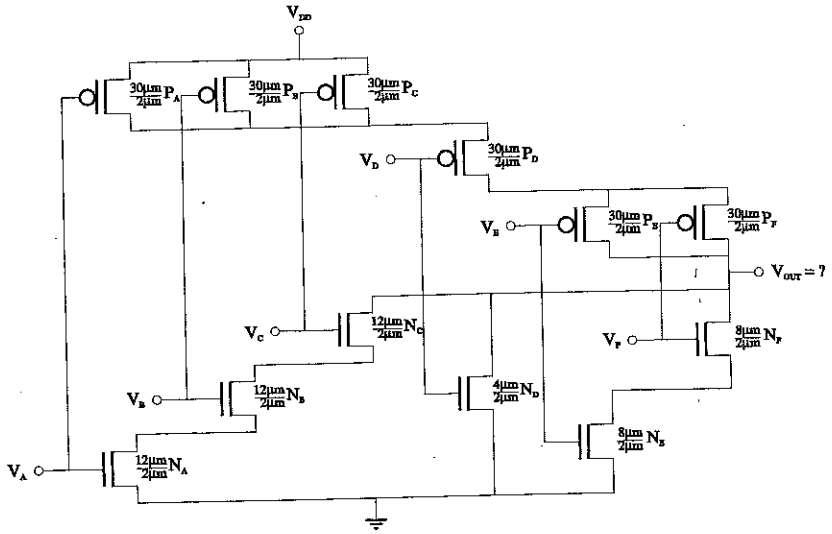
Solution (Second Inverter Stage) Since the two stages of the CMOS circuit of Figure 24.19b should have the same response as the inverter of Example 23.2, the inverter stage PMOS and NMOS have channel W/L ratios given by

$$\frac{W_{PI}}{L_{PI}} = \frac{10\mu m}{2\ \mu m}$$

and

$$\frac{W_{NI}}{L_{NI}} = \frac{4\ \mu m}{2\ \mu m}$$

Solution (NMOS W_N/L_N Ratios of Multi-input Stage) For the initial multi-input stage, all output



(a)

FIGURE 24.20 Six-input Complex CMOS AND-OR-invert Gate of Examples 24.6 and 24.7: (a) Circuit schematic

pull-down paths to ground are through three NMOS transistors. The W_N/L_N ratios should therefore be three times that of N_I or

$$\frac{W_N}{L_N}(A, B, C, D, E) = 3 \times \frac{W_{NI}}{L_{NI}} = 3 \times \frac{4\ \mu m}{2\ \mu m} = \frac{12\ \mu m}{2\ \mu m}$$

Solution (PMOS, W_P/L_P Ratios of Multi-Input Stage) Three output pull-up paths to V_{DD} are available. Two of the paths are through two PMOS transistors, P_A and P_B or P_C and P_D. Thus, the PMOS transistors P_A, P_B, P_C, and P_D should have W_P/L_P ratios twice that of P_I or

$$\frac{W_P}{L_P}(A, B, C, D) = 2 \times \frac{W_{PI}}{L_{PI}} = 2 \times \frac{10\ \mu m}{2\ \mu m} = \frac{20\ \mu m}{2\ \mu m}$$

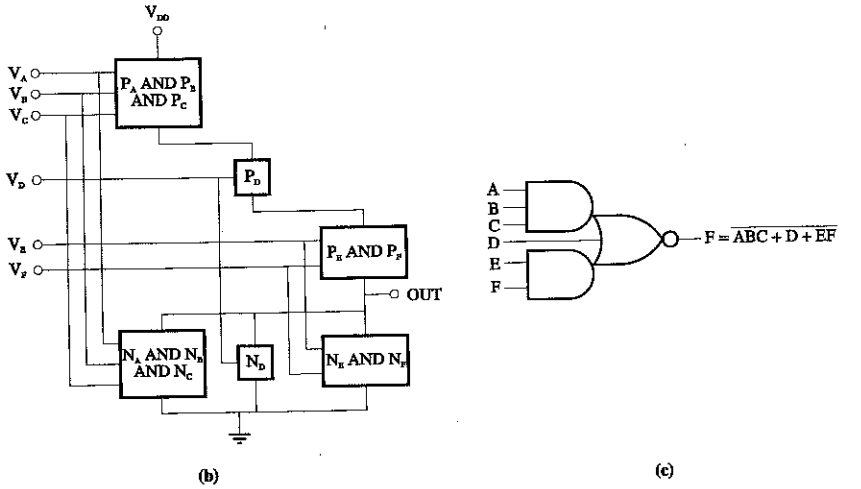
The third output pull-up path to V_{DD} is through the single transistor P_E. The W_P/L_P ratio need only be that of P_I and thus

$$\frac{W_{PE}}{L_{PE}} = \frac{W_{PI}}{L_{PI}} = \frac{10\ \mu m}{2\ \mu m}$$

The following two examples demonstrate the design of a complex CMOS AND-OR-invert logic gate. The channel width/length ratios are calculated in the secondary example.

Example 24.6 *Complex CMOS AND-OR-Invert Logic Gate*

What complex logic function is performed by the six-input CMOS logic gate of Figure 24.20a?



(b) (c)

FIGURE 24.20 (continued) (b) Block diagram, (c) Logic schematic

Solution (Block Diagram, NMOS Pull-Down Sections) Examining the complex CMOS logic gate of Figure 24.20a it is seen that three output pull-down paths to ground exist as follows: (1) through N_A, N_B, and N_C; (2) through N_D; and (3) through N_E and N_F. Figure 24.20b shows a block diagram of this complex CMOS logic gate with a separate block dedicated to each NMOS pull-down path. As noted in this and previous sections, series connection of NMOS devices performs an ANDing of signals. Thus, the blocks representing the first and third pull-down path are labeled N_A AND N_B AND N_C and N_E AND N_F. The block representing the pull-down of the single transistor is labeled N_D.

Solution (Block Diagram, PMOS Pull-Up Sections) Further examining Figure 24.20a, note the PMOS output pull-up path to V_{DD} is in three stages: (1) P_A, P_B, and P_C; (2) P_D; and (3) P_E and P_F. The P-channel MOSFETs of each pull-up stage correspond to the N-channel MOSFETs of each pull-down path. The block diagram of Figure 24.20b also includes blocks representing each PMOS pull-up stage. Since parallel combinations of P-channel MOSFETs represent ANDing of signals, the block of Figure 24.20b representing the PMOS pull-up stage closest to V_{DD} is labeled P_A AND P_B AND P_C. Similarly, the block representing the pull-up stage closest to the output is labeled P_E AND P_F. The block representing the single transistor pull-up stage is labeled P_D.

Solution (NORing of ANDing) Examining the block diagram of Figure 24.20b, the pull-down paths are in parallel and a corresponding PMOS pull-up stage is present in a series pull-up. Corresponding blocks in the pull-down and pull-up paths perform the same logic function. Hence, the logic gate of Figure 24.20a performs a NORing of the individual sub-logic sections. Since each section is either an ANDing or a single signal, this gate performs the logic function

$$F = (A\ AND\ B\ AND\ C)\ NOR\ D\ NOR\ (E\ AND\ F)$$
$$= NOT[(A\ AND\ B\ AND\ C)\ OR\ D\ OR\ (E\ AND\ F)]$$
$$= \overline{ABC + D + EF}$$

Figure 24.20c shows the symbolic representation of this logic function. Constructing a truth table for all

combinations ($2^6 = 64$) of low and high input states and corresponding outputs would provide complete confirmation of the logic gate output function.

Example 24.7 *Complex CMOS Logic Gate Channel Width/Length Ratios*

Calculate the channel width/length W/L ratios for all MOSFETs in the logic gate of the previous example (Figure 24.20a). Both the multi-input and cascaded inverting stages should have the VTC and transient response of the CMOS inverter in Example 23.2.

Solution (NMOS W_N/L_N Ratios) The channel width/length ratio for the NMOS transistor of the CMOS inverter in Example 23.2 was found to be $W_{NI}/L_{NI} = 4\mu m/2\mu m$. The complex CMOS logic gate of Figure 24.20a has three NMOS pull-down paths. The first pull-down path is through the three NMOS transistors N_A, N_B, and N_C. The N-channel MOSFETs N_A, N_B, and N_C should therefore have W_N/L_N ratios three times that of the NMOS device in Example 23.2:

$$\frac{W_N}{L_N}(A, B, C) = 3 \times \frac{W_{NI}}{L_{NI}} = 3 \times \frac{4\ \mu m}{2\ \mu m} = \frac{12\ \mu m}{2\ \mu m}$$

Since N_D is a single transistor pull-down path, the W_N/L_N ratio is the same as that in the inverter of Example 23.2 given by

$$\frac{W_{ND}}{L_{ND}} = \frac{W_{NI}}{L_{NI}} = \frac{4\ \mu m}{2\ \mu m}$$

The third pull-down path consists of the two NMOS transistors N_E and N_F. The W_N/L_N ratio for N_E and N_F should therefore be twice that of the Example 23.2 inverter and thus

$$\frac{W_N}{L_N}(E, F) = 2 \times \frac{W_{NI}}{L_{NI}} = 2 \times \frac{4\ \mu m}{2\ \mu m} = \frac{8\ \mu m}{2\ \mu m}$$

Solution (PMOS W_P/L_P Ratios) The channel width/length ratio for the PMOS transistor of the CMOS inverter in Example 23.2 was found to be $W_{PI}/L_{PI} = 10\mu m/2\mu m$. Examining Figure 24.20a, all output pull-up paths to V_{DD} are through a series combination of three P-channel MOSFETs. Thus, all PMOS devices in the complex CMOS logic gate of Figure 24.20a should have channel W_P/L_P ratios three times that of the inverter in Example 23.2 and thus

$$\frac{W_P}{L_P}(A, B, C, D, E, F) = 3 \times \frac{W_{PI}}{L_{PI}} = 3 \times \frac{10\ \mu m}{2\ \mu m} = \frac{30\ \mu m}{2\ \mu m}$$

CMOS logic gates can be even more complex than those shown previously. The following example describes a more complex gate.

Example 24.8 *Super Complex CMOS Logic Gate*

Determine the logic function performed by the eight-input complex CMOS logic gate shown in Figure 24.21a.

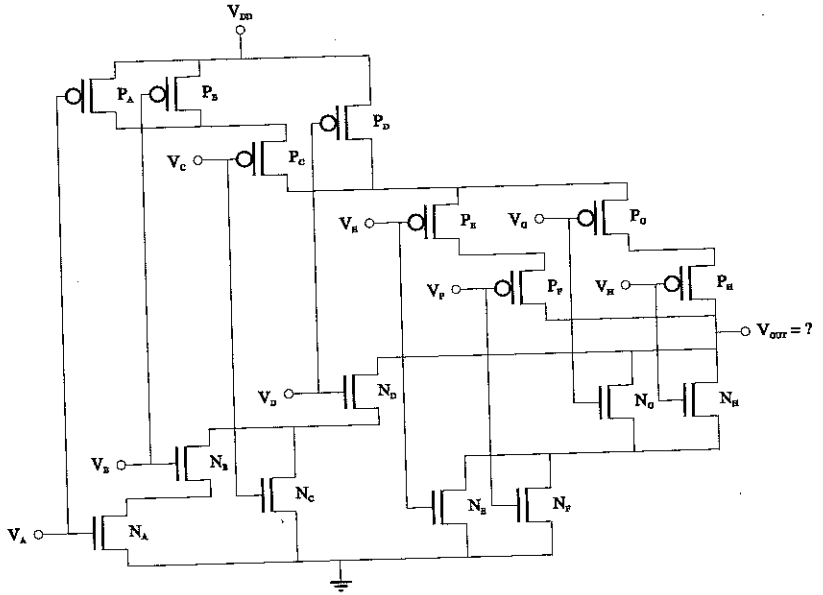
Solution (Block Diagram) Examining the logic gate of Figure 24.21a, note that two NMOS output pull-down paths to ground are present: (1) through the N_A, N_B, N_C, and N_D configurations, and (2) through the N_E, N_F, N_G, and N_H configurations. Also, the PMOS output pull-up path to V_{DD} is in two major sections: (1) through the P_A, P_B, P_C, and P_D configurations, and (2) through the P_E, P_F, P_G, and P_H configurations. The block diagram of Figure 24.21b illustrates this configuration. Parallel configurations of pull-down paths and series configurations of pull-up sections imply an overall NORing of the sub-logic sections.

Solution (Left Pull-Down Path) The NMOS pull-down path in Figure 24.21a consisting of N_A, N_B, N_C, and N_D will be considered first. The transistors N_A and N_B are in series, realizing the NMOS pull-down logic **A AND B**. The series N_A-N_B MOSFETs are in parallel with N_C, thus achieving the logic **(A AND B) OR C**. Finally, the N_A-N_B-N_C configuration is in series with the NMOS device N_D denoting an ANDing. The N_A, N_B, N_C, and N_D NMOS section thus realizes the NMOS pull-down logic **[(A AND B) OR C] AND D**.

Solution (Upper Pull-Up Section) The P-channel MOSFETs in Figure 24.21a for the PMOS pull-up section closest to V_{DD} are connected to the N-channel MOSFETs of the NMOS pull-down path on the left side of the gate schematic. This PMOS pull-up section should therefore realize the same logic calculated in the previous solution sub-section.

The PMOS devices P_A and P_B are in parallel and therefore perform the logic **A AND B**. The parallel P_A-P_B section is in series with P_C achieving the logic **[(A AND B) OR C]**. Finally, the P_A-P_B-P_C configuration is in parallel with the P-channel MOSFET P_D. Thus, the top PMOS pull-up section does indeed realize the same logic **[(A AND B) OR C] AND D** performed by the corresponding NMOS pull-down path.

Solution (Right Pull-Down Path) The NMOS pull-down path of Figure 24.21a including N_E, N_F, N_G, and N_H is made up of two parallel N-channel MOSFET sections in series. This NMOS configuration realizes the logic **(E OR F) AND (G OR H)**.



(a)

FIGURE 24.21 Eight-input Super-Complex CMOS Logic Gate of Example 24.8: **(a)** Circuit schematic

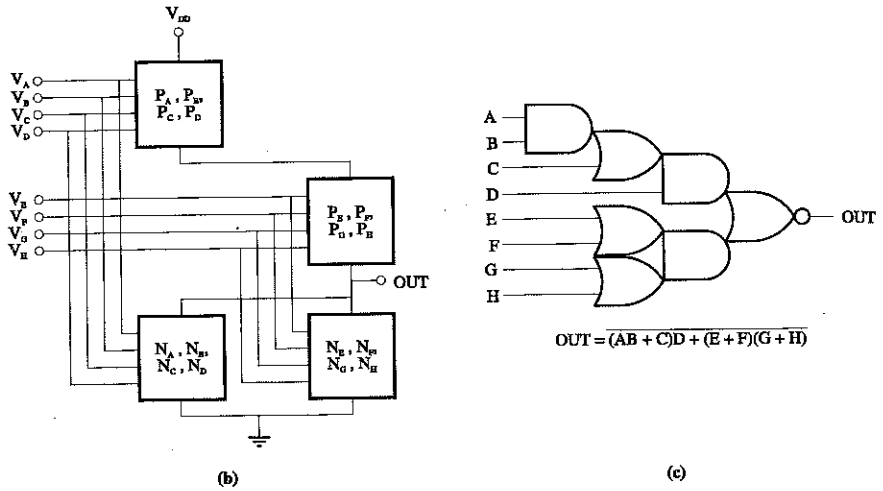


FIGURE 24.21 (continued) (b) First level block diagram: NORing, (c) Logic schematic

Solution (Lower Pull-Up Section) The PMOS pull-up section consisting of P_E, P_F, P_G, and P_H is a parallel combination of series P-channel MOSFETs. This realizes the same logic (E OR F) AND (G OR H) performed by the corresponding NMOS pull-down path.

Solution (NORing of Sub-Logic Sections) The previous solution sub-sections showed that the two PMOS pull-up sections realize the same logic as the complementing NMOS pull-down paths. Since the NMOS pull-down paths and PMOS pull-up sections are in an overall NORing configuration, the logic function provided by the complex CMOS logic gate of Figure 24.21 is

$$\begin{aligned} F &= \{[(A \text{ AND } B] \text{ OR } C)] \text{ AND } D\} \\ &\quad NOR\ [(E \text{ OR } F) \text{ AND } (G \text{ OR } H)] \\ &= NOT(([[A \text{ AND } B] \text{ OR } C)] \text{ AND } D\} \\ &\quad OR\ [(E \text{ OR } F) \text{ AND } (G \text{ OR } H)]) \\ &= \overline{(AB + C)D + (E + F)(G + H)} \end{aligned}$$

This logic function is shown symbolically in Figure 24.21c. Constructing a truth table for all ($2^8 = 256$) combinations of low and high inputs and their corresponding outputs would prove a formidable task but would also provide complete verification of this logic expression.

Tips, Tricks, and Gimmicks

De Morgan's Theorems

De Morgan's theorems will be needed in the following section. They can be stated simply as follows:

De Morgan's NOR Theorem:

$$\overline{W + Y} = \overline{W}\,\overline{Y}$$

De Morgan's NAND Theorem:

$$\overline{WY} = \overline{W} + \overline{Y}$$

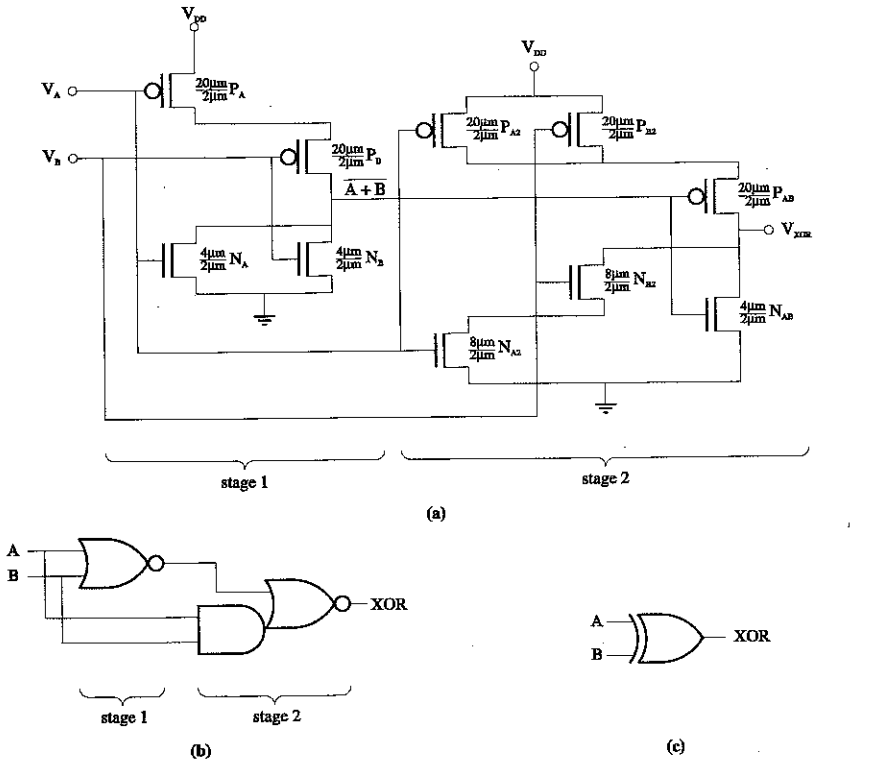


FIGURE 24.22 XOR Gate: (a) CMOS two-stage combinational logic realization, (b) Logic embodiment, (c) Circuit symbol

24.6 CMOS XOR/XNOR GATES

Two Stage Circuit

Exclusive OR (XOR) and exclusive NOR (XNOR) gates can not be constructed in any clever way similar to the NMOS XOR gate discussed in section 22.5. The design of a CMOS XOR gate through combinational logic realization results in the two stage CMOS gate shown in Figure 24.22a. The two stages of this circuit are a two-input CMOS NOR gate ($\overline{A\ \ B}$) and a three-input CMOS AOI performing the logic function $\overline{AB\ \ C}$. The logic output $\overline{A\ \ B}$ of the first stage is fed into the C input of the AOI giving an output logic function

$$F = \overline{AB + \overline{A + B}}$$

The logic circuit is shown symbolically in Figure 24.22b. To show that this is in fact the XOR function, we apply De Morgan's NOR theorem to the $\overline{A + B}$ term to obtain

$$F = \overline{AB + \overline{A}\,\overline{B}} = A \text{ XOR } B$$