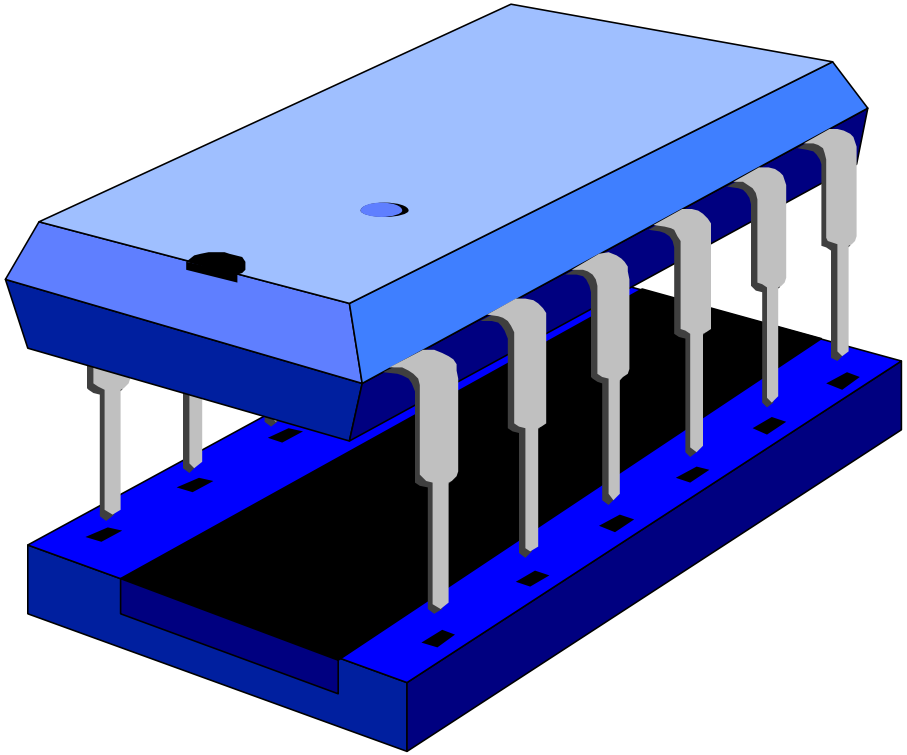
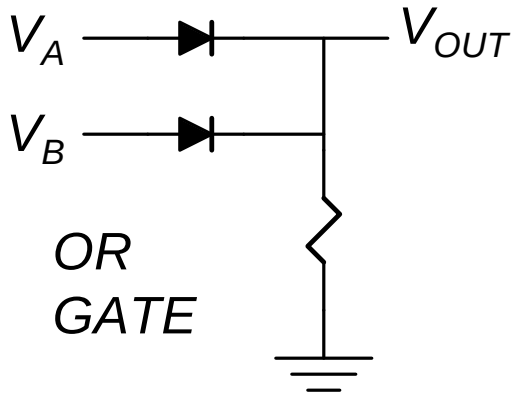
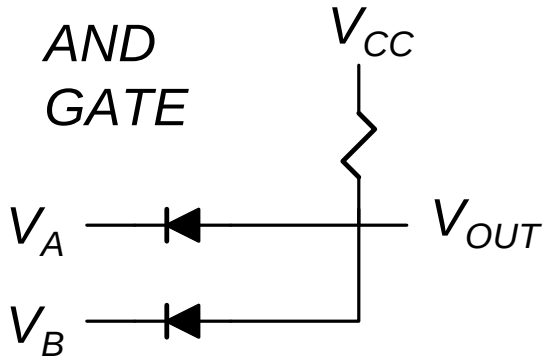
Diode-Transistor Logic (DTL)



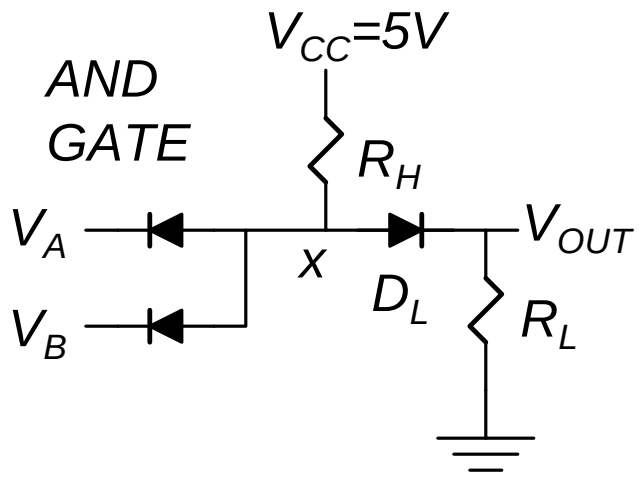
Diode Logic





- *Diode Logic suffers from voltage degradation from one stage to the next.*
- *Diode Logic only permits the OR and AND functions.*
- *Diode Logic is used extensively but not in integrated circuits!*

Level-Shifted Diode Logic



With either input at 0V, V_X=0.7V, D_L is just cut off, and V_{OUT}=0V.

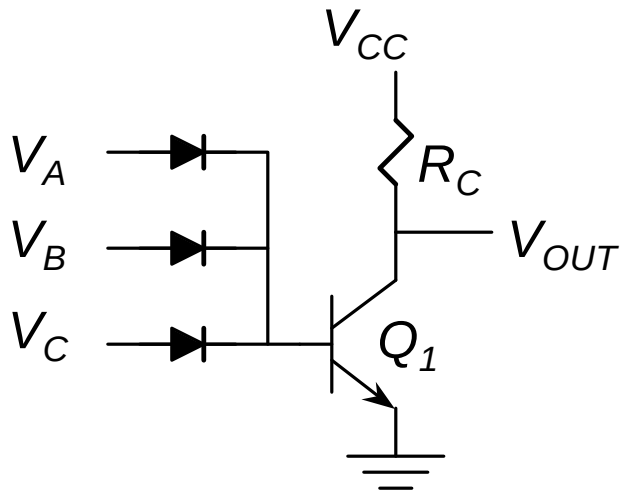
With both inputs at 1V, V_X=1.7V and V_{OUT}=1V.

With V_A=V_B=5V, both input diodes are cut off. Then

$$V_{OUT} = R_L\left(\frac{V_{CC} - 0.7V}{R_H + R_L}\right)$$

- *Level shifting eliminates the voltage degradation from the input to the ouput. However,*
- *the logic swing falls short of rail-to-rail, and*
- *the inverting function still is not available without using a transistor!*

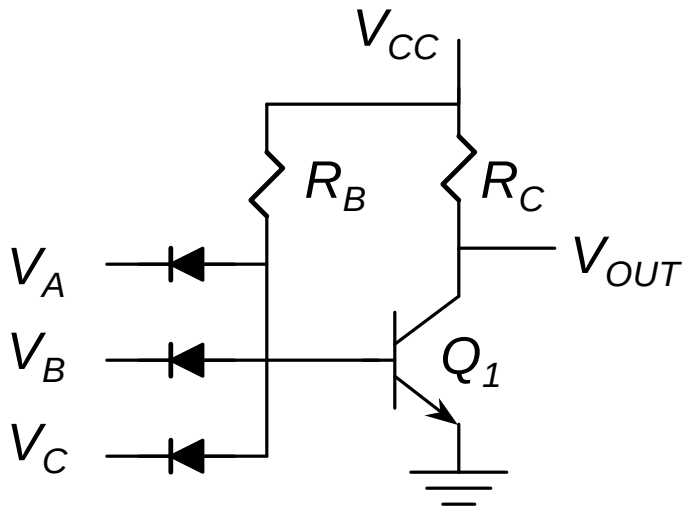
Diode-Transistor Logic (DTL)



Primitive Precursor to DTL

- *If any input goes high, the transistor saturates and V_{OUT} goes low.*
- *If all inputs are low, the transistor cuts off and V_{OUT} goes high.*
- *This is a NOR gate.*
- *"Current Hogging" is a problem because the bipolar transistors can not be matched precisely.*

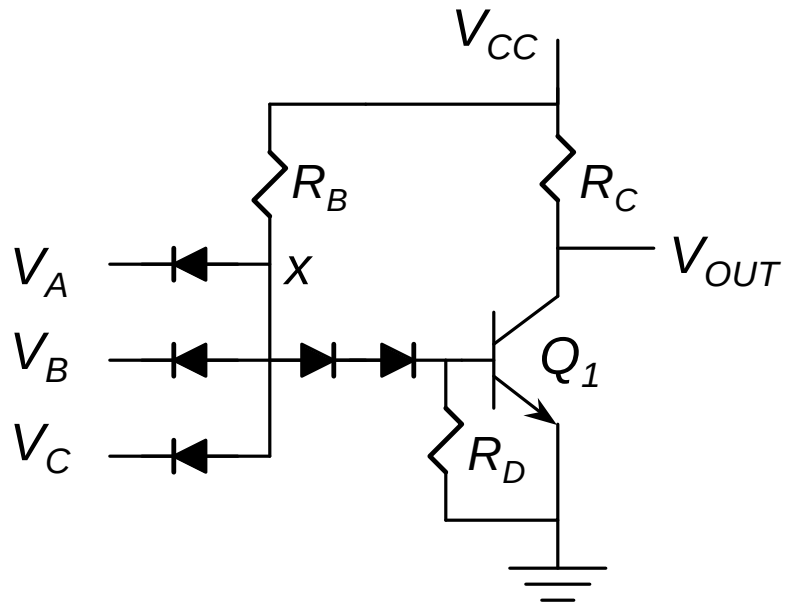
Diode-Transistor Logic (DTL)



Improved gate with reversed diodes.

- *If all inputs are high, the transistor saturates and V_{OUT} goes low.*
- *If any input goes low, the base current is diverted out through the input diode. The transistor cuts off and V_{OUT} goes high.*
- *This is a NAND gate.*
- *The gate works <u>marginally</u> because $V_D = V_{BEA} = 0.7V$.*

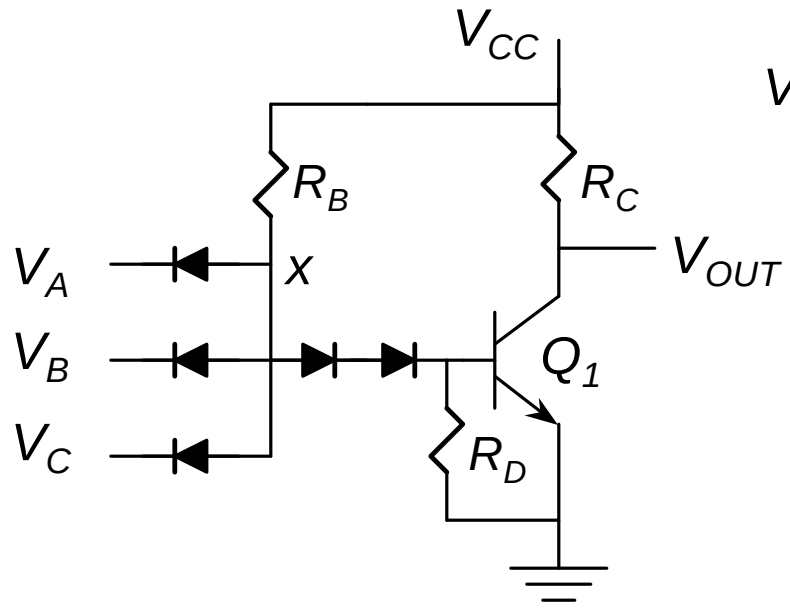
Diode-Transistor Logic (DTL)

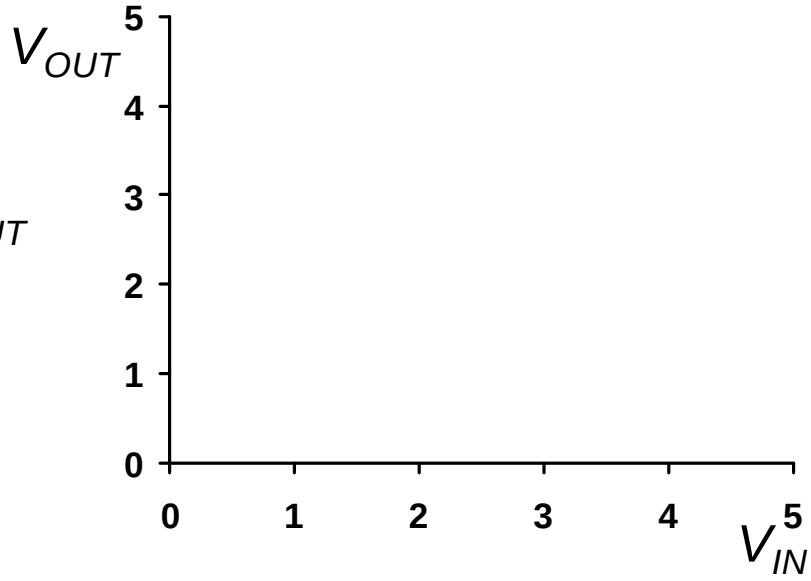


Basic DTL NAND gate.

- *If all inputs are high, V_x = 2.2V and the transistor is saturated.*
- *If any input goes low (0.2V), V_x=0.9V, and the transistor cuts off.*
- *The added resistor R_D provides a discharge path for stored base charge in the BJT, to provide a reasonable t_{PLH}.*

DTL VTC





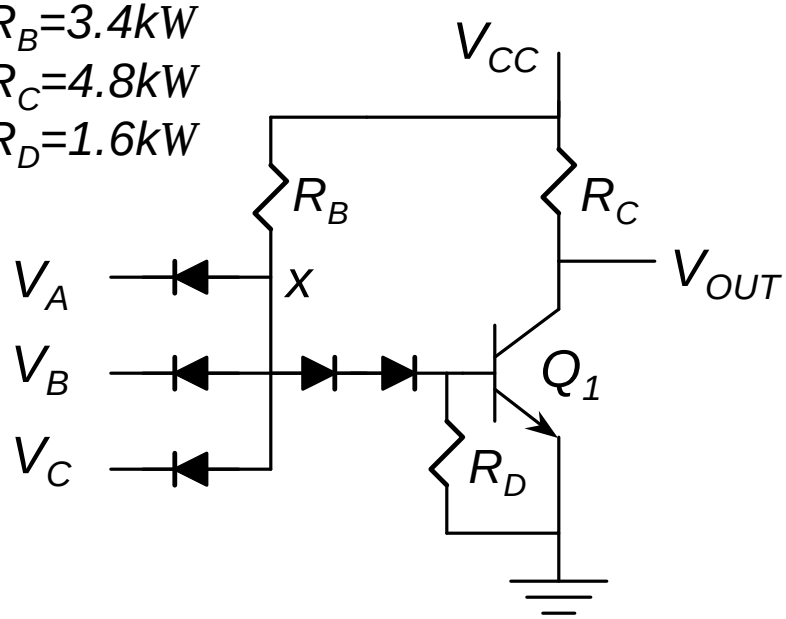
$V_{OH} =$ $V_{IL} =$

$V_{OL} =$ $V_{IH} =$

- *The noise margins are more symmetric than in the RTL case.*

DTL Power Dissipation

R_B=3.4kW
R_C=4.8kW
R_D=1.6kW



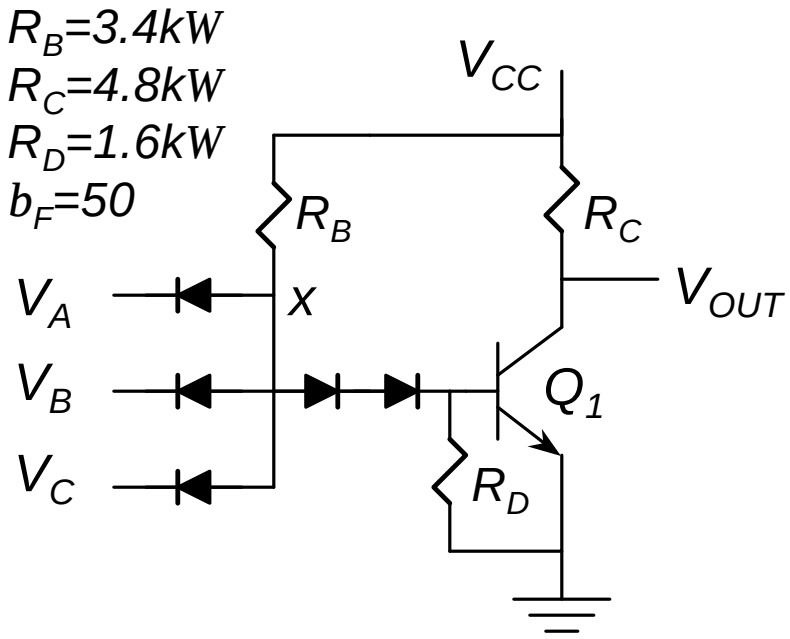
$$P_L =$$

$$P_H =$$

- *Scaling R_B and R_C involves a direct tradeoff between speed and power.*

$$P =$$

DTL Fanout



$I_{CS} =$

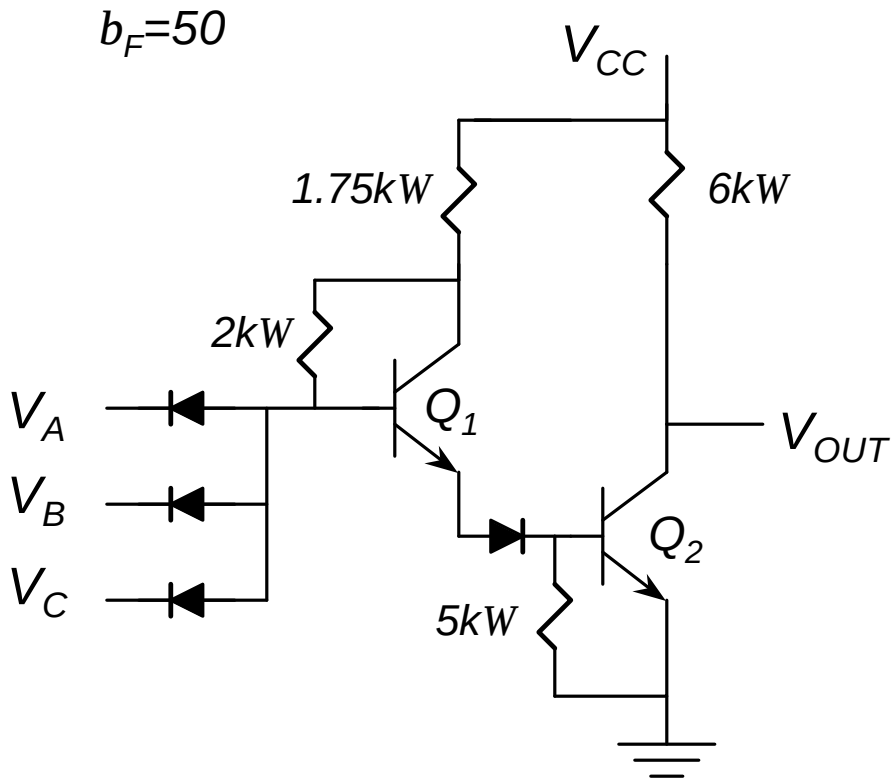
$I_{BS} =$

$I_{CS} =$

$N_{\max} =$

- *Good fanout requires high b_F, large R_D/R_B.*

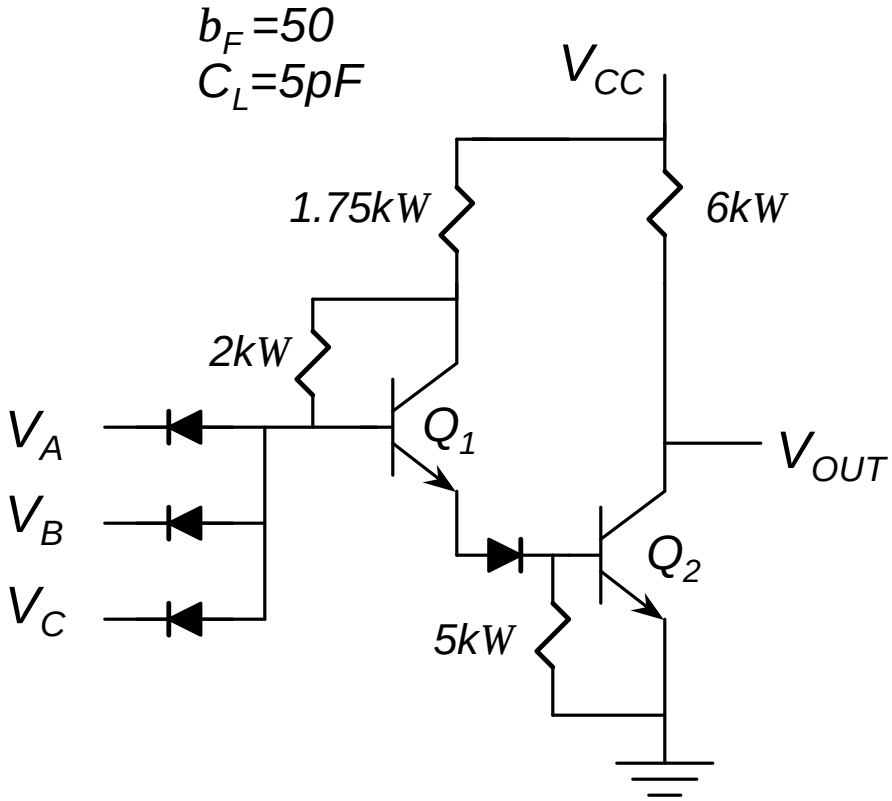
930 Series DTL (ca 1964 A.D.)



- *One of the series diodes is replaced by Q_1, providing more base drive for Q_2 and improving the fanout (N_{max} = 45).*
- *Does Q_1 saturate?*

930 DTL Characteristics	
V_{OH} / V_{OL}	5.0V / 0.2V
V_{IH} / V_{IL}	1.5V / 1.4V
Fanout	45
Dissipation	10mW
t_P	75ns

930 DTL Propagation Delays

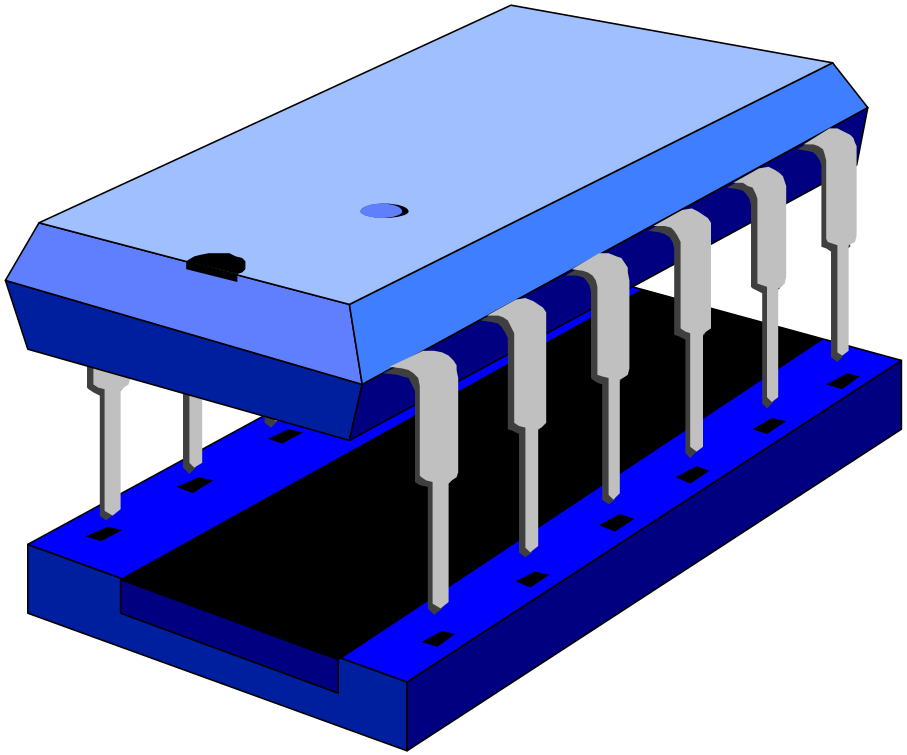


- $t_{PLH} >> t_{PHL}$
- $t_{PLH} = t_S + t_r/2$

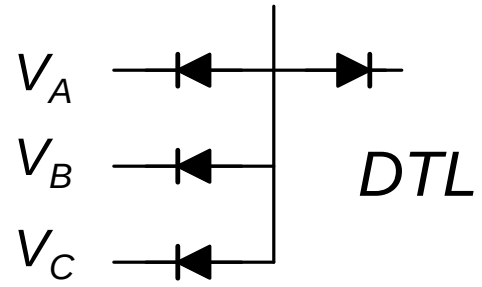
$t_s =$

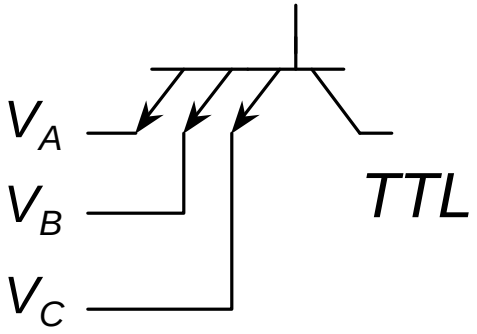
$t_r \approx$

Transistor-Transistor Logic (TTL)



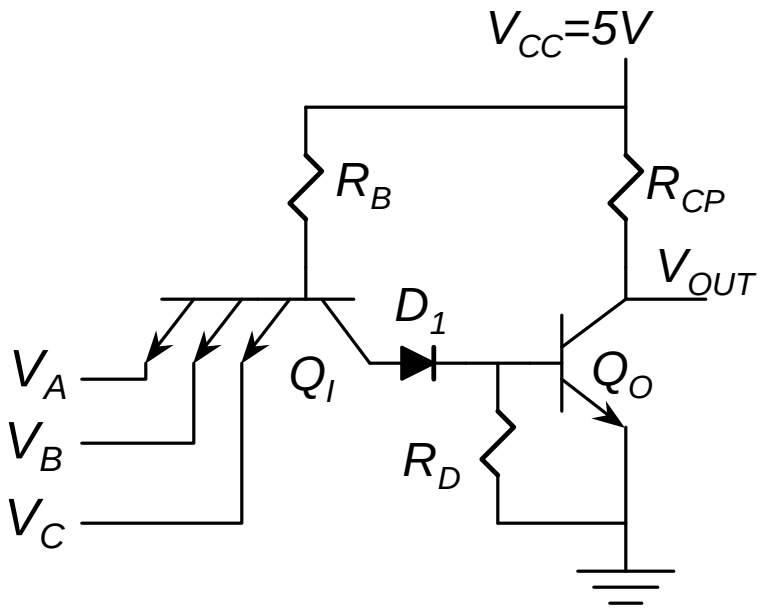
Why TTL?





- *The DTL input uses a number of diodes which take up considerable chip area.*
- *In TTL, a single multi-emitter BJT replaces the input diodes, resulting in a more area-efficient design.*
- *DTL was ousted by faster TTL gates by 1974.*

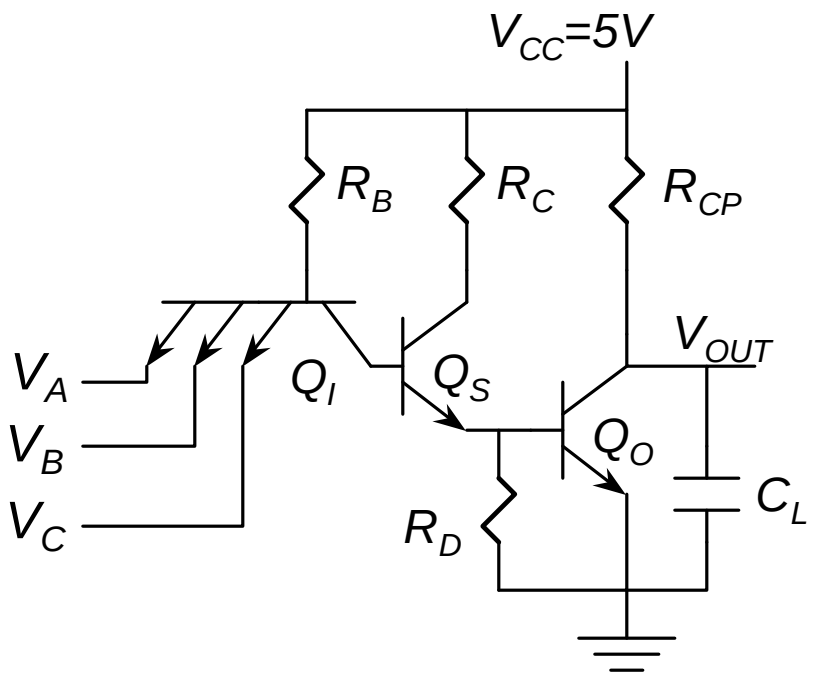
Basic TTL NAND Gate.



- *ALL INPUTS HIGH.*
  - *Q_I is reverse active.*
  - *Q_O is saturated.*
  - *$V_{OL} = V_{CES}$*
- *ANY INPUT LOW.*
  - *Q_I is saturated.*
  - *Q_O is cut off.*
  - *$V_{OH} = V_{CC}$*

<u>Multi-emitter transistor.</u> Forward-biased emitter base junctions override reverse-biased junctions in determining the base and collector currents.

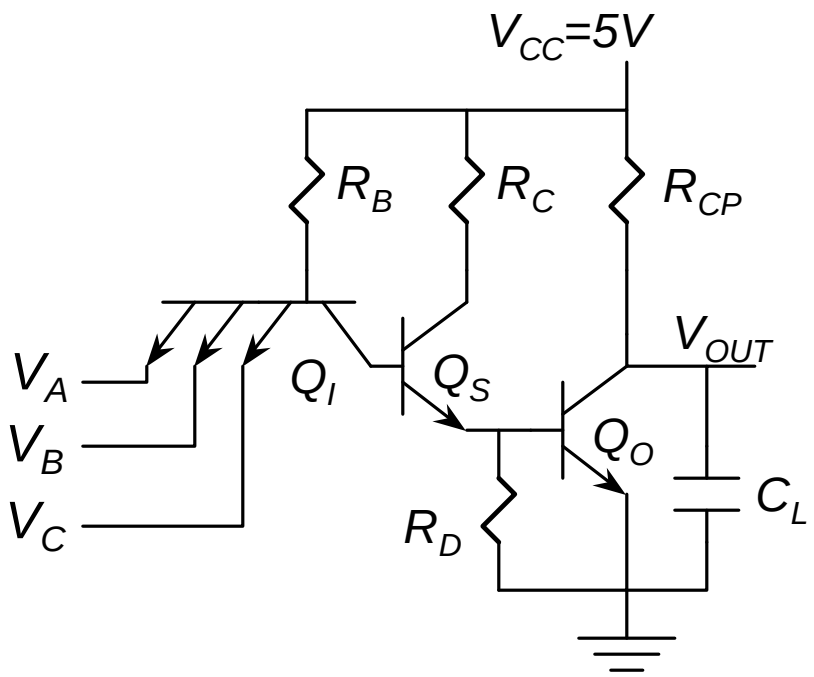
TTL Switching Speed: t_{PLH}



- *The depletion capacitance of the Q_I EB junction must discharge;*
- *Base charge must be removed from the saturated Q_S;*
- *Ditto for Q_O; and*
- *The capactive load must be charged to V_{CC}.*

<u>Multi-emitter transistor.</u> Forward-biased emitter base junctions override reverse-biased junctions in determining the base and collector currents.

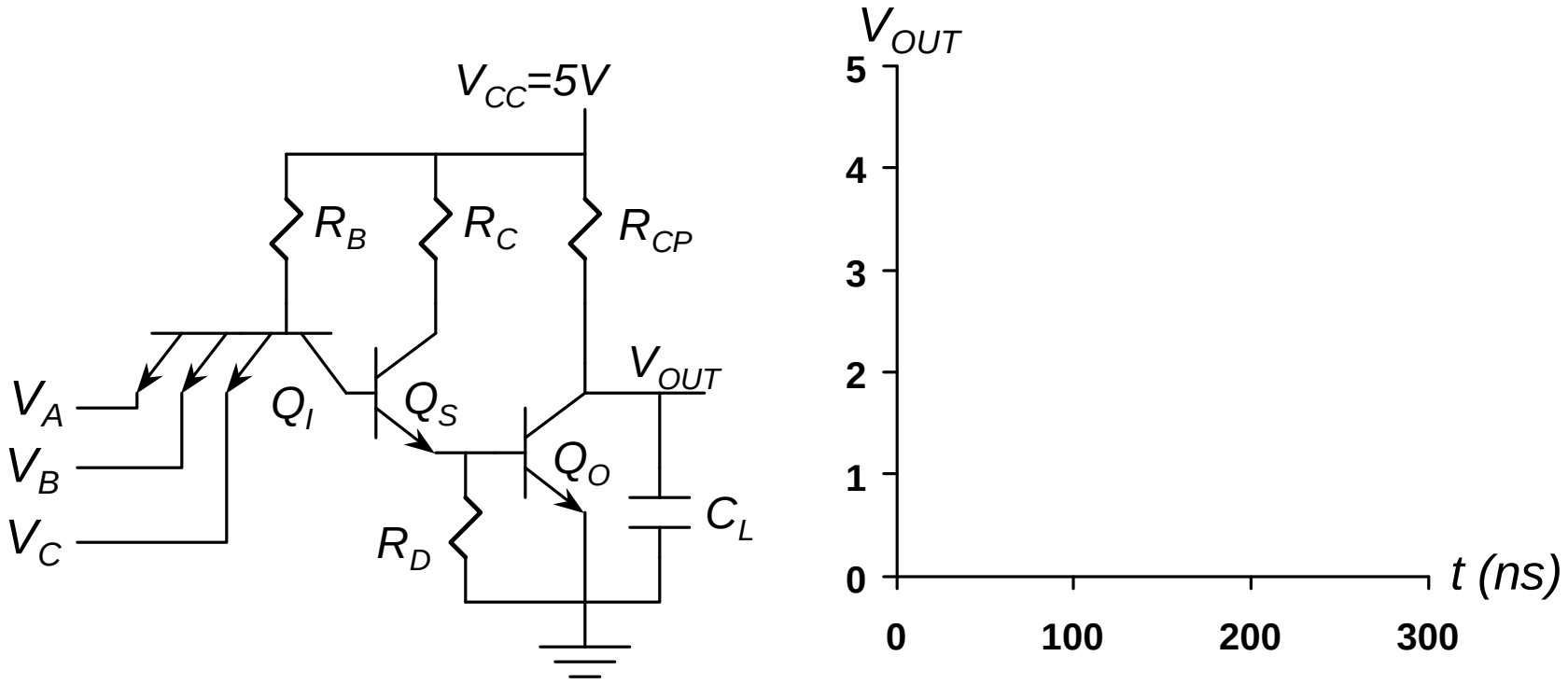
TTL Switching Speed: t_{PLH}



- *The time required to discharge the Q_I depletion layers is << 1ns.*
- *The time required to extract the Q_S base charge is also << 1ns:*
  - *Q_I becomes forward active;*
  - *$|I_{BR}|$ becomes large for Q_S*

- *Removal of base charge from Q_O is similar to the DTL case. With R_D = 1 kW, t_s = 10ns (these are typical values for 7400 series TTL).*

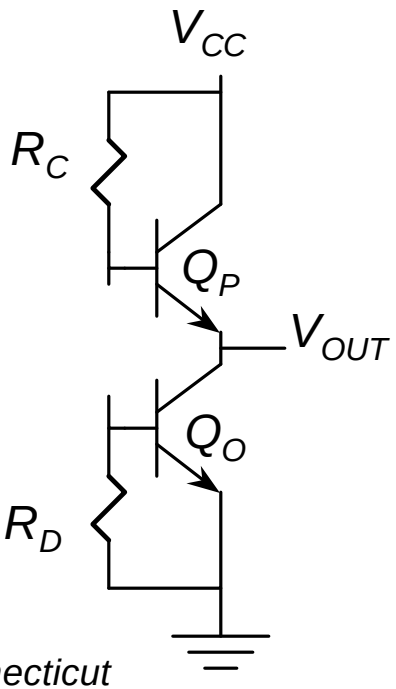
TTL Switching Speed: t_{PLH}



- *Charging of the capacitive load can be slow with "passive pullup." e.g., with a 5kΩ pull-up resistor and a 15 pF load (ten TTL gates) RC = 75 ns and t_r = 2.3RC = 173 ns!*

TTL with Active Pullup

- *In the previous example, the dominant switching speed limitation was the charging of capacitive loads through the pullup resistor.*
- *A small pullup resistance will improve the switching speed but will also increase the power and reduce the fanout.*

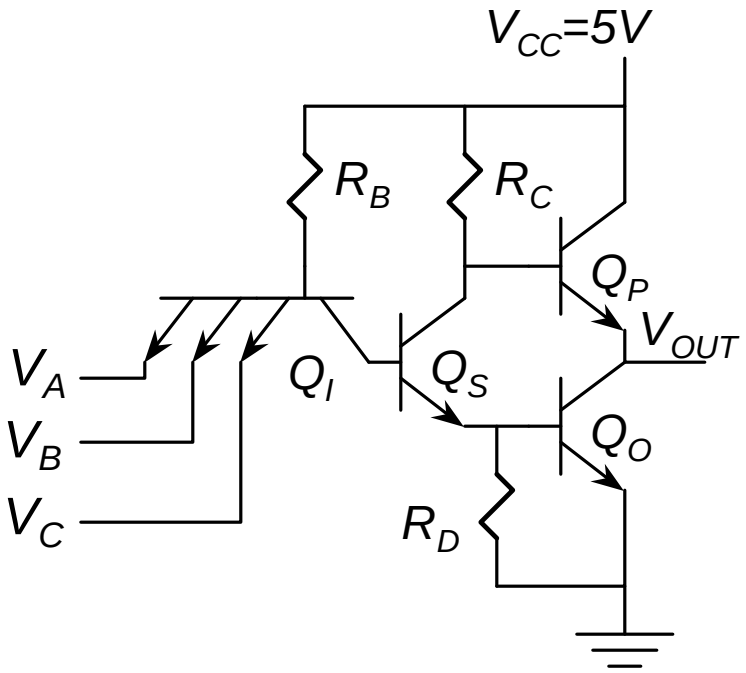


With active pullup, we can achieve the best of both worlds:

- *When the output is low, Q_P is cutoff, minimizing the power and maximizing the fanout;*
- *when the output goes high, Q_P becomes forward active to provide maximum drive current for a quick rise time.*

TTL with Active Pullup

- *With a high output,*
  - Q_S *is cutoff*
  - Q_P *is forward active*
- *With a low output,*
  - Q_S *is saturated*
  - Q_P *should be cutoff*



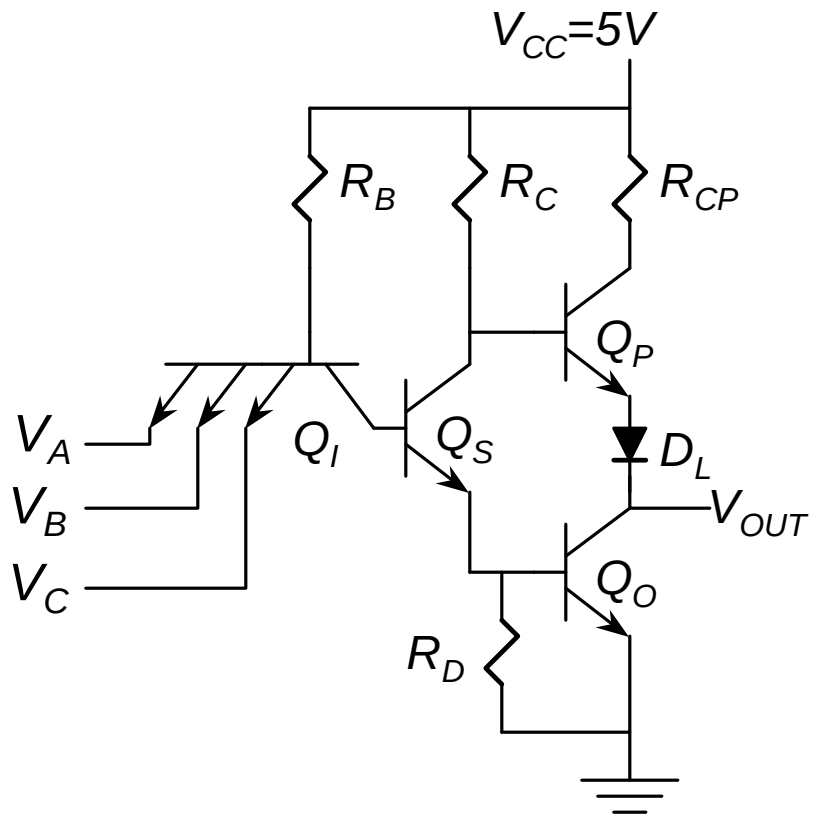
The low output case is unsatisfactory with this circuit:

V_{BP} = V_{EP} =

V_{BEP} =

The "Totem Pole Output" solves this problem.

TTL with "Totem Pole Output"



- *During turn-off, Q_S switches off before Q_O.*
- *Q_P begins to conduct when*

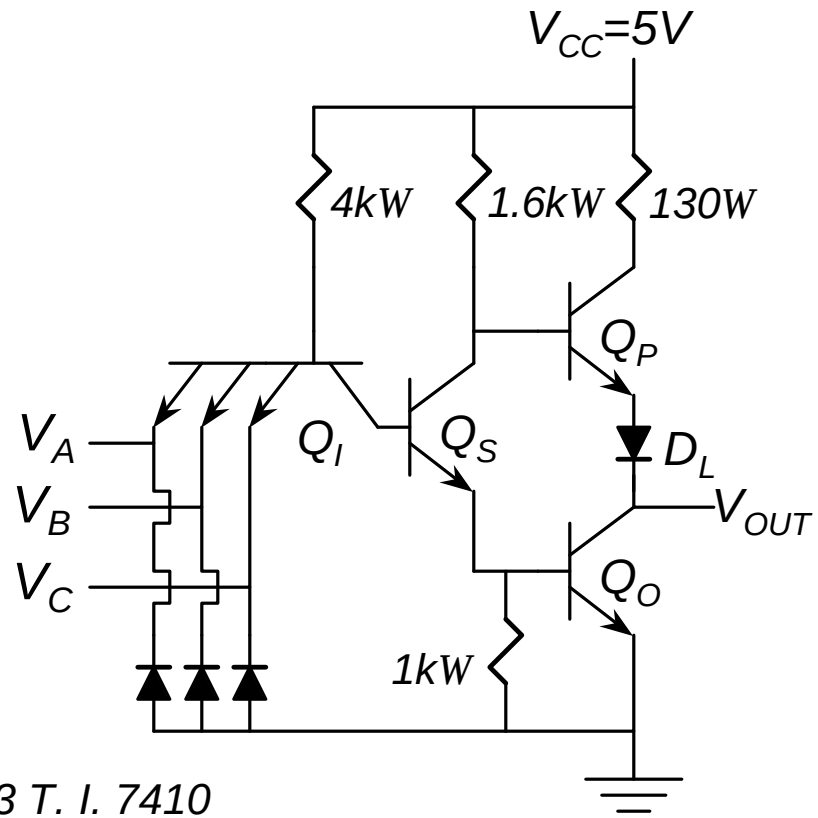
  $V_{CS} = V_{CESO} + V_D + V_{BEAP}$

  $= 1.6V$
- *Initially,*

$$I_{BP} =$$

R_{CP} limits the collector current to a safe value.

Typical 74xx Series TTL

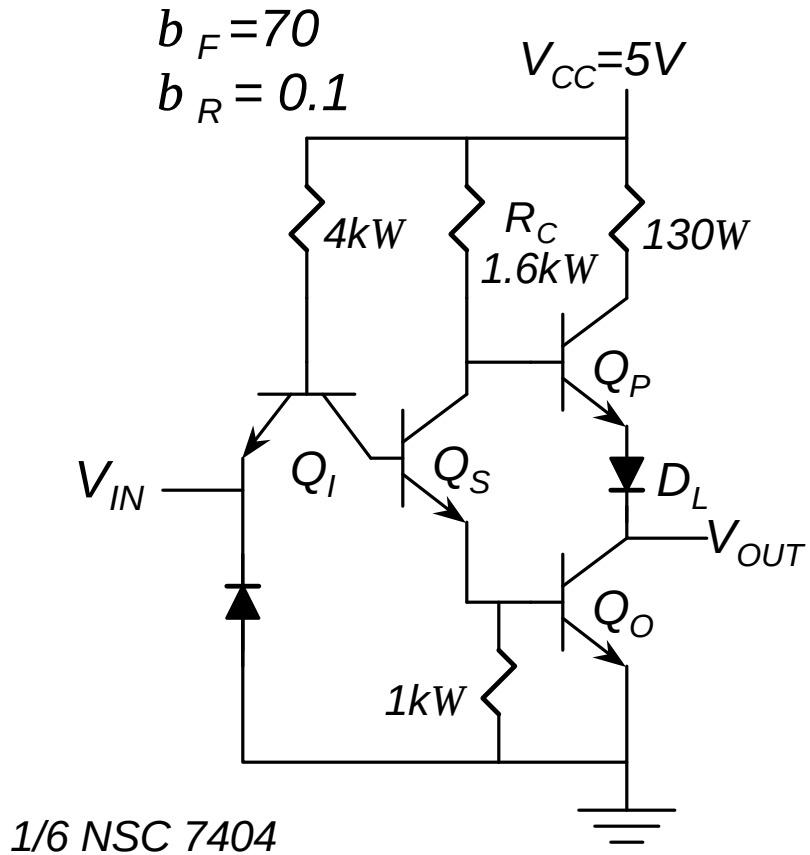


1/3 T. I. 7410
triple 3-input NAND

74xx TTL Characteristics	
t_{PLH}	*12 ns*
t_{PHL}	*8 ns*
Fanout	*10*
Dissipation	*10 mW*
PDP	*100 pJ*

The anti-ringing diodes at the input are normally cut off. During switching transients, they turn on if an input goes more negative than -0.7V.

Standard TTL: VTC



1/6 NSC 7404
Hex Inverter

- $\underline{V_{IN}=0.}$ Q_I is saturated; Q_S, Q_O are cutoff; Q_P is forward active.

  V_{OH} =

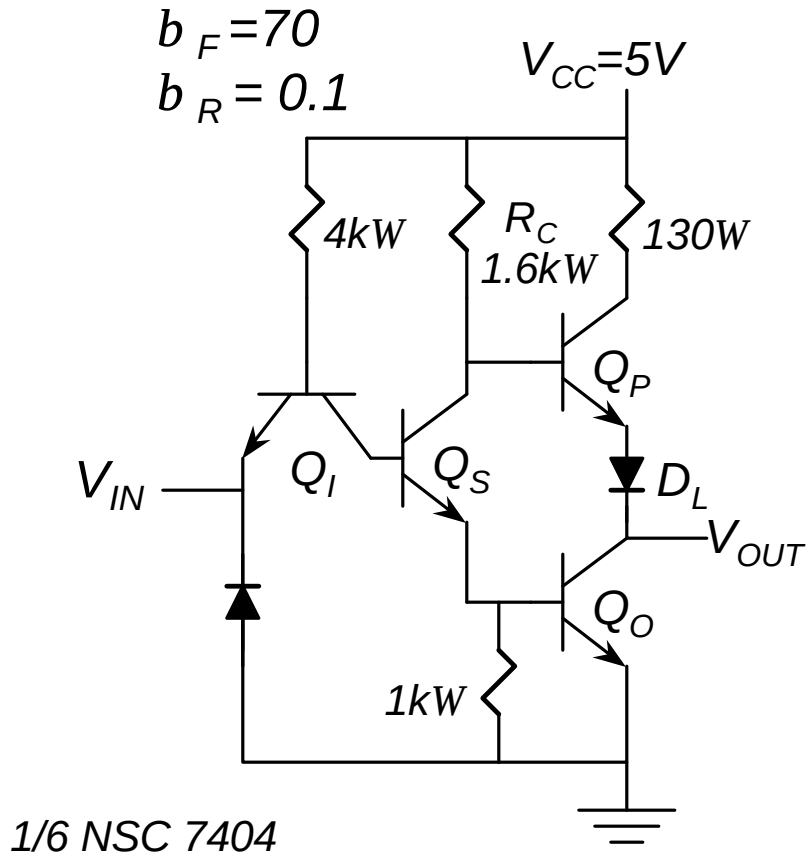
  (the drop in the base resistor is small)

- $\underline{\text{First Breakpoint.}}$ Q_S turns on.

  V_{IL} =

  (at the edge of conduction, I_C=0)

Standard TTL: VTC



1/6 NSC 7404
Hex Inverter

- <u>Second Breakpoint.</u> Q_O turns on.

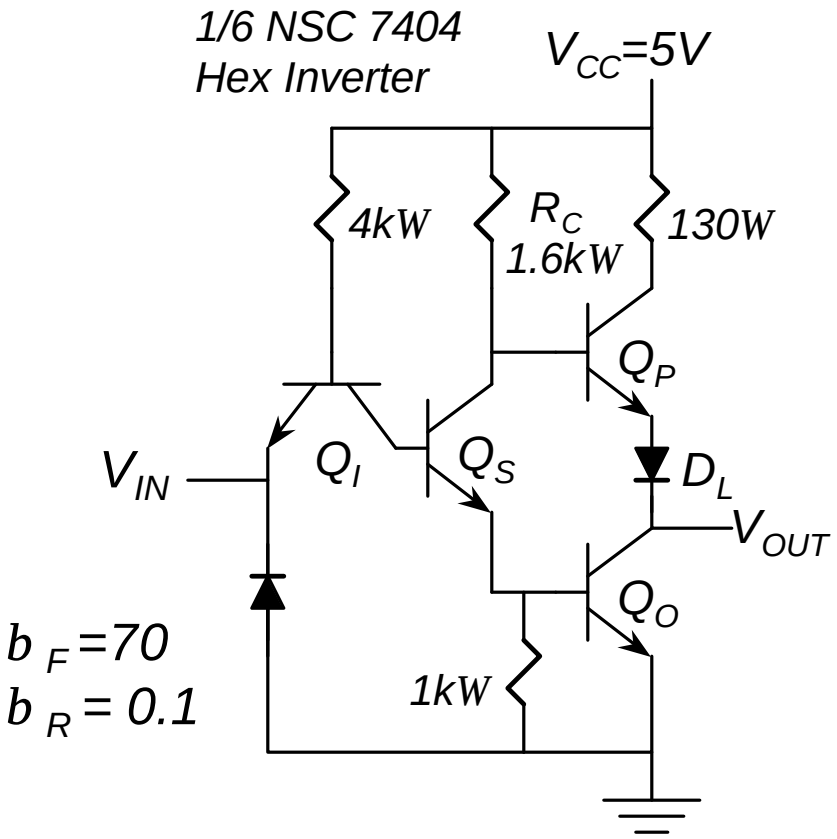
  V_{IN} =

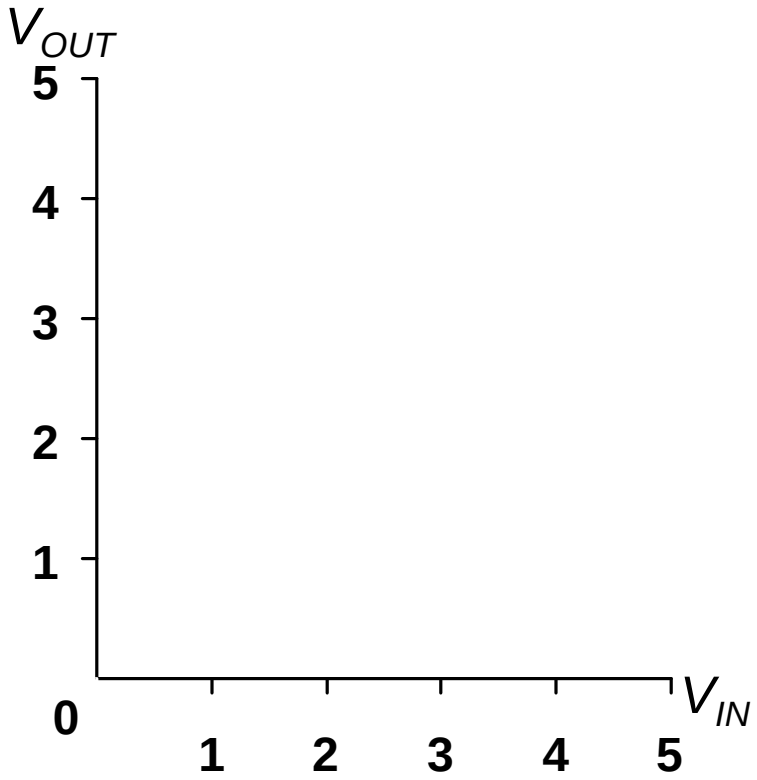
  V_{OUT} =

- <u>Third Breakpoint.</u> Q_O saturates.

  V_{IH} =

Standard TTL: VTC

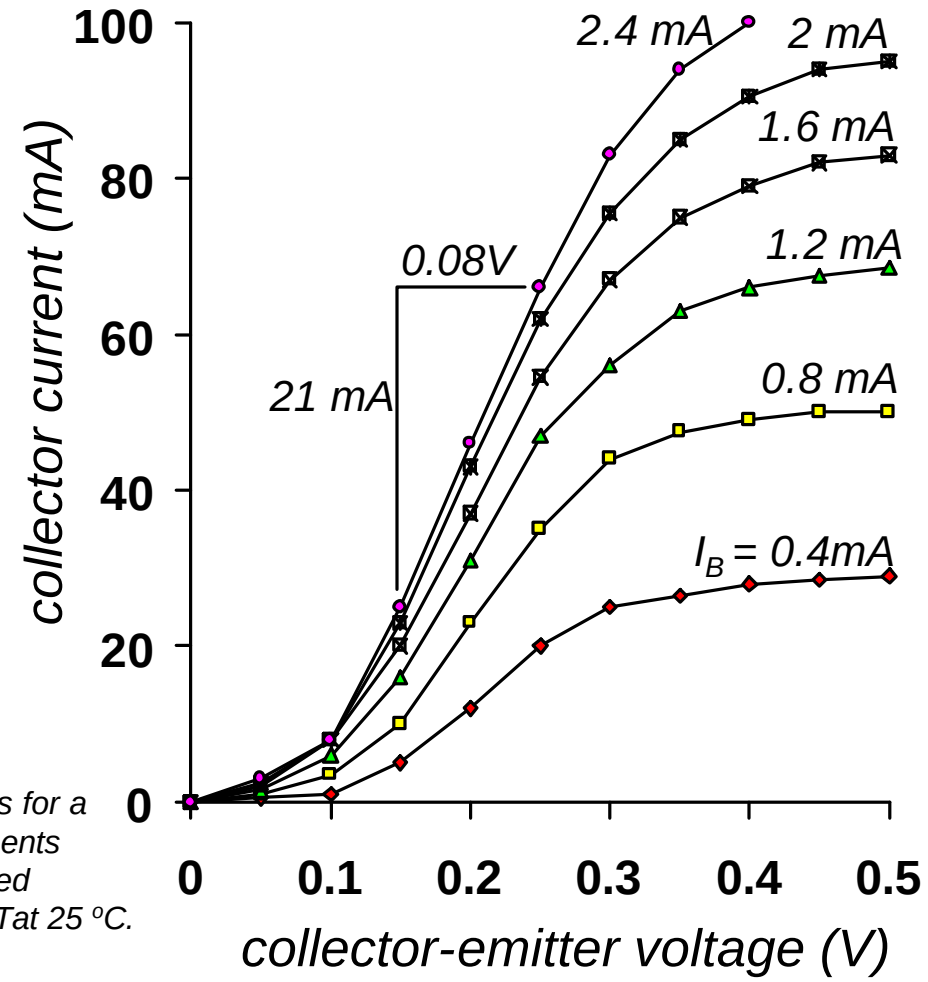




V_{NML} =

V_{NMH} =

Standard TTL: Low State R_{OUT}



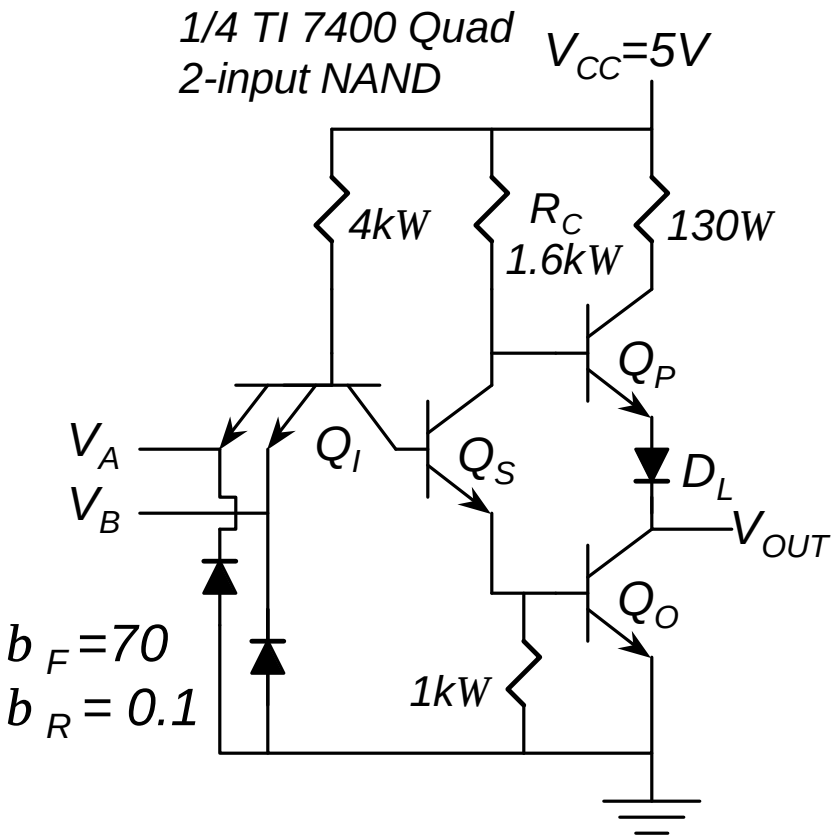
Characteristics for a Texas Instruments junction isolated digital npn BJTat 25 °C.

For the saturated BJT with I_B = 2.4 mA, the output impedance is

$$R_{OL} =$$

The very low output impedance means that noise currents are translated into tiny noise voltages. Thus only a small noise margin is neccesary.

Standard TTL: Input Current



- I_{IH} (Q_I is reverse active)

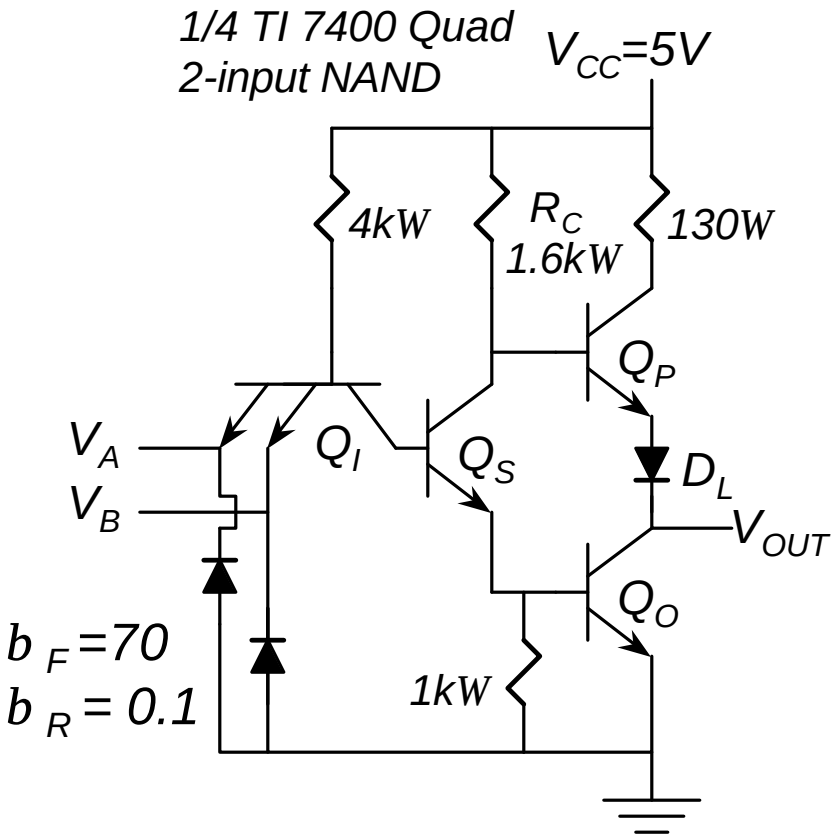
$$I_{BI} =$$

$$I_{IH} =$$

- I_{IL} (Q_I is saturated)

$$I_{IL} =$$

Standard TTL: DC Fanout



- *With high inputs,*

$$I_{CI} =$$

$$I_{CS} =$$

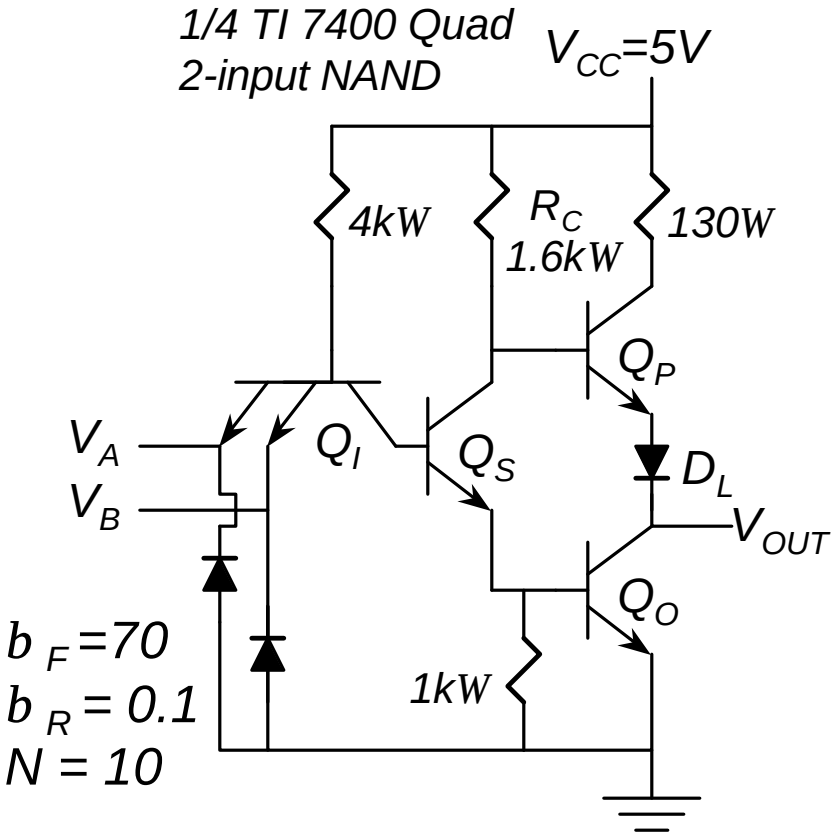
$$I_{BO} =$$

- *To keep Q_O saturated,*

$$N_{\max} =$$

AC considerations usually limit the fanout to a much lower number.

Standard TTL: DC Dissipation



$P_H =$

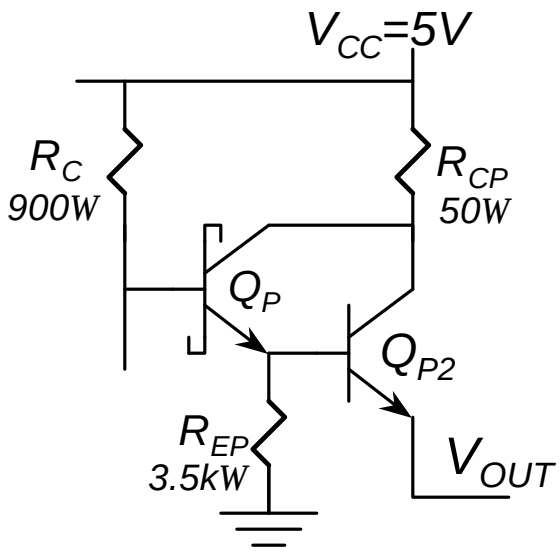
$P_L =$

$P =$

Advanced TTL Designs

- *Schottky Clamping. Q_S and Q_O may be Schottky clamped, preventing saturation. This greatly improves t_{PLH}.*
- *Darlington Pullup. The Darlington pullup arrangement increases the average output drive current for charging a capacitive load. Although R_{CP} limits the maximum output current, this maximum drive is maintained over a wider range of V_{OUT} than with a single pullup transistor.*
- *Squaring Circuit. Active pull-down for the base of the output transistor squares the VTC, improving the low noise margin. An added benefit is faster charge removal for the output transistor.*
- *Improved Fabrication. Smaller devices, and oxide isolation, have steadily reduced parasitic capacitances and reduced RC time constants.*

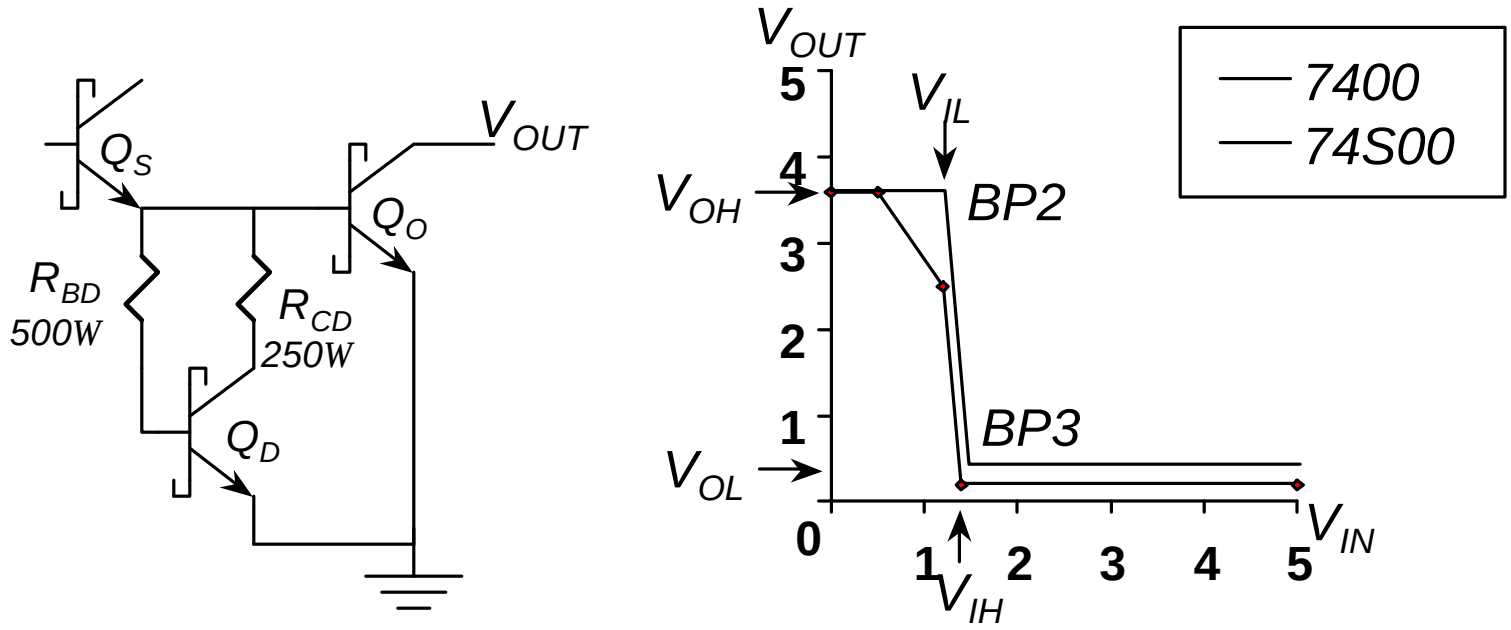
Darlington Pullup



- Q_{P2} *is added, forming a Darlington pair with* Q_P.
- *The EB junction of* Q_{P2} *introduces a 0.7V level shift, so DL can be eliminated.*
- Q_{P2} *can not saturate, so Schottky clamping is not neccessary.*
- R_{EP} *is needed to provide a discharge path for* Q_{P2} *base charge.*

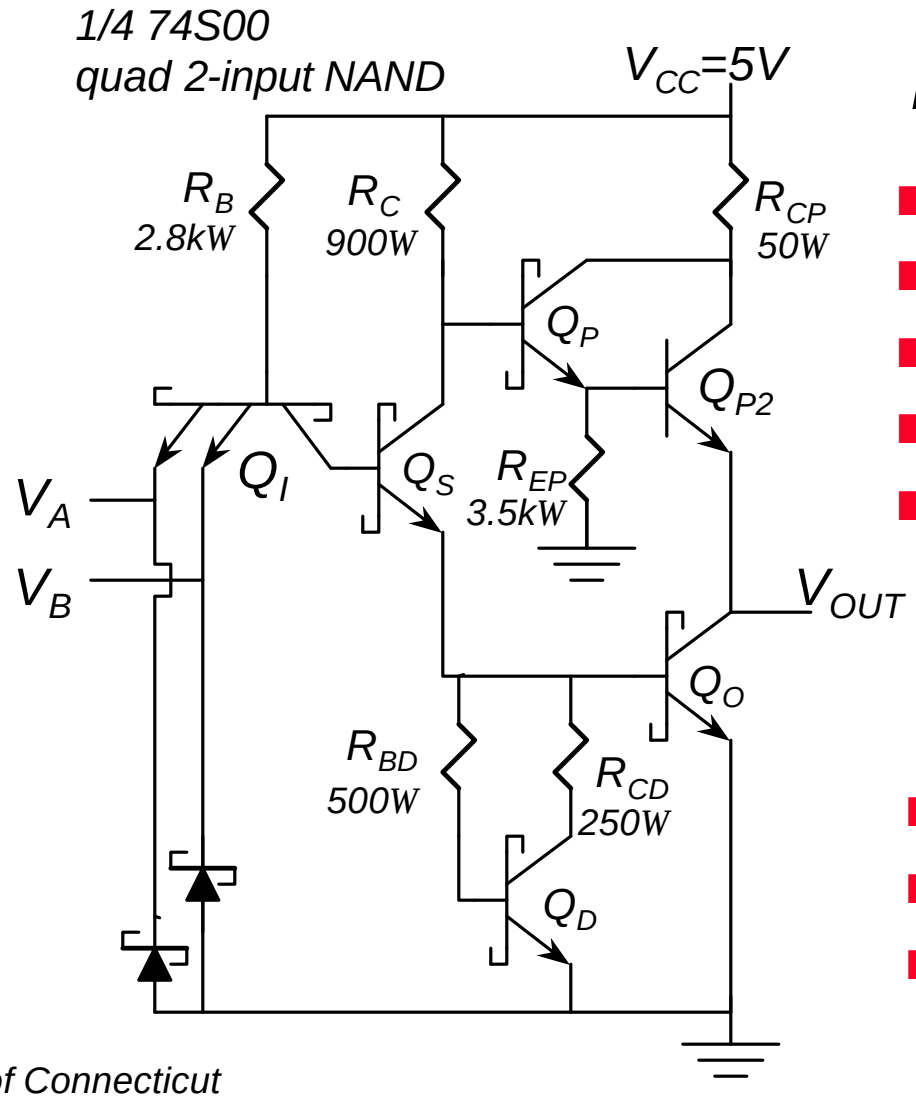
The Darlington emitter follower provides a very low output impedance, approaching R_C/b^2. *This greatly reduces the rise time.*

Squaring Circuit



- *There is no path for Q_S emitter current until Q_D and Q_O turn on.*
- *Q_S and Q_O begin to conduct simultaneously.*
- *BP1 is eliminated from the VTC; in other words, the VTC is "squared."*
- *V_{IL} is increased, improving the low noise margin.*

Schottky TTL (74S / 54S Series)



Features:

- *Schottky clamping*
- *Schottky anti-ringing diodes*
- *Darlington pullup circuit*
- *Squaring circuit*
- *Scaled resistors*

Performance:

- *P = 20 mW*
- *t_P = 3 ns (15 pF)*
- *PDP = 60 pJ*