

# **CURRICULUM VITAE**

## **AHMED H. M. E. HAREEDY**

***Assistant Professor, EEE Department, Middle East Technical University***

Address: Üniversiteler Mahallesi, Dumlupınar Bulvarı No:1 06800 Çankaya, Ankara, Turkey.

E-mail: ahareedy@metu.edu.tr. Phone number: +90 531 505 7285.

### **PERSONAL INFORMATION**

- ***Date of birth:*** March 22, 1984.
- ***Citizenship:*** Egyptian.

### **RESEARCH INTERESTS**

- My research interests are broadly in coding/information theory, focusing on state-of-the-art coding techniques for data-hungry applications, including data storage, cloud storage, blockchain-based systems, machine learning, distributed computing, quantum computing, DNA analysis, computer systems, and wireless communications.
- The techniques I develop involve tools from combinatorics, graph theory, linear algebra, algorithms, probability theory, stochastic processes, statistics, abstract algebra, and optimization.

### **WORK EXPERIENCE**

***Assistant Professor at Middle East Technical University (METU)***

- Assistant Professor in the Electrical and Electronics Engineering (EEE) Department, Middle East Technical University, 2022-present.

***Affiliated Faculty at Middle East Technical University (METU)***

- Affiliated Faculty Member in the Institute of Applied Mathematics (IAM), Middle East Technical University, 2023-present.

***Director of the Reliable and Efficient INFORMATION Systems (REINS) Group at METU.***

***Postdoctoral Associate at Duke University***

- Postdoctoral Associate in the Electrical and Computer Engineering (ECE) Department, Duke University, 2018-2021.
- ***Overall rating:*** Exceptional in 2018-2019, 2019-2020, and 2020-2021.
- ***Major projects:*** Developing coding theoretic techniques to enhance the performance and the reliability of modern data storage, cloud storage, computational storage, distributed computing, DNA data storage, and quantum computing systems.

***Development Engineer at Mentor Graphic Corporation***

- Senior Development Engineer in the Device Modeling Team (DMT), Analog-Mixed Signal (AMS) Verification, Deep Sub-Micron (DSM) Division, Mentor Graphics Corporation (MGC), 2006-2014.
- ***Major projects:*** Device models implementation/testing, TSMC modeling interface (TMI), input-output buffer information specification (IBIS) modeling, reliability framework standardization, and parameter extraction for new technologies.

# **CURRICULUM VITAE**

## **INTERNSHIP EXPERIENCE**

### ***ECC Architect at Intel Corporation***

- Error-Correction Coding (ECC) Architect in the Non-Volatile Memory Solutions Group (NSG), Intel Corporation, June 2017-September 2017.
- **Major project:** Designing spatially-coupled codes for Flash memories.
  
- Error-Correction Coding (ECC) Architect in the Non-Volatile Memory Solutions Group (NSG), Intel Corporation, June 2015-September 2015.
- **Major project:** Designing non-binary LDPC codes for Flash memories.

## **EDUCATION**

### ***Ph.D. in Electrical and Computer Engineering, 2018***

- **Institution:** The University of California, Los Angeles (UCLA).
- **GPA:** 3.925. Advanced to candidacy in June 2016.
- **Lab:** Laboratory for Robust Information Systems (LORIS).
- **Dissertation:** Graph-Based Error Correcting Codes for Modern Dense Storage Devices.  
**Distinguished Ph.D. Dissertation Award**

### ***M.S. in Electronics and Communications Engineering, 2011***

- **Institution:** Cairo University.
- **Rating:** Distinction (94.70%) and ranked 1<sup>st</sup>.
- **Thesis:** LDPC Decoding Using Selective Max-Min (SMM) Algorithm: Theory and Implementation.

### ***Bachelor of Electronics and Communications Engineering, 2006***

- **Institution:** Cairo University.
- **Rating:** Distinction with honor (86.03%).
- **Graduation project:** CUSPARC Processor: Optimization, Characterization and Testing.  
**Egyptian Engineering Day Award**

## **MAJOR STUDIES**

- Coding theory, information theory, data storage, data analysis, signal processing, communication theory, mathematics, computer systems, and electronics (device physics/modeling).

## **TEACHING EXPERIENCE**

### ***Instructor at METU***

- Instructor for Coding Theory (EE 534) at METU, spring 2022.
- Instructor for Signals and Systems II (EE 306) at METU, spring 2022.
- Instructor for Coding Theory (EE 534) at METU, fall 2022.
- Instructor for Computer Architecture I (EE 445) at METU, fall 2022.
- Instructor for Signals and Systems II (EE 306) at METU, spring 2023.
- Instructor for Coding Theory (EE 534) at METU, fall 2023.
- Instructor for Computer Architecture I (EE 445) at METU, fall 2023.

## **CURRICULUM VITAE**

- Instructor for Signals and Systems II (EE 306) at METU, spring 2024.
- Instructor for Probability and Random Variables (EE 230) at METU, spring 2024.

### ***Instructor at Duke University***

- Instructor for Modern Coding Theory with Applications in Data Science (ECE/CS 590) at Duke University, spring 2020.
- **Overall rating:** Average: 4.60/5.00. Median: 5.00/5.00.
- Several conference and journal papers resulted from the course projects.

### ***Teaching Assistant at UCLA***

- Teaching Assistant for Probability and Statistics (EE 131A) at UCLA, winter 2017.
- **Overall rating:** Average: 8.24/9.00. Median: 9.00/9.00.

#### **Excellence in Teaching Award**

- Teaching Assistant for Probability and Statistics (EE 131A) at UCLA, winter 2016.
- **Overall rating:** Average: 8.17/9.00. Median: 9.00/9.00.

## **AWARDS & HONORS**

### ***Best Paper Award, 2020***

- My paper “A combinatorial methodology for optimizing non-binary graph-based codes: Theoretical analysis and applications in data storage” won the 2018-2019 Best Student Paper Award of the IEEE Data Storage Technical Committee (DSTC).

### ***Distinguished Ph.D. Dissertation Award, 2019***

- I won the prestigious 2018-2019 Distinguished Ph.D. Dissertation Award in Signals and Systems from the Electrical and Computer Engineering (ECE) Department at UCLA.

### ***Memorable Paper Award, 2018***

- My paper “A three-stage approach for designing non-binary spatially-coupled codes for Flash memories,” which is a summary of my paper “High performance non-binary spatially-coupled codes for Flash memories,” won the inaugural Memorable Paper Award at the 2018 Non-Volatile Memories Workshop (NVMW), in the area of devices, coding, and information theory.

### ***Dissertation Year Fellowship, 2017***

- I was one of only four Ph.D. candidates in the Electrical Engineering Department at UCLA who won the 2017-2018 Dissertation Year Fellowship (DYF), which is a campus-wide fellowship.

### ***Excellence in Teaching Award, 2017***

- I won the 2016-2017 Electrical Engineering Henry Samueli Excellence in Teaching Award for teaching Probability and Statistics (EE 131A) at UCLA.

### ***ITA Graduation Day Talk, 2017***

- I represented UCLA by giving a Graduation Day (GD) Talk at the 2017 Information Theory and Applications Workshop (ITA).

## **CURRICULUM VITAE**

### ***Best Paper Award, 2015***

- My paper “Non-binary LDPC code optimization for partial-response channels” won the Best Paper Award at the 2015 IEEE Global Communications Conference (GLOBECOM), Selected Areas in Communications (SAC), Data Storage Track.

### ***Ph.D. Scholarship, 2014-2018***

- I received a Ph.D. scholarship offer to work as a Graduate Student Researcher (GSR) with LORIS Lab in the ECE Department at UCLA.

### ***Egyptian Engineering Day Award, 2006***

- My CUSPARC graduation project was the winner of the first prize at the 2006 Egyptian Engineering Day (EED) organized by IEEE Young Professionals (YP) Egypt.

## **FUNDING**

- I have been awarded the **TÜBİTAK 2232-B International Fellowship for Early Stage Researchers** in 2022. My Research Project Proposal is titled “Reliable low-latency storage and computing at the network edge via combining machine learning and coding,” under the Research Plan titled “From devices to clouds and beyond: Coding for modern and next generation storage and computing systems.”
- I contributed to an NSF proposal with collaborators at Duke University and at the University of Arizona (UA) on quantum error correction, funded by the CISE Directorate in 2021.
- I submitted an NSF proposal as a co-PI with Robert Calderbank titled “Reconfigurable constrained codes for modern data storage devices” to the CISE Directorate in 2019.

## **PUBLICATIONS**

### ***Journal Articles***

- C. Irimagzi, Y. Uslan, and **A. Hareedy**, “Protecting the future of information: LOCO coding with error detection for DNA data storage,” accepted at *IEEE Transactions on Molecular, Biological and Multi-Scale Communications*, 2024.
- I. Guzel, D. Ozbayrak, R. Calderbank, and **A. Hareedy**, “Eliminating media noise while preserving storage capacity: Reconfigurable constrained codes for two-dimensional magnetic recording,” accepted at *IEEE Transactions on Information Theory*, 2024.
- **A. Hareedy**, S. Zheng, P. Siegel, and R. Calderbank, “Efficient constrained codes that enable page separation in modern Flash memories,” *IEEE Transactions on Communications*, vol. 71, no. 12, pp. 6834-6848, Dec. 2023.
- S. Yang, **A. Hareedy**, R. Calderbank, and L. Dolecek, “Breaking the computational bottleneck: Probabilistic optimization of high-memory spatially-coupled codes,” *IEEE Transactions on Information Theory*, vol. 69, no. 2, pp. 886-909, Feb. 2023.
- **A. Hareedy**, B. Dabak, and R. Calderbank, “The secret arithmetic of patterns: A general method for designing constrained codes based on lexicographic indexing,” *IEEE Transactions on Information Theory*, vol. 68, no. 9, pp. 5747-5778, Sep. 2022.

## **CURRICULUM VITAE**

- S. Yang, **A. Hareedy**, R. Calderbank, and L. Dolecek, “Hierarchical coding for cloud storage: Topology-adaptivity, scalability, and flexibility,” *IEEE Transactions on Information Theory*, vol. 68, no. 6, pp. 3657-3680, Jun. 2022.
- J. Centers, X. Tan, **A. Hareedy**, and R. Calderbank, “Power spectra of constrained codes with level-based signaling: Overcoming finite-length challenges,” *IEEE Transactions on Communications*, vol. 69, no. 8, pp. 4971-4986, Aug. 2021.
- **A. Hareedy**, B. Dabak, and R. Calderbank, “Managing device lifecycle: Reconfigurable constrained codes for M/T/Q/P-LC Flash memories,” *IEEE Transactions on Information Theory*, vol. 67, no. 1, pp. 282-295, Jan. 2021.
- B. Dabak, **A. Hareedy**, and R. Calderbank, “Non-binary constrained codes for two-dimensional magnetic recording,” *IEEE Transactions on Magnetics*, vol. 56, no. 11, Nov. 2020.
- **A. Hareedy**, R. Kuditipudi, and R. Calderbank, “Minimizing the number of detrimental objects in multi-dimensional graph-based codes,” *IEEE Transactions on Communications*, vol. 68, no. 9, pp. 5299-5312, Sep. 2020.
- **A. Hareedy**, R. Wu, and L. Dolecek, “A channel-aware combinatorial approach to design high performance spatially-coupled codes,” *IEEE Transactions on Information Theory*, vol. 66, no. 8, pp. 4834-4852, Aug. 2020.
- **A. Hareedy** and R. Calderbank, “LOCO codes: Lexicographically-ordered constrained codes,” *IEEE Transactions on Information Theory*, vol. 66, no. 6, pp. 3572-3589, Jun. 2020.
- **A. Hareedy**, C. Lanka, N. Guo, and L. Dolecek, “A combinatorial methodology for optimizing non-binary graph-based codes: Theoretical analysis and applications in data storage,” **Best Paper Award** *IEEE Transactions on Information Theory*, vol. 65, no. 4, pp. 2128-2154, Apr. 2019.
- H. Esfahanizadeh, **A. Hareedy**, and L. Dolecek, “Finite-length construction of high performance spatially-coupled codes via optimized partitioning and lifting,” *IEEE Transactions on Communications*, vol. 67, no. 1, pp. 3-16, Jan. 2019.
- H. Esfahanizadeh, **A. Hareedy**, R. Wu, R. Galbraith, and L. Dolecek, “Spatially-coupled codes for channels with SNR variation,” *IEEE Transactions on Magnetics*, vol. 54, no. 11, Nov. 2018.
- H. Esfahanizadeh, **A. Hareedy**, and L. Dolecek, “Spatially-coupled codes optimized for magnetic recording applications,” *IEEE Transactions on Magnetics*, vol. 53, no. 2, Feb. 2017.
- **A. Hareedy**, C. Lanka, and L. Dolecek, “A general non-binary LDPC code optimization framework suitable for dense Flash memory and magnetic storage,” *IEEE Journal on Selected Areas in Communications*, vol. 34, no. 9, pp. 2402-2415, Sep. 2016.
- **A. Hareedy**, B. Amiri, R. Galbraith, and L. Dolecek, “Non-binary LDPC codes for magnetic recording channels: Error floor analysis and optimized code design,” *IEEE Transactions on Communications*, vol. 64, no. 8, pp. 3194-3207, Aug. 2016.
- **A. H. Hareedy** and M. M. Khairy, “Selective max-min algorithm for low-density parity-check decoding,” *IET Communications*, vol. 7, no. 1, pp. 65-70, Jan. 2013.

### **Preprints**

- S. Yang, **A. Hareedy**, R. Calderbank, and L. Dolecek, “Hierarchical hybrid error correction for time-sensitive devices at the edge.”

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- B. Dabak, **A. Hareedy**, A. Ashikhmin, and R. Calderbank, “Unequal error protection achieves threshold gains on BEC and BSC via higher fidelity messages.”

### **Conference Papers**

- C. Irimagzi, A. Tanrikulu, and **A. Hareedy**, “Probabilistic design of multi-dimensional spatially-coupled codes,”  
accepted at *IEEE International Symposium on Information Theory (ISIT)*, 2024.
- D. Ozbayrak, D. Uyar, and **A. Hareedy**, “Low-complexity constrained coding schemes for two-dimensional magnetic recording,”  
accepted at *IEEE International Symposium on Information Theory (ISIT)*, 2024.
- B. Dabak, E. Tiryaki, R. Calderbank, and **A. Hareedy**, “LDPC decoders prefer more reliable parity bits: Unequal data protection over BSC,”  
in *Proc. International Symposium on Topics in Coding (ISTC)*, Brest, France, Sep. 2023, pp. 1-5.
- **A. Hareedy**, S. Zheng, P. Siegel, and R. Calderbank, “Read-and-run constrained coding for modern Flash devices,”  
in *Proc. IEEE International Conference on Communications (ICC)*, Seoul, South Korea, May 2022, pp. 3466-3471.
- S. Yang, **A. Hareedy**, S. Venkatasubramanian, R. Calderbank, and L. Dolecek, “GRADE-AO: Towards near-optimal spatially-coupled codes with high memories,”  
in *Proc. IEEE International Symposium on Information Theory (ISIT)*, Melbourne, Australia, Jul. 2021, pp. 587-592.
- **A. Hareedy**, B. Dabak, and R. Calderbank, “Q-ary asymmetric LOCO codes: Constrained codes supporting Flash evolution,”  
in *Proc. IEEE International Symposium on Information Theory (ISIT)*, Los Angeles, CA, USA, Jun. 2020, pp. 688-693.
- S. Yang, **A. Hareedy**, R. Calderbank, and L. Dolecek, “Topology-aware cooperative data protection in blockchain-based decentralized storage networks,”  
in *Proc. IEEE International Symposium on Information Theory (ISIT)*, Los Angeles, CA, USA, Jun. 2020, pp. 622-627.
- S. Yang, **A. Hareedy**, R. Calderbank, and L. Dolecek, “Hierarchical coding to enable scalability and flexibility in heterogeneous cloud storage,”  
in *Proc. IEEE Global Communications Conference (GLOBECOM)*, Waikoloa, HI, USA, Dec. 2019, pp. 1-6.
- **A. Hareedy** and R. Calderbank, “Asymmetric LOCO codes: Constrained codes for Flash memories,”  
in *Proc. Allerton Conference on Communications, Control, and Computing (Allerton)*, Monticello, IL, USA, Sep. 2019, pp. 124-131.
- **A. Hareedy**, R. Kuditipudi, and R. Calderbank, “Increasing the lifetime of Flash memories using multi-dimensional graph-based codes,”  
in *Proc. IEEE Information Theory Workshop (ITW)*, Visby, Sweden, Aug. 2019, pp. 1-5.
- **A. Hareedy** and R. Calderbank, “A new family of constrained codes with applications in data storage,”  
in *Proc. IEEE Information Theory Workshop (ITW)*, Visby, Sweden, Aug. 2019, pp. 1-5.

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- **A. Hareedy**, H. Esfahanizadeh, A. Tan, and L. Dolecek, “Spatially-coupled code design for partial-response channels: Optimal object-minimization approach,” in *Proc. IEEE Global Communications Conference (GLOBECOM)*, Abu Dhabi, UAE, Dec. 2018, pp. 1-7.
- H. Esfahanizadeh, **A. Hareedy**, and L. Dolecek, “Multi-dimensional spatially-coupled code design through informed relocation of circulants,” in *Proc. Allerton Conference on Communications, Control, and Computing (Allerton)*, Monticello, IL, USA, Oct. 2018, pp. 695-701.
- H. Esfahanizadeh, **A. Hareedy**, R. Galbraith, R. Wu, and L. Dolecek, “Spatially-coupled codes for channels with SNR variation,” in *Proc. IEEE International Magnetics Conference (INTERMAG)*, Singapore, Singapore, Apr. 2018.
- **A. Hareedy**, H. Esfahanizadeh, and L. Dolecek, “High performance non-binary spatially-coupled codes for Flash memories,” **Memorable Paper Award** in *Proc. IEEE Information Theory Workshop (ITW)*, Kaohsiung, Taiwan, Nov. 2017, pp. 229-233.
- H. Esfahanizadeh, **A. Hareedy**, and L. Dolecek, “A novel combinatorial framework to construct spatially-coupled codes: Minimum overlap partitioning,” in *Proc. IEEE International Symposium on Information Theory (ISIT)*, Aachen, Germany, Jun. 2017, pp. 1693-1697.
- H. Esfahanizadeh, **A. Hareedy**, and L. Dolecek, “The finite length analysis of spatially-coupled codes for 1-D magnetic recording channels,” in *Proc. Asilomar Conference on Signals, Systems, and Computers (Asilomar)*, Pacific Grove, CA, USA, Nov. 2016, pp. 1128-1132.
- **A. Hareedy**, C. Lanka, C. Schoeny, and L. Dolecek, “The weight consistency matrix framework for general non-binary LDPC code optimization: Applications in Flash memories,” in *Proc. IEEE International Symposium on Information Theory (ISIT)*, Barcelona, Spain, Jul. 2016, pp. 2709-2713.
- **A. Hareedy**, B. Amiri, S. Zhao, R. Galbraith, and L. Dolecek, “Non-binary LDPC code optimization for partial-response channels,” **Best Paper Award** in *Proc. IEEE Global Communications Conference (GLOBECOM)*, San Diego, CA, USA, Dec. 2015, pp. 1-6.
- E. E. O. Hussein *et al.*, “CUSPARC IP processor: Design, characterization and applications,” in *Proc. International Conference on Microelectronics (ICM)*, Cairo, Egypt, Dec. 2010, pp. 435-438.
- Y. Sabry, **A. Hareedy**, and M. Selim, “Novel method for modeling IBIS4.2 four-level hysteresis behavior in an analog simulator,” in *Proc. Electronics Packaging Technology Conference (EPTC)*, Singapore, Singapore, Dec. 2008, pp. 1403-1408.

### **Workshop Abstracts**

- **A. Hareedy**, S. Zheng, P. Siegel, and R. Calderbank, “Read-and-run constrained coding for modern Flash memories,” *Non-Volatile Memories Workshop (NVMW)*, San Diego, CA, USA, Mar. 2024.
- J. Centers, X. Tan, **A. Hareedy**, and R. Calderbank, “Power spectra of finite-length constrained codes with level-based signaling,” *Non-Volatile Memories Workshop (NVMW)*, San Diego, CA, USA, Mar. 2021.

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- S. Yang, **A. Hareedy**, R. Calderbank, and L. Dolecek, “Cooperative data protection for topology-aware decentralized storage networks,”  
*Non-Volatile Memories Workshop (NVMW)*, San Diego, CA, USA, Mar. 2021.
- H. Esfahanizadeh, **A. Hareedy**, and L. Dolecek, “Multi-dimensional spatially-coupled code design with improved cycle properties,”  
*Non-Volatile Memories Workshop (NVMW)*, San Diego, CA, USA, Mar. 2019.
- **A. Hareedy**, H. Esfahanizadeh, and L. Dolecek, “A three-stage approach for designing non-binary spatially-coupled codes for Flash memories,” (summary of my ITW 2017 paper)  
*Non-Volatile Memories Workshop (NVMW)*, San Diego, CA, USA, Mar. 2018.
- **A. Hareedy**, C. Lanka, and L. Dolecek, “Non-binary LDPC code optimization for modern storage systems,”  
*Non-Volatile Memories Workshop (NVMW)*, San Diego, CA, USA, Mar. 2017.
- C. Schoeny, B. Amiri, **A. Hareedy**, and L. Dolecek, “Quasi-cyclic non-binary LDPC codes for MLC NAND Flash memory,”  
*Non-Volatile Memories Workshop (NVMW)*, San Diego, CA, USA, Mar. 2015.

## **COMMUNITY SERVICE**

- **TPC member**: TPC member at the IEEE ICC, Selected Areas in Communications (SAC): Cloud Computing, Networking, and Storage, 2024.
- **TPC member**: TPC member at the NVMW, 2024.
- **Guest Editor**: Editor for a special issue of the IEEE BITS Magazine (the IEEE Information Theory Magazine) on data storage, 2023.
- **DSTC member**: Member of the IEEE Data Storage Technical Committee (DSTC).
- **TPC member**: TPC member at the IEEE ICC, Selected Areas in Communications (SAC): Cloud Computing, Networking, and Storage, 2023.
- **Session chair**: Session chair for SAC-CCNS-2 (Edge Computing II) at the IEEE ICC, 2022.
- **TPC member**: TPC member at the IEEE GLOBECOM, Selected Areas in Communications (SAC): Cloud & Fog/Edge Computing, Networking, and Storage (CCNS), 2021.
- **Session chair**: Session chair for 4A (Devices and ECC) at the NVMW, 2021.
- **TPC member**: TPC member at the NVMW, 2021.
- **TPC member**: TPC member at the IEEE GLOBECOM, Selected Areas in Communications (SAC): Cloud & Fog/Edge Computing, Networking, and Storage (CCNS), 2020.
- **TPC member**: TPC member at the IEEE International Conference on Cloud Computing (CLOUD), 2020.
- **TPC member**: TPC member at the NVMW, 2020 (also served on the Memorable Paper Award Selection Subcommittee).
- **Session chair**: Session chair for SAC CCNS1 (Coded Data Storage) at the IEEE GLOBECOM, 2019.
- **Reviewer**: I regularly review papers for various journals and conferences in coding/information theory, communications, and storage:
  - *IEEE Transactions on Information Theory (TIT)*,
  - *IEEE Transactions on Communications (TCOM)*,
  - *IEEE Transactions on Magnetics (TMAG)*,
  - *IEEE Communications Letters (COML)*,

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- *IET Communications*,
- *IEEE International Symposium on Information Theory (ISIT)*,
- *IEEE Information Theory Workshop (ITW)*,
- *IEEE Global Communications Conference (GLOBECOM)*,
- *IEEE International Symposium on Topics in Coding (ISTC)*.

### **TALKS**

#### **Oral Tutorials**

- **A. Hareedy**, “Graph-based error correcting codes for Flash memories,”  
*Flash Memory Summit (FMS)*, Santa Clara, CA, USA, Aug. 2019.

#### **Oral Presentations**

- **A. Hareedy**, S. Zheng, P. Siegel, and R. Calderbank, “Read-and-run constrained coding for modern Flash devices,”  
*IEEE International Conference on Communications (ICC)*, Seoul, South Korea, May 2022.
- **A. Hareedy**, “From devices to clouds: Coding for modern and next generation storage and computing systems,”  
Télécom Paris (ENST), Oct. 2021.
- **A. Hareedy**, “From devices to clouds: Coding for modern and next generation storage systems,”  
Koç University, Jun. 2021.
- **A. Hareedy**, “From devices to clouds: Coding for modern and next generation storage systems,”  
Middle East Technical University (METU), Jun. 2021.
- **A. Hareedy**, “From devices to clouds: Coding for modern and next generation storage systems,”  
Bilkent University, Apr. 2021.
- **A. Hareedy**, “From devices to clouds: Coding for modern and next generation storage systems,”  
The Pennsylvania State University (Penn State), Feb. 2021.
- **A. Hareedy**, B. Dabak, and R. Calderbank, “Q-ary asymmetric LOCO codes: Constrained codes supporting Flash evolution,”  
*IEEE International Symposium on Information Theory (ISIT)*, Los Angeles, CA, USA, Jun. 2020.
- **A. Hareedy**, “From devices to clouds: Coding for modern and next generation storage systems,”  
The University of Colorado, Boulder (CU Boulder), Mar. 2020.
- **A. Hareedy**, “Modern coding techniques for highly reliable massive storage systems,”  
Eindhoven University of Technology (TU/e), Oct. 2019.
- **A. Hareedy** and R. Calderbank, “Asymmetric LOCO codes: Constrained codes for Flash memories,”  
*Allerton Conference on Communications, Control, and Computing (Allerton)*, Monticello, IL, USA, Sep. 2019.
- **A. Hareedy**, H. Esfahanizadeh, A. Tan, and L. Dolecek, “Spatially-coupled code design for partial-response channels: Optimal object-minimization approach,”  
*IEEE Global Communications Conference (GLOBECOM)*, Abu Dhabi, UAE, Dec. 2018.
- **A. Hareedy**, H. Esfahanizadeh, and L. Dolecek, “A three-stage approach for designing spatially-coupled codes for Flash memories,”  
*Non-Volatile Memories Workshop (NVMW)*, San Diego, CA, USA, Mar. 2018.

## **CURRICULUM VITAE**

- **A. Hareedy**, H. Esfahanizadeh, and L. Dolecek, “High performance non-binary spatially-coupled codes for Flash memories,”  
*IEEE Information Theory Workshop (ITW)*, Kaohsiung, Taiwan, Nov. 2017.
- **A. Hareedy**, C. Lanka, and L. Dolecek, “LDPC codes for Flash memories,”  
*UCLA ECE Annual Research Review (UCLA ARR)*, Los Angeles, CA, USA, Apr. 2017.
- **A. Hareedy**, C. Lanka, and L. Dolecek, “Non-binary LDPC code optimization for modern storage systems,”  
*Non-Volatile Memories Workshop (NVMW)*, San Diego, CA, USA, Mar. 2017.
- **A. Hareedy** and L. Dolecek, “Graph-based error correcting codes for modern dense storage devices,” **ITA Graduation Day Talk**  
*Information Theory and Applications Workshop (ITA)*, San Diego, CA, USA, Feb. 2017.
- **A. Hareedy**, C. Lanka, C. Schoeny, and L. Dolecek, “The weight consistency matrix framework for general non-binary LDPC code optimization: Applications in Flash memories,”  
*IEEE International Symposium on Information Theory (ISIT)*, Barcelona, Spain, Jul. 2016.
- **A. Hareedy**, B. Amiri, S. Zhao, R. Galbraith, and L. Dolecek, “Non-binary LDPC code optimization for partial-response channels,”  
*IEEE Global Communications Conference (GLOBECOM)*, San Diego, CA, USA, Dec. 2015.
- C. Schoeny, B. Amiri, **A. Hareedy**, and L. Dolecek, “Quasi-cyclic non-binary LDPC codes for MLC NAND Flash memory,”  
*Flash Memory Summit (FMS)*, Santa Clara, CA, USA, Aug. 2015.
- Y. Sabry, **A. Hareedy**, and M. Selim, “Novel method for modeling IBIS4.2 four-level hysteresis behavior in an analog simulator,”  
*Electronics Packaging Technology Conference (EPTC)*, Singapore, Singapore, Dec. 2008.

## **PROGRAMMING SKILLS**

- MATLAB (including Simulink).
- C and C++.
- Shell scripting.
- R and Python.
- Verilog/VHDL (digital design).
- FPGA experience.
- Verilog-A/VHDL-AMS (analog/mixed signal design).
- XML and HTML.

## **COURSES & TRAINING**

### ***Technical Skills***

Selected courses:

- (UCLA) Matrix Analysis, Coding for Modern Storage Devices, Graphs and Network Flows, Information Theory, Network Information Theory (audit), Convex Optimization (audit), Analysis (A and B, audit).
- (MGC) Device Physics, Quantum Mechanics.

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### ***Soft Skills***

Selected courses:

- (Think Logic) Time Management, Presentation Skills.
- (Dale Carnegie) Communication Skills, Problem Solving and Decision Making.

### **LANGUAGES**

- English and Arabic.

### **HOBBIES**

- Writing poems, reading in different fields, calligraphy, and practicing/watching sports.

### **ADDITIONAL INFORMATION**

Additional information is available at my:

- Website <http://users.metu.edu.tr/ahareedy>.
- LinkedIn account <https://www.linkedin.com/in/ahmed-hareedy-8a063063>.
- ORCID <https://orcid.org/0000-0002-8523-6754>.
- Google Scholar account <https://scholar.google.com/citations?user=yNJ0Tq4AAAAJ&hl=en&oi=ao>.
- Research Gate account [https://www.researchgate.net/profile/Ahmed\\_Hareedy](https://www.researchgate.net/profile/Ahmed_Hareedy).