Analog Integr Circ Sig Process (2010) 64:137–145
DOI 10.1007/s10470-009-9433-4

A high performance Σ-Δ readout circuitry for μg resolution microaccelerometers

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Received: 25 August 2008 / Revised: 3 November 2009 / Accepted: 3 December 2009 / Published online: 22 December 2009

Abstract This paper reports a second order electromechanical sigma-delta readout for micro-g resolution accelerometers in addition to other high-sensitivity capacitive microsensors with large base capacitance. The chip implements a switched-capacitor readout front-end and an oversampled sigma-delta modulator, and hence can be used for both open-loop analog readout and closed-loop control and readout with direct digital output. The readout circuit has more than 115 dB dynamic range and can resolve less than 3 aF/$\sqrt{\text{Hz}}$. Also this IC includes start-up circuit and feedback mechanism for closed-loop control of the accelerometer with a single 5 V supply in a ±4 g range. Together with the accelerometer, bandwidth of the overall system is limited with the sensor resonance frequency (1.53 kHz) in the open-loop mode. However in closed loop mode, oversampling of the acceleration data increases the bandwidth of the system up to few hundred kilohertz which is limited with the cut-off frequency of the low-pass filter placed at the output of the system. The start-up circuit allows rebalancing of a thick silicon proof mass with the limited 5 V supply after system start from power down or in the case of over-range input acceleration. The readout chip has been combined with a Silicon-On-Glass lateral accelerometer, which has a high sensitivity of 1.88 pF/g with large proof mass and long finger structures. A digital filtration and decimation circuitry is also implemented to signal process the output bit stream of the readout circuit. The complete module consumes 16 mW from a ±2.5 V supply and has an adjustable sensitivity up to 8 V/g with a noise level of 4.8 μg/$\sqrt{\text{Hz}}$ in open-loop.

Keywords Sigma-delta modulation · Switched capacitor readout circuit · Capacitive sensors · MEMS accelerometer

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1 Introduction

High precision accelerometers with micro-g (μg, $g = 9.8\ \text{m/s}^2$) resolution have many applications, including inertial navigation and guidance, microgravity measurements in space, tilt control and platform stabilization, seismometry, and GPS-aided navigators for the consumer market. Most of these applications require digital output with force-feedback operation, large dynamic range, and high sensitivity with inertial grade resolution. The attractive features of MEMS as applied to inertial systems are its potentially low cost, drastically reduced size and weight, and low power dissipation, all of which are prerequisites for the development of next generation navigation systems. Recently, capacitive accelerometers have become very attractive for high precision μg applications due to their high sensitivity, low temperature sensitivity, low power, wide dynamic range and simple structure. To date, only a few inertial-grade silicon accelerometers have been reported [1–6]. However, none of these have reported a micro-g level resolution together with a large operation range of few g's.

Capacitive accelerometers are required to have a large proof mass, compliant suspensions, and large capacitance sensitivity to increase the acceleration sensitivity. When operated in open-loop, such an accelerometer will have a limited dynamic range and bandwidth. To increase the dynamic range, the accelerometer can be operated in closed-loop by applying an electrostatically-generated

force feedback signal that maintains the proof mass in null position. Recently, Σ-Δ modulation control loops have been used in microaccelerometers to achieve force-rebalancing and obtain a direct digital output [3–5]. A 2nd-order Σ-Δ modulator, with two integrators, one mechanical and one electrical, not only provides a digital output, but also relaxes the accuracy requirements on the analog circuits. In micromechanical accelerometers, since the mechanical bandwidth is usually quite small (<2 kHz), sigma-delta conversion can effectively reduce noise and improve overall performance [7–11].

This paper reports a capacitive interface chip for micro-accelerometers aiming to have high sensitivity and operation range with in a large frequency band. The chip can be used for both open-loop and closed-loop operation of the micro-accelerometer. In the closed-loop mode of operation, the interface chip forms a second-order electromechanical oversampled sigma-delta modulator with the sensor, and provides direct digital output and force feedback of the proof mass simultaneously. The low-pass mechanical transfer function of the accelerometer forms the first integrator loop in this configuration, and the charge integrator front-end provides the second loop integrator function as well. The circuit is specifically designed for high sensitivity capacitive microsensors, with each block optimized to achieve lowest noise and high sensitivity while maintaining a high operation range. The reported circuits for microaccelerometers [1–9] either lack achieving low noise, or operate only for very low acceleration levels. The circuitry reported in this paper achieves a resolution of 3 aF/$\sqrt{\text{Hz}}$ with 115 dB dynamic range in open loop mode, and ±4 g of operation range in closed loop together with the accelerometer. This IC can also be used for other high sensitivity capacitive silicon sensors, such as barometric pressure sensors that require very good dc response as well.

In the following sections, first the micro-g accelerometer is described. Then, the operation of the readout circuit is discussed in detail. Finally, implementation and test results are presented.

2 SOG lateral accelerometer

It has been especially challenging to design precision accelerometers sensitive in lateral axes because of the difficulty in achieving small capacitive gaps over large area. The Silicon-On-Glass (SOG) accelerometer implemented is sensitive in lateral axes, and it is designed for maximum electrical sensitivity and minimum mechanical noise based on the allowable features of the process and device dimensions.

Figure 1 shows the structure of the SOG lateral accelerometer. The sensor is quite simple and utilizes the well-known lateral varying gap comb finger structures for sensing and feedback, except that it has a very large proof mass and sense capacitances because of the large thickness of the device realized using Deep Reactive Ion Etching (DRIE) process. The fabrication process requires only 4 masks. First, a glass substrate is etched to form anchor regions [Fig. 2(a)]. Then, a shielding metal layer is patterned on a 100 μm-thick silicon wafer [Fig. 2(b)]. This layer prevents DRIE notching and acts as a heat sink during DRIE. Next, the silicon and glass wafers are anodically bonded [Fig. 2(c)]. Metal contacts are evaporated and patterned, and finally the wafer is etched with DRIE to define the proof mass and sensing electrodes [Fig. 2(d), (e), (f)]. Then the shielding layer is removed. This process is simple, requires no special steps other than DRIE, and does not require any high-temperature processing. The glass substrate is insulating, which reduces parasitic capacitance, facilitating interfacing with a hybrid readout circuit. Note that the fingers are ∼100 μm tall and the sensing gap is ∼4.5 μm. The large proof mass and long fingers (500 μm) results in a high sensitivity (1.88 pF/g) and low Brownian noise (2.81 μg/$\sqrt{\text{Hz}}$ at atmospheric pressure.) Table 1 shows the fabricated accelerometer parameters.

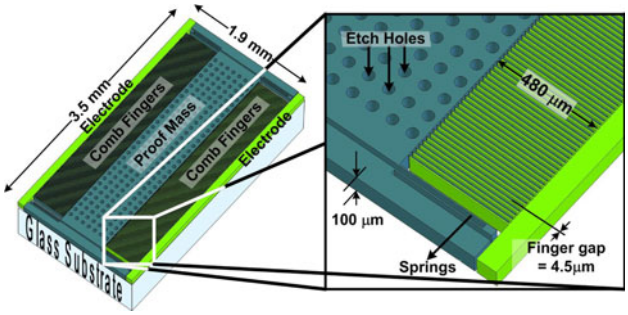

Fig. 1 The structure of the SOG accelerometer

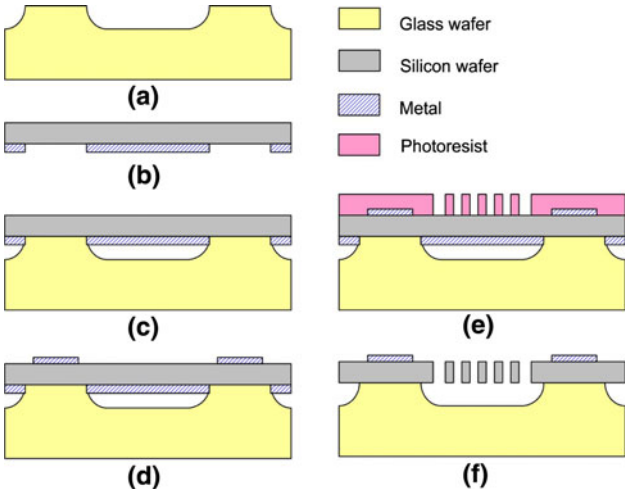

Fig. 2 Fabrication process of the SOG accelerometer

Table 1 Fabricated sensor parameters

Parameter	Value
Mass of proof mass	0.72 milli-g
Resonant frequency	1.53 kHz
Proof mass thickness	100 μm
Sensing gap	4.48 μm
Sense capacitance	24.8 pF
Sense fingers length	500 μm
Number of fingers	290
Sensitivity	1.88 pF/g
Brownian noise	2.81 $\mu g/\sqrt{Hz}$

3 Interface electronics

For measuring the acceleration signals from the accelerometer sensor, a capacitive readout circuit is designed and implemented. The readout circuit forms a fully differential switched capacitor Σ-Δ modulator together with the sensor. The circuit can operate either in open-loop or closed-loop mode. In open-loop, the capacitance difference of the accelerometer is measured, and the output is generated as an analog voltage with a high sampling rate of 500 kHz. In this case, the output is proportional to the capacitance difference, and it can be assumed linear only for small displacements of the proof-mass. Therefore, linear range of the system is limited in open-loop. In the closed-loop case; the output is a one-bit Pulse Density Modulated (PDM) digital stream and it is applied as an electrostatic feedback voltage to the proof mass to hold it stationary independent from the incoming acceleration. In other words, the proof mass is not moving at all during the operation and hence the linear range is extended significantly.

Circuit noise is one of the most critical parameter affecting the overall system performance. Quantization is an important noise component for closed-loop accelerometers with digital output. In Σ-Δ approach, quantization noise is shaped and transferred to high frequencies, since sampling rate is much higher than the Nyquist frequency of the signal. Therefore, the quantization noise remaining in the signal bandwidth is greatly reduced. The remaining high frequency quantization noise can then be eliminated with a digital processing stage including low pass filtration and decimation. When the system is operated with a clock frequency of 500 kHz, it achieves a high over-sampling ratio of about 500 for a sensor bandwidth of 500 Hz. The closed-loop operation improves the system linearity, quantization noise, range and the bandwidth.

Figure 3 shows the detailed schematic view of the readout electronics which has four main blocks: the switched capacitor front-end, start-up, bias generator, and clock generator. The front-end circuit includes the switched capacitor network, the operational transconductance amplifier and a comparator. The circuit generates an output voltage proportional to the sensor capacitance difference. The detailed operation of this block is as follows: The sensor is connected to fixed reference capacitors to form a

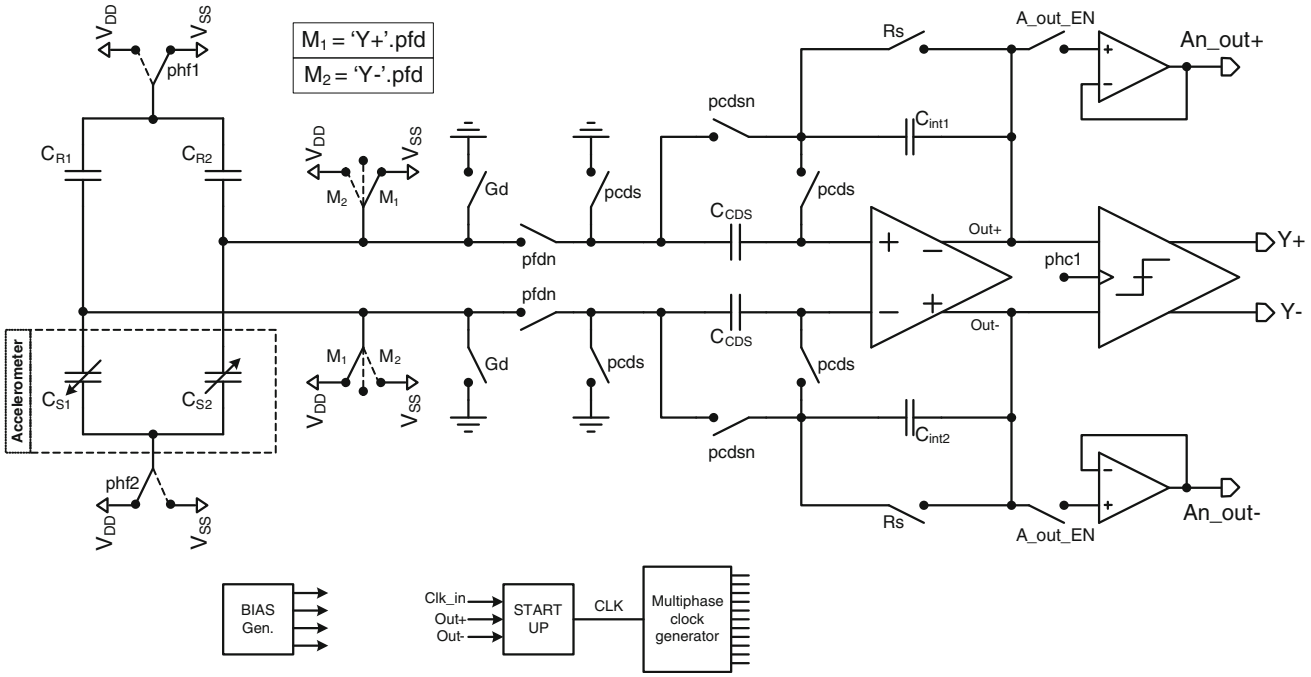

Fig. 3 Schematic of the sigma delta readout circuit

full bridge configuration. The main phases of operation of the circuit are the sense phase and the feedback phase. In the sense phase, when 'phf1' and 'phf2' signals change state, the sense and reference capacitors are charged to new voltage values, and the charge difference, arising from the sensor capacitance difference, is transferred to the charge integrator.

The operational trans-conductance amplifier (OTA) used in the charge integrator is a critical component for the sampling rate and noise considerations. For this purpose a folded cascode fully-differential OTA is designed as seen in Fig. 4. This structure utilizes high power supply rejection ratio, high gain and low noise. A simplified noise formula for the folded cascode OTA can be shown as in Eq. (1). Hence, in order to decrease the thermal noise of the amplifier, the input transistors M1 and M2 are designed to have large widths, while the transconductance of transistors M5, M6, M7, M8, M13 and M14 are held small. There is a trade off between noise and the speed of the amplifier for setting the widths of the input transistors. Increasing width of the input transistors increases the gate capacitances and hence, decreases the slew rate and the unity gain frequency of the amplifier. Also, decreasing noise results in higher currents in the branches; therefore increases the power dissipation of the circuit. A high slew rate, low noise, low power dissipation OTA was designed considering all these requirements and tradeoffs.

$$V_n^2 = 8kT\left(\frac{2}{3g_{m1,2}} + \frac{2\left(g_{m5,6}+g_{m7,8}\right)}{3\left(g_{m1,2}\right)^2} + \frac{2g_{m13,14}}{3\left(g_{m1,2}\right)^2}\right) \quad (1)$$

The OTA also includes a common mode feedback circuitry, in order to set the common mode voltage at the output. The common mode feedback circuitry makes use of the transistors operating at deep triode region.

The integrator output is then given to the latching comparator, the schematic of which is given in Fig. 5. The

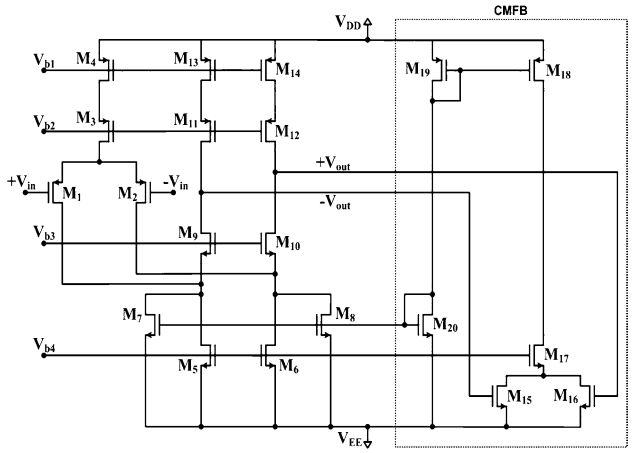

Fig. 4 Circuit schematic of the fully differential folded cascode OTA

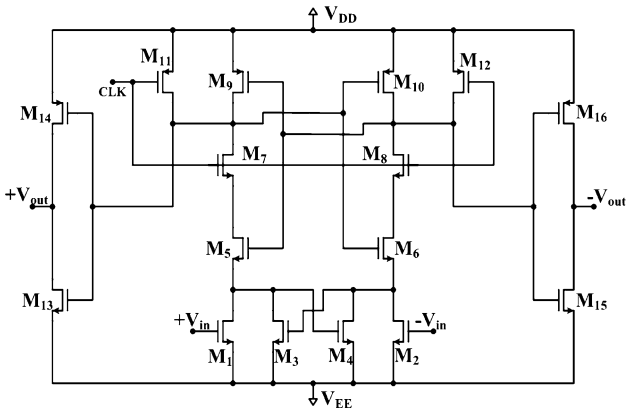

Fig. 5 Circuit schematic of the latching comparator

comparator generates a one-bit PDM for electrostatic force-feedback at the rising edge of the applied clock signal, and holds it during the feedback phase. In this phase, a 5 V potential difference is applied between one of the electrodes and the proof mass to provide pulling. Besides pulling the proof mass to its rest position, this PDM bit stream is also used as the closed-loop system output. While applying the feedback force to the sensor, integration capacitors are reset for the next cycle. Correlated Double Sampling (CDS) technique is utilized in the front-end for flicker (1/f) noise and offset reduction, by storing these non-idealities in the CDS capacitors in the feedback phase and subtracting from the measured signal.

The other blocks used in the readout circuit are the bias generator, start-up and multiphase clock generator circuits. The bias generator block generates the bias voltages for the folded cascode OTA used in the charge integrator, and for other amplifiers used in the circuit. The start-up circuit is also needed for avoiding high accelerations and deflections of proof mass at the start up of the system. Another major block is the multiphase clock generator, which supplies various clock signals with various duty cycles and phases to provide proper switched capacitor operation.

4 Modeling and simulation

The overall system including the accelerometer sensor and the readout circuit is an electromechanical system. Hence the model of the system should include both electrical models and the mechanical models, to verify the operation of the system and its stability. For this purpose, an electromechanical model is constructed in MATLAB Simulink environment, as the block diagram shown in Fig. 6. The parameters used for the accelerometer model are selected for the lateral SOG accelerometer. The damping ratio of the sensor is calculated for the atmospheric pressure, as the squeeze film damping of the finger structures. An interface

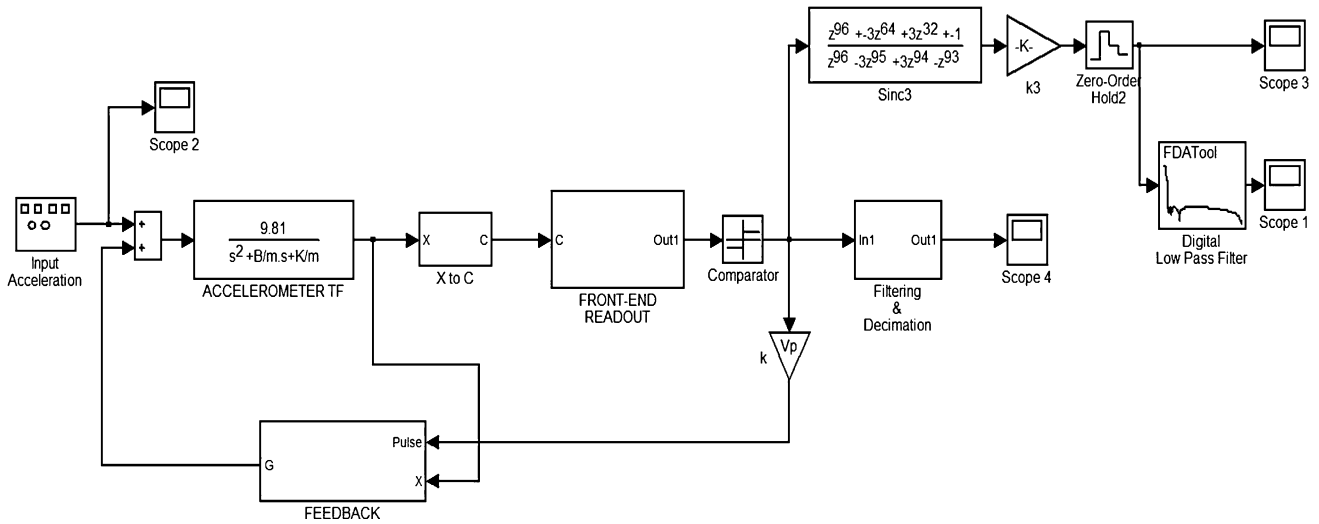

Fig. 6 Simulink Model of the accelerometer system including digital filtration and decimation blocks

block is also implemented for converting the mechanical proof mass displacement data to differential capacitance value generated in between the sensor fingers. The capacitance data is then given to the model of the front-end readout circuit, which includes a charge integrator circuit, and hence the model generates output voltage values depending on the input capacitance difference value. The front-end readout circuit is modeled including the output saturation voltages and charge integrator capacitance variations, coherent with the timings of the circuit. After this stage, a comparator generates the digital data according to the input analog voltage supplied from the front-end readout circuit. The digital output from the comparator, should be applied to the accelerometer as a feedback. Hence, a feedback block is required for calculating the feedback forces according to the sensor parameters and the instantaneous position of the proof-mass. In this way, the model for the accelerometer system is generated, but the output of this system is a bit stream and should be signal processed by filtration and decimation stages, to extract the high resolution acceleration data at the Nyquist sampling rate.

To perform the processing of the data, two models are given. One of these models is the "Filtration & Decimation" block as shown in the system model in Fig. 6. This model uses three stages of cascaded filtration and decimation stages, to obtain the desired Nyquist sampling rate with precise low pass filtering. Three stages are used for gradually decreasing the sampling frequency and for using lower order low-pass filters and hence reducing the processor time. This model uses the digital filtering toolboxes of MATLAB and hence provides high-quality filtering, but requires high performance digital signal processors for realization.

Another model, which is much more realizable and affords a similar performance with the prior model, is also given in the model of the system in Fig. 7. This model uses a Sinc^3 filter which both decimates and filters the data. Sinc filters have the advantage of simplicity in implementing, since it does not include any multiplication blocks, but it is composed of only summation and difference blocks. The optimum order of the decimation filter is selected as 1 more than the order of sigma-delta modulator [12]. Hence, for the second order sigma-delta structure, a third order sinc filter is used. The Sinc^3 filter is composed of 3 stages of integration and 3 stages of differentiation stages. In the integration stage, the data rate is the same as the data rate of the output bit stream, which is 512 kHz, but it is decimated to 2 kHz using a sampler and the data rate is reduced for the differentiation stage. The Sinc^3 filter is not a high quality low pass filter and also passes some of the higher frequency signals, so a basic low pass filtration would be required following the Sinc^3 filter stage. Hence at the output of the low-pass filter, decimated and filtered, high resolution data is obtained. Using the Sinc^3 filter with the

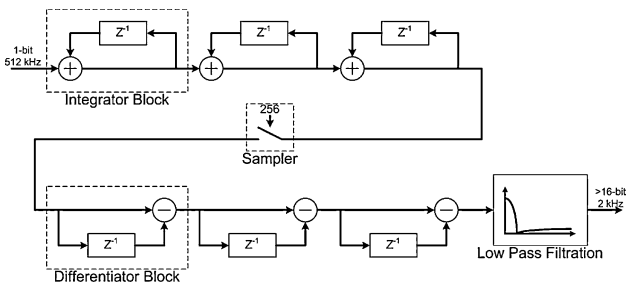

Fig. 7 The structure of the filtration and decimation block including sinc^3 decimation filter and the low pass filtration

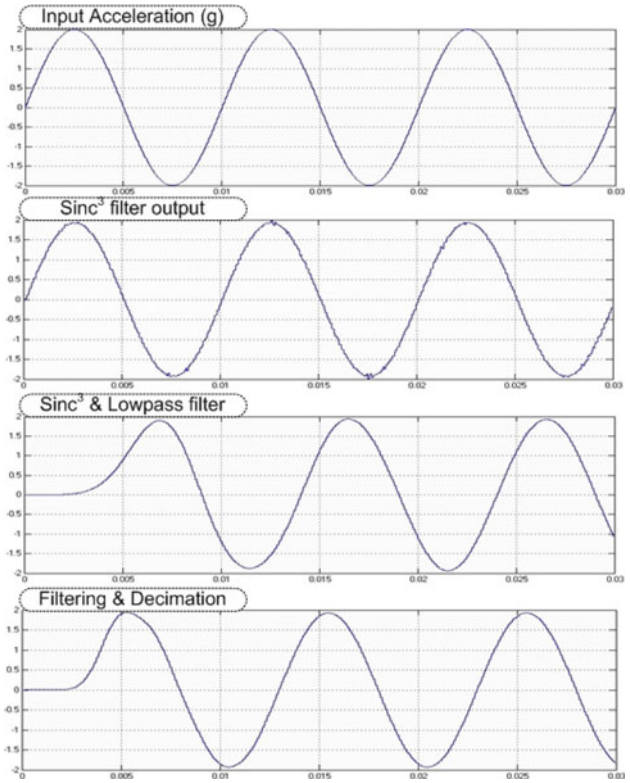

Fig. 8 Simulation results of the MATLAB Simulink model, with different filtering structures

basic low pass filter stage results in a similar performance with the model implemented using the toolboxes of MATLAB. The Sinc^3 model was also realized and tested with the accelerometer and the readout circuit, which will be discussed in Sect. 5.

The simulation results of the system model are given in Fig. 8, which verifies the system operation and stability. The simulations were performed using the accelerometer parameters given in Table 1, and an input acceleration of 2 g amplitude at 100 Hz is applied. After processing the 1 bit signal with the Sinc^{3}filter, the acceleration signal is obtained. But this signal includes some higher frequency components. These high frequency signals are eliminated by using a low pass filter, which has a low order and basic structure. In this way, similar performance is obtained with the filtering and decimation block, which uses sharp filters and decimation stages, hence difficult to be realized.

5 Implementation and test results

The accelerometer readout circuit was designed in XFab 0.6 μm two-metal, two-poly CMOS process. The die photograph of the fabricated chip is given in Fig. 9. The chip occupies an area of 2.4 × 1.2 mm^2 including the

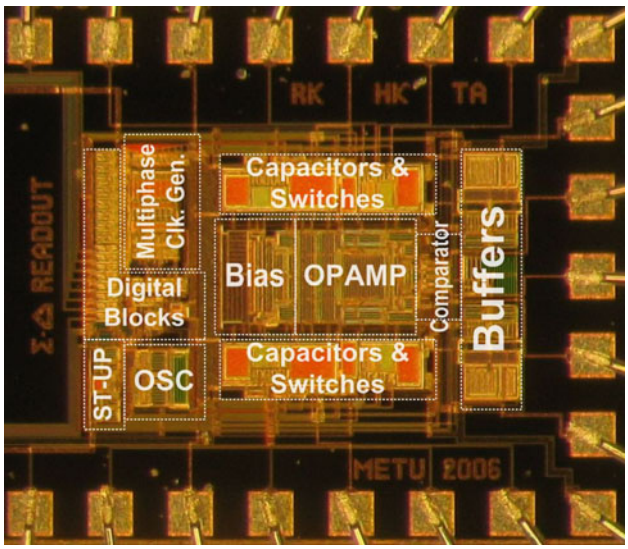

Fig. 9 The die photograph of the readout circuit chip

pads, and has 38 input/output pads, most of which are used for testing purposes. The tests for each block are performed, and the functionalities are verified. The circuit operates with ±2.5 V power supply, having 16 mW of power consumption and can operate with a clock signal up to 750 kHz. The chip is able to be operated with either an internally generated 500 kHz clock signal from an on-chip oscillator or an externally applied clock signal. The reference capacitors, whose values can be controlled digitally, are implemented on chip for constituting the full bridge structure with the sensor capacitances. The on-chip integration capacitors are also made digitally adjustable in a range of values, for testing purposes. The selection of the integration capacitors allows adjustable differential sensitivities in the range between 0.3 and 5 V/pF.

Figure 10 shows the manufactured PCB for the accelerometer system. The chip is wire-bonded to a 44-lead SMD package, and the PCB is designed and manufactured for the testing of the readout circuit. The accelerometer sensor is also wire bonded on the PCB, and both the sensor and the chip are shielded to isolate the system from the external noise sources. The shielding is removed in Fig. 10 for illustration purposes.

Open-loop tests are performed on the hybrid accelerometer system. DC input acceleration is applied to the system in the range of ±1g with a turn table, and the differential analog output voltage is measured at various values of integration capacitance values. Figure 11 shows the results of these tests, showing that the system has an adjustable sensitivity between 0.8 and 8 V/g with the changing integration capacitances. For integration capacitance selected as 4 pF, the open-loop sensitivity is measured to be 2.36 V/g.

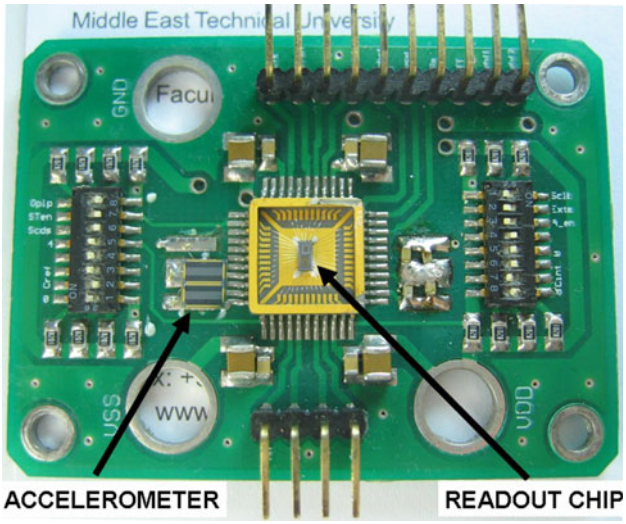

Fig. 10 Accelerometer system

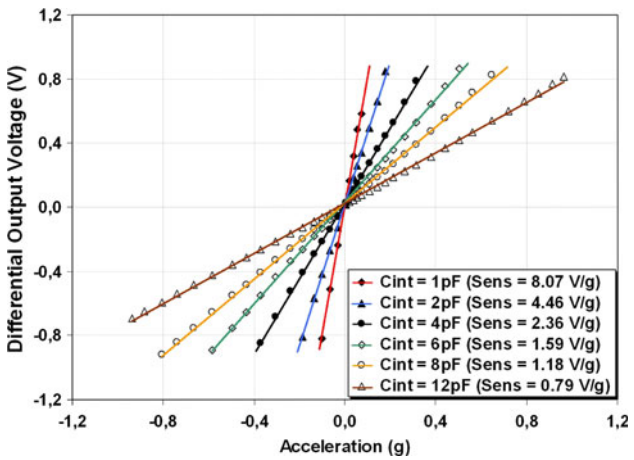

Fig. 11 Open-loop test results with different C_{int} values

Figure 12 gives the open-loop noise test results both for the readout circuit itself and the total system. Open-loop noise tests are performed in a faraday cage and the circuit was supplied by independent batteries, to minimize the external noises. The open-loop noise of the readout circuit is measured as 810 nV/$\sqrt{\text{Hz}}$ resulting in 1.22 μg/$\sqrt{\text{Hz}}$ noise level. This noise level provides 115 dB dynamic range (DR) and a minimum resolvable capacitance of 2.2 aF for the readout circuit with 4 pF integration capacitance. The total system has 4.8 μg/$\sqrt{\text{Hz}}$ noise level, corresponding to 105 dB of dynamic range with the ±0.4 g linear range. A 560 kΩ resistance noise is also measured and illustrated in Fig. 12 for exhibiting a reference noise value.

For the closed-loop tests of the system, the acceleration signal should be obtained by processing the pulse density modulated output bit stream. As the first step, the system is

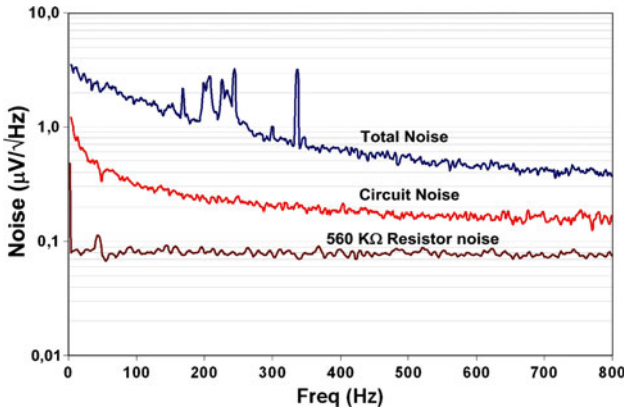

Fig. 12 Open-loop noise test results

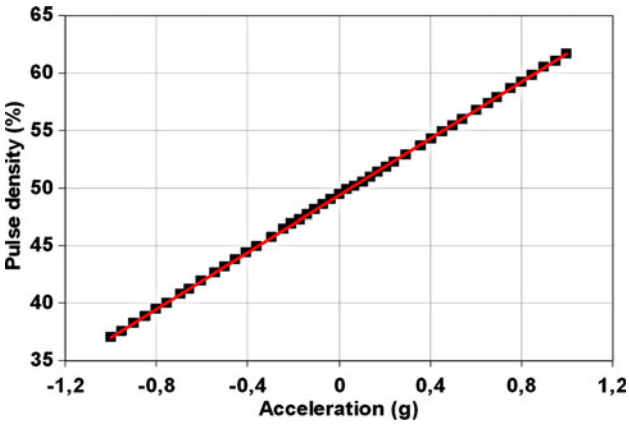

Fig. 13 Closed loop output pulse density versus input acceleration

placed on a turn table and constant acceleration is applied and the output data is collected for a period of time, at several angles. Then for obtaining the value of acceleration, the pulse density of the collected data is calculated. This test is performed for values of accelerations covering ±1 g. Figure 13 shows the percentage of the output pulse density versus applied acceleration indicating a 12.5%/g scale factor, with a high linearity. So the total range of the closed-loop system can be calculated as ±4 g.

Next, the system is placed on a rate table and a sinusoidal acceleration is applied on it. The pulse density modulated digital bit-stream at 500 kHz is collected using a data acquisition board. The data is then processed by the software implemented in MATLAB to perform digital filtration and decimation of the digital data. Figure 14 shows the filtered and decimated outputs for applied sinusoidal accelerations at 10 Hz with peak-to-peak amplitudes of 70, 140 and 210 mg.

After obtaining the filtration and decimation of the data in MATLAB environment, the Sinc^3 filter is realized using microcontrollers. The microcontrollers process the output bit stream using a sinc^3 filter, which realizes both

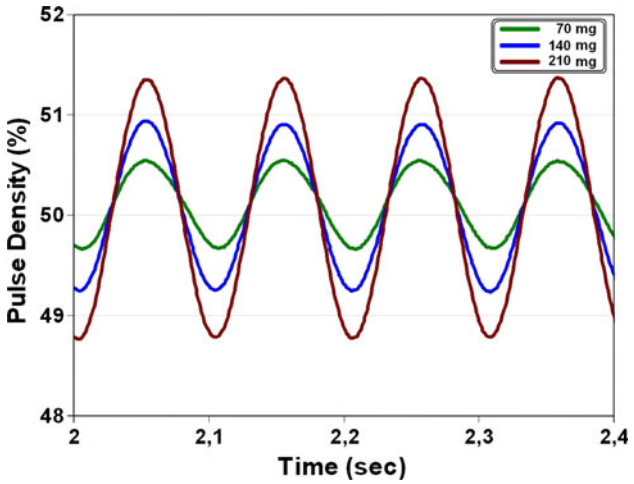

Fig. 14 Filtered and decimated closed-loop output for various amplitude sinusoidal inputs at 10 Hz

Table 2 Test results of the CMOS interface readout circuit and the hybrid micro-accelerometer system (with $C_{int} = 4$ pF)

Parameter	Value
Circuit sensitivity	1.3 V/pF
Circuit noise (open-loop)	1.22 μg/$\sqrt{\text{Hz}}$
Minimum resolvable capacitance	2.2 aF/$\sqrt{\text{Hz}}$
Brownian noise	2.81 μg/$\sqrt{\text{Hz}}$
Sensitivity	2.36 V/g
Noise (open-loop)	4.8 μg$\sqrt{\text{Hz}}$
Open-loop dynamic range	105 dB
Close-loop linear operation range	±4 g

decimation and filtering. Another digital low-pass filtration stage is also implemented using microcontrollers after the sinc^3 filter, for further elimination of the high frequency components. Hence, the complete system, including the digital processing of the output bit stream is realized on a PCB. The tests of the circuit are performed using the filtration and decimation stage and the operation is verified.

Table 2 shows the overall test results summary of the readout circuit.

6 Conclusion

This paper reports a high-sensitivity, low-noise, closed-loop capacitive accelerometer system with micro-g resolution. The system operates as a 2nd-order electromechanical sigma delta modulator together with the interface electronics. The system can be operated in open-loop for analog readout or in closed-loop to obtain digital output in the form of pulse density modulated bit stream. The hybrid system has been tested in both open and closed-loop mode with the digital filtration and decimation circuitry. The complete module consumes 16 mW from a ±2.5 V supply and has an adjustable sensitivity up to 8 V/g with a noise level of 4.8 μg/$\sqrt{\text{Hz}}$ in open-loop. The analog readout circuit uses the Correlated Double Sampling technique to reduce the flicker noise and the offset and the circuit components are designed to have minimum level of noise. Hence, the circuit achieves 115 dB DR and 2.2 aF/$\sqrt{\text{Hz}}$ capacitance resolution by itself and 105 dB DR with the accelerometer sensor in open-loop. The linear range is ±0.4 g in open-loop (with $C_{int} = 4$ pF) and ±4 g in closed-loop.

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