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A LOW COST UNCOOLED INFRARED MICROBOLOMETER FOCAL PLANE ARRAY USING THE CMOS N-WELL LAYER

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ABSTRACT

This paper reports a low-cost, 256-pixel uncooled infrared microbolometer focal plane array (FPA) implemented using a 0.8µm CMOS process where the n-well layer is used as the active microbolometer material. The suspended n-well structure is obtained by simple front-end bulk etching of the fabricated CMOS dies, while the n-well region is protected from etching by electrochemical etch-stop technique within a TMAH solution. Electrical connections to the suspended n-well are obtained with polysilicon interconnect layer instead of aluminum to increase the thermal isolation of the pixel by an order of magnitude. Since polysilicon has very low TCR and high resistance, the effective TCR of the pixel is reduced to 0.34%/K, even though the n-well TCR is measured to be 0.58%/K. A 16x16 pixel array prototype with 80µmx80µm pixel sizes has successfully been implemented. The pixel resistance measurements show that pixels are very uniform with a nonuniformity of 1.23%. Measurements and calculations show that the detector and the array provide a responsivity of 1200V/W, a detectivity of 2.2×10^8cmHz$^{1/2}$/W, and a noise equivalent temperature difference (NETD) of 200mK at 0.5Hz frame rate with fully serial readout scheme. This performance can be further increased by using other advanced readout techniques, therefore, the CMOS n-well microbolometer approach seems to be a very cost-effective method to produce large focal plane arrays for low-cost infrared imaging applications.

INTRODUCTION

Uncooled infrared detectors have recently gained wide attention for infrared imaging applications, due to their advantages such as low cost, low weight, low power, large spectral response, and long term operation compared to those of photon detectors. The general trend is to implement these detectors monolithically with CMOS readout electronics to achieve low cost infrared detector arrays, where post-CMOS surface or bulk micromaching are usually used to merge detectors with readout electronics.

Surface micromachined uncooled detectors are mostly based on microbolometer approach, where infrared radiation heats the sensor material, changing its resistance related to its temperature coefficient of resistance (TCR). This approach allows the implementation of small pixel sizes, such as 50µmx50µm, but these detectors usually require deposition of some exotic materials with high TCR after CMOS fabrication, complicating post-CMOS processing and increasing its cost. For example, vanadium oxide (VO_x), the most widely known and used microbolometer material, has a high TCR of about 2-3%/K [1]; however, VO_x is not a standard material in IC fabrication and requires dedicated expensive equipment. IC compatible materials such as amorphous silicon carbide [2] and polycrystalline silicon-germanium [3] have also high TCR values of 4-6%/K and 2-3%/K, respectively. However, these materials require high temperature annealing, which is not suitable for post-CMOS processing for monolithic integration unless a different material than aluminum is used. A low temperature and IC compatible approach is to implement microbolometers using metal films [4], but metals have very low TCR in general. Therefore, although surface micromachined microbolometers are very cheap compared to photon detectors, their prices are still high for many commercial applications.

Bulk micromachined uncooled detectors are mostly based on thermoelectric sensors [5, 6]. Implementation of these detectors does not require complicated processes, since the devices can be obtained by front or back-end bulk micromachining of CMOS fabricated dies. However, the responsivity of the thermopiles are very low, in the order of 5-15V/W, and the pixel sizes in these devices are large, such as 250µmx250µm, limiting their use for large detector arrays. When back-end bulk micromaching is used, these detectors also require extra processing for thermal isolation between pixels, such as processing steps to obtain silicon islands [5] or electroplated gold lines [6]. Although there are successful implementations of thermopile arrays, their low responsivities and large pixel areas limit their performance and application areas.

Another possible approach is to implement microbolometers by bulk-micromachining of standard CMOS fabricated dies to achieve very low cost detectors with reasonable performance, and we have shown the implementation of such an infrared detector by using the CMOS n-well layer as the sensitive bolometer material [7]. The n-well layer is selected due to its relatively high TCR of 0.5-0.65%/K. This paper reports the implementation of a 16x16 uncooled microbolometer array prototype using the n-well microbolometer approach. The pixel size in the array is 80µmx80µm, which is close to surface micromachined approach, and the performance of the detector array is higher than CMOS bulk-micromachined thermoelectric approach.

N-WELL MICROBOLOMETER STRUCTURE

Figure 1 shows a perspective view of the n-well microbolometer that can be obtained with any standard CMOS process. Infrared radiation heats the absorbing layer on the thermally isolated n-well, increasing its temperature, which in turn results in a change in its resistance related to its TCR. The bulk silicon under n-well is etched away to reduce thermal conductivity and to increase responsivity of the detector. This thermally isolated suspended structure is obtained by front-end bulk etching of fabricated CMOS dies in TMAH, while using the electrochemical etch-stop technique to prevent the etching of the n-well [8, 9].

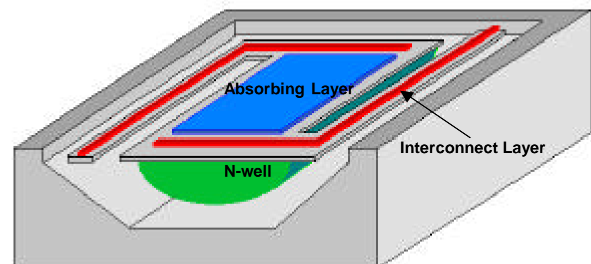

Figure 1. *Perspective view of the n-well microbolometer.*

The performance of the n-well microbolometer pixel is affected by a number of design parameters and material characteristics, including interconnect layer on the support arms, pixel size, opening and support arm widths, fill factor, and the absorbing layer. The interconnect layer on the support arms should have low thermal conductance to increase its pixel thermal isolation and should have low resistance to reduce its negative contribution to the noise and TCR of the pixel since it comes series with the sensitive resistance sensor material. The support arms should be as long as possible and as thin as possible to reduce its thermal conductance, but at the same time they should not be fragile. There are two alternatives for interconnect layer: the metal and polysilicon layers. The metal layer has a low electrical resistivity, therefore, the pixel noise and TCR are mainly determined by the n-well layer. However, metal has a high thermal conductance, resulting in a poor thermal isolation of the sensor material. Unlike metals, the polysilicon layer has a high electrical resistance resulting in an increased noise contribution and reduced overall pixel TCR. On the other hand, polysilicon layer has lower thermal conductance, providing an order of magnitude better thermal isolation according to ANSYS FEM simulations. Hence, we have decided to use polysilicon as the interconnect layer.

The pixel size and fill factor are determined by process limitations, such as the minimum interconnect width and opening between the arms that allow silicon to be exposed to the solution during etching. In our previous studies [7], we have demonstrated that it is possible to implement 50µmx50µm pixel sizes with 25% fill factor using a 0.8µm CMOS process. These pixels have 4µm opening widths, and due to this small size, some metal residues are left on the openings. Cleaning of these residues is possible with additional post processing steps. To prevent these steps and to increase the etching yield of array pixels, we have decided to increase the opening widths to 10µm, resulting in a 74µmx74µm pixel size. When the area for the routing is included, the final pixel size of the array became 80µmx80µm with a fill factor of 13%. The pixel size and the fill factor can be improved with the advanced CMOS processes and structures.

The absorbing layer is necessary on top of the n-well layer since silicon is transparent to infrared radiation [10]. In this study, we have used a sandwich layer composed of oxide-metal-passivation layers as absorber layer which provides an average absorptance of about 33% in the 8-14µm band according to simulations obtained by the Kidger Optics software.

ARRAY DESIGN AND ETCHING

A 16x16 n-well microbolometer array has been implemented as an initial prototype to demonstrate its feasibility. Figure 2 shows the block diagram of array readout circuitry, which is composed of vertical and horizontal shift registers, a controller, and an 8-bit synchronous counter. In this small size array, serial readout approach was selected for simple implementation. Figure 3 shows the schematic view of the electronic pixel connection inside the array, including the circuitry used for etching process. Each pixel is connected to the output by sequentially switching the column and row signals. To simplify the readout scheme and to reduce the number of interconnects, pixels include built-in diodes, eliminating the need for MOS switches within pixels. When a row is selected, the bias voltage is applied to all pixels in that row, but only the selected column allows for current flow. During this time, no signal comes from the other rows, since the diodes of the unselected rows remain off, providing signal isolation.

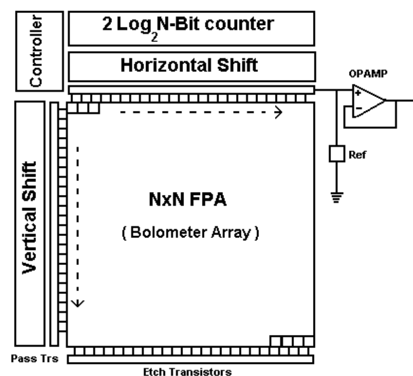

Figure 2. *Block diagram of n-well microbolometer array readout circuitry, which is based on serial readout approach.*

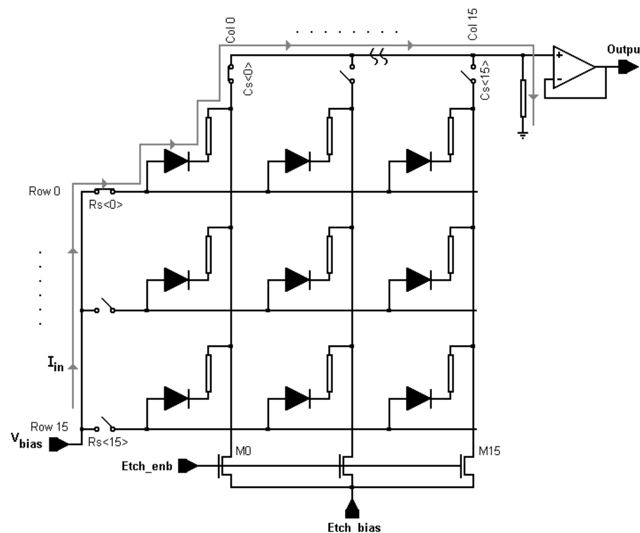

Figure 3. *Schematic view of the electronic pixel connection inside the array, including the circuitry used for post processing.*

Figure 3 also shows the electronic circuitry used during etching. The n-wells of the array need to be connected to passivation potential during etching, but they need to be isolated during normal operation. This is achieved by turning on transistors M_0-M_{15} to apply the etch potential to all n-wells. After etching is completed, *Etch_enb* and *Etch_bias* pins are shorted to isolate the n-wells between columns [11]. As explained before, the isolation of rows is achieved by built-in diodes in the n-well.

The post-CMOS etching of n-well microbolometer array includes the etching of bulk silicon substrate and releasing n-well to achieve thermal isolation. The details of the post-CMOS etching is given elsewhere and will not be repeated here [9], but some of the important points are summarized below. Anisotropic etching is done in a Tetramethyl Ammonium Hydroxide (TMAH) solution using electrochemical etch-stop technique to prevent the etching of the n-well layers. In order to achieve high silicon etch rate, a 5wt.% TMAH solution at 85°C is used. Hillock formation in this low concentration TMAH is overcome by adding proper amount of ammonium peroxidisulfate into the solution. Enough silicon is also dissolved in the solution to prevent the etching of aluminum pads. It should be noted here that the open circuit potential (OCP) for the bulk silicon changes with the concentration of the TMAH solution [12], hence measurement of OCP is necessary before the application of electrochemical etch-stop.

FABRICATION AND TEST RESULTS

A 16x16 n-well microbolometer test array has been designed and fabricated using the AMS 0.8μm CMOS process. Figure 4 shows the SEM pictures of the fabricated and post processed array die verifying that all n-well structures are thermally isolated from the substrate and remain flat due to the stress compensated silicon dioxide and silicon nitride composite layers. None of the support arms are broken, and the etching yield of 100% is achieved. It should be noted that the bulk silicon regions between the suspended n-wells reduce the thermal cross talk between pixels, eliminating the need for gold stripes or silicon islands between the pixels which have been used in other approaches [5, 6].

A number of electrical tests have been performed to verify the operation of the readout circuitry and to measure the pixel uniformity. The scanning circuit is measured to operate at a frequency as high as 15MHz, which allows its use even in very large FPAs. To verify pixel uniformity, the resistance values of the individual pixels were measured. Figure 5 and Figure 6 show the resistance measurement results and the histogram plot of the 256 pixels, respectively, verifying their high uniformity. The mean value of the pixel resistances is 8.37kΩ with a standard deviation of 103Ω and a nonuniformity of 1.23%.

Thermal measurements were also performed to characterize the thermal conductance and TCR of the pixels used in the array. The thermal conductance of the structure is determined as 6.2×10^{-7} W/K. The TCR of the n-well is measured as 0.58%/K, however, the effective TCR of the pixel in the array results in a smaller value than the n-well TCR, due to the low TCR polysilicon interconnect layer that comes in series with the n-well resistance. The TCR of the n-well microbolometer structure with polysilicon interconnects is both calculated and measured as 0.34%/K in a separate test pixel, but effective TCR of the pixel array is further reduced to about 0.24%/K due to negative temperature coefficient of voltage of the built-in diode.

A model is derived to analyze the reduction in responsivity due to the polysilicon resistors and the built-in diode. Figure 7 shows the model of the n-well microbolometer biasing circuit, and Equation 1 gives the responsivity derived using the circuit parameters.

$$\Re = \frac{\eta V_{bias_eff} R_{ref}}{G_{th} R_{total}} \left[\frac{1}{V_{bias_eff}} \frac{dV_D}{dT} + \frac{2R_{poly}}{R_{total}} \alpha_{poly} + \frac{R_{nwell}}{R_{total}} \alpha_{nwell} \right] \quad (1)$$

$$V_{bias_eff} = V_{bias} - V_{D,on}$$

$$R_{total} = 2R_{poly} + R_{nwell} + R_{ref}$$

where, η is absorptance, G_{th} is thermal conductance, R_{ref} is reference resistance, R_{nwell} is n-well resistance, R_{poly} is polysilicon resistance in each arm, α_{nwell} is TCR of n-well layer, α_{poly} is TCR of polysilicon layer, V_{bias} is bias voltage, and $V_{D,on}$ is diode turn-on voltage.

The equation shows that, for a fixed η, V_{bias_eff}, and G_{th}, the responsivity is maximized when R_{nwell} is made much larger than R_{poly} and when R_{ref} is selected equal to the total pixel resistance. The equation also shows that the reduction in the responsivity occurs due to the diode since the term dV_D/dT that comes from the diode is negative with a typical value of -2mV/K.

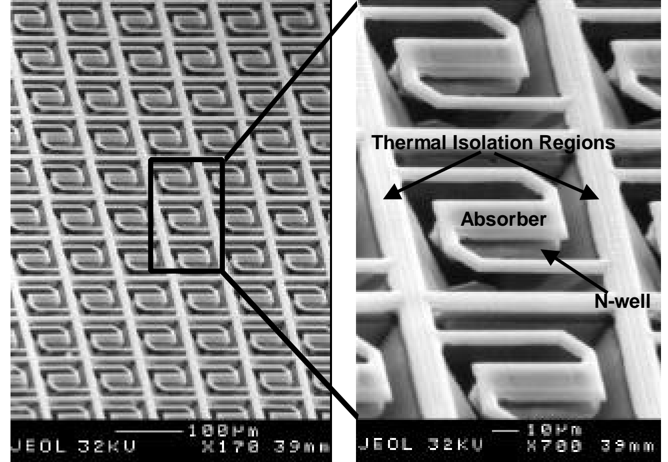

Figure 4. *SEM picture of the fabricated and post processed 16x16 n-well microbolometer array.*

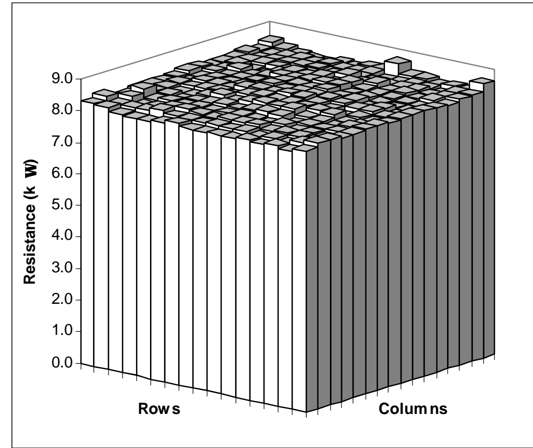

Figure 5. *N-well microbolometer pixel resistance values.*

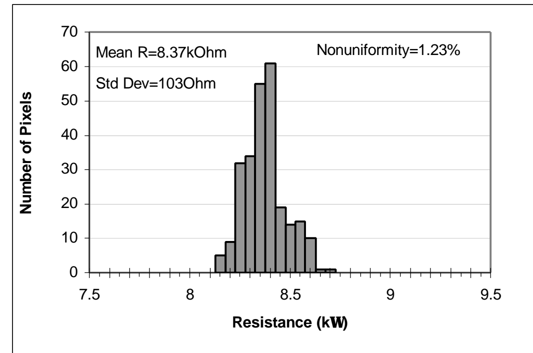

Figure 6. *Histogram plot of the 16x16 pixel resistance values. The mean value of the pixel resistances is 8.37k*Ω with a *standard deviation of 103Ω and a nonuniformity of 1.23%.*

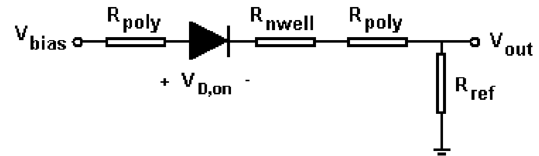

Figure 7. *Model of the n-well microbolometer biasing circuit.*

The noise of the pixel is also negatively affected by the polysilicon resistances. The dominant noise in the pixel is measured to be the thermal noise coming from the n-well and polysilicon layers. N-well 1/f noise and diode shot noise are negligible, since n-well is single crystal and the diode internal resistance is low compared to the detector and reference resistances. The overall noise voltage at the output is found as 0.12µV for 0.5fps scanning rate, which is expected to result in an NETD value of 200 mK. It should be noted here that self-heating effects at the output is reduced by using the suspended reference resistor which is included in the fabricated die. Table 1 summarizes the device parameters and performance results of the n-well microbolometer array.

Table 1. *The summary of device parameters and performance results of the n-well microbolometer array.*

Parameter	Value
Process	AMS 0.8µm CMOS
Array Size	16x16
Pixel Size	80µmx80µm
Fill Factor	13%
Absorbance	33%
Total Pixel Resistance	8.4kΩ
Thermal Conductance	$6.2x10^{-7}$W/K
Responsivity	1200 V/W
Detectivity	$2.2x10^{8}$ cmHz$^{1/2}$/W
NETD*	200mK @ 0.5fps

*Expected.

CONCLUSIONS

A 16x16 n-well microbolometer test array has been designed and fabricated using the AMS 0.8µm CMOS process. The suspended n-well structures are obtained by front-end bulk etching of the fabricated CMOS dies, while the n-well region is protected from etching by electrochemical etch-stop technique using a TMAH solution. Tests in the fabricated die show that the readout circuitry are fully functional and all of the 256 pixels are operational. The resistance measurements in these pixels show that the suspended structures are very uniform with a nonuniformity of 1.23%. Although the TCR of the n-well is measured to be 0.58%/K, the effective TCR of the pixel is reduced due to the polysilicon interconnect and built-in diodes in individual pixels. Therefore, the overall responsivity and the detectivity in the array is not as high as the single pixel microbolometer detector developed before [7]; the responsivity and detectivity are obtained as 1200V/W and $2.2x10^{8}$ cmHz$^{1/2}$/W. Although these values are lower than surface micromachined microbolometers, they are higher than the bulk-micromachined CMOS thermopile arrays (Table 2). In addition, the pixel size of the n-well microbolometers is 80µmx80µm, resulting in a small chip size and allowing large FPA arrays. The final device is obtained by a simple etch step after the CMOS fabrication, without requiring extra processes for the thermal isolation between the pixels; therefore, the device cost is very low. Considering the fact that advanced readout techniques and improved pixel structures can further increase the performance of the array, the CMOS n-well microbolometer technique seems to be a promising approach to implement very low-cost uncooled infrared detector arrays with reasonable performance.

Table 2. *Comparison of CMOS n-well microbolometer detector array with post-CMOS bulk-micromachined thermopile arrays.*

Parameter	Ref. [5]	Ref. [6]	N-well
Process (CMOS)	3µm	1µm	0.8µm
Array Size (# of pixels)	32x32	10x10	16x16
Pixel Size (µm^2)	375x375	250x250	80x80
Chip Size (mm^2)	16x16	5.5x6.2	2.1x2.1
Responsivity (V/W)	15	4	1200
Detectivity (cmHz$^{1/2}$/W)	$1.6x10^{7}$	$1.56x10^{7}$	$2.2x10^{8}$
NETD	500mK* @6.7fps	320mK @0.5fps	200mK* @0.5fps

*Expected.

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REFERENCES

1. R.A. Wood, "Uncooled Thermal Imaging with Monolithic Silicon Focal Arrays," *Infrared Technology XIX Proc. SPIE*, 2020, 322 (1993).
2. T.Ichihara, Y. Watabe, Y. Honda, and K. Aizawa, "A High Performance Amorphous Si1-xCx:H Thermistor Bolometer based on Micro-machined Structure," *Int. Conf. On Solid-State Sensors&Actuators (TRANSDUCERS'97)*, Chicago, Illinois, 6/16-19/97, (1997), pp. 1253-1256.
3. S. Sedky, P. Fiorini, K. Baert, L. Hermans, and R. Mertens, "Characterization and Optimization of Infrared Poly SiGe Bolometers," *IEEE Transactions on Electron Devices*, 46, 675 (1999).
4. J.S. Shie, Y.M. Chen, M.O Yang, and B.C.S. Chou, "Characterisation and Modelling of Metal-Film Microbolometer," *J. of Microelectro-mechanical Systems*, 5, 298 (1996).
5. A.D. Oliver and K.D. Wise, "A 1024-Element Bulk-Micromachined Thermopile Infrared Imaging Array," Sensors and Actuators A, 73, 222 (1999).
6. A. Schaufelbuhl, N. Schneeberger, U. Munch, O. Paul, H. Baltes, C. Menofi, and Q. Huang, "Uncooled Low-Cost Thermal Imager Using Micromachined CMOS Integrated Sensor Array," *Int. Conf. On Solid-State Sensors&Actuators (TRANSDUCERS'99)*, Sendai, Japan, 6/7-10/99, (1999), pp. 606-609.
7. D.S. Tezcan, F. Kocer, and T. Akin, "An Uncooled Microbolometer Infrared Detector in any Standard CMOS Technology," *Int. Conf. On Solid-State Sensors&Actuators (TRANSDUCERS'99)*, Sendai, Japan, 6/7-10/99, (1999), pp. 610-613.
8. M. Parameswaran, H.Baltes, L.Ristic, D. Dhaded, and A. Robinson, "A New Approach for the Fabrication of Micromechanical Structures," *Sensors and Actuators A*, 19, 289 (1989).
9. T. Akin, Z. Olgun, O. Akar, and H. Kulah, "An Integrated Thermopile Structure with High Responsivity using Any Standard CMOS Process," *Sensors and Actuators A*, 66, 218 (1998).
10. N. Schneeberger, O. Paul, and H. Baltes, "Spectral Infrared Absorption of CMOS Thin Film Stacks," *Int. Conf. on Micro Electromechanical Systems (MEMS'99)*, Orlando, Florida, 1/17-21/99, (1999), pp. 106-111.
11. E.H. Klaassen, R.J. Reay, C. Storment, and G. T. A. Kovacs, "Micromachined Thermally Isolated Circuits," *Sensor and Actuators A,* 48, 43 (1997).
12. M.C. Acero, J. Esteve, C. Burrer, and A. Gotz, "Electrochemical Etch-Stop Characteristics of TMAH:IPA Solutions," *Sensors and Actuators A*, 46-47, 22 (1995).