

# Performance Characteristics of the Reduced Common Mode Voltage Near State PWM Method

E. Ün, design engineer, Defense Systems Technologies Division, Aselsan Inc., Turkey

A.M. Hava, Department of Electrical and Electronics Engineering, Middle East Technical University, Ankara, Turkey

Keywords: Common mode current, Common mode voltage, EMI, Harmonic, Inverter, Long cable, PWM, Ripple, Scalar PWM, Space vector, Voltage reflection, VSI

## Abstract

The Near State PWM (NSPWM) method, which has low common mode voltage and low common mode current, is proposed for three-phase voltage source inverter drives. The method is described and its voltage linearity, output current ripple, DC bus current ripple, common mode voltage and output line-to-line pulse patterns are thoroughly studied and compared with classical PWM methods. The theory, simulation, and laboratory experiments illustrate that in the high modulation index operating range NSPWM has superior overall performance compared to other methods. NSPWM has low common mode voltage and this results in low common mode current. NSPWM has low switching losses comparable to those of DPWM methods, it has low current ripple compared to the classical methods, and it exhibits no significant overvoltage problems in long cable applications as its pulse pattern involves a sufficient distance between the polarity reversing voltage pulses.

## Introduction

Most AC induction and permanent magnet machines are driven through three-phase Voltage Source Inverters (VSI) which allow the motor voltage and frequency to be freely controlled such that high drive motion quality and high energy efficiency are obtained. With the availability of the high performance power semiconductors such as Insulated Gate Bipolar Transistors (IGBTs), the inverter switches are operated at high switching frequency (a few kHz and above) such that the motor current/torque ripple is low and dynamic performance is high. Pulse Width Modulation (PWM) is the standard approach to operate the inverter switches in order to generate the required output voltages [1]. Conventional Continuous PWM (CPWM) methods such as Space Vector PWM (SVPWM) and Discontinuous PWM (DPWM) methods such as DPWM1, perform satisfactorily in terms of voltage linearity, output current ripple, DC bus current ripple, and average switching frequency requirements [2, 3]. However, they have poor Common Mode Voltage (CMV) and Common Mode Current (CMC) characteristics [4, 5] which result in performance problems in the application field [6]. CMV is defined as the potential of the star point of the load with respect to the center of the DC bus of the Voltage Source Inverter (VSI) ( $V_{no}$  in Fig. 1) and it is expressed as follows.

$$V_{no} = (V_{ao} + V_{bo} + V_{co}) / 3 \quad (1)$$

Depending on the VSI type (two-level, neutral point clamped three-level, etc.) CMV may have various levels. In the two-level VSI, which is the standard topology that this paper investigates, CMV may be  $\pm V_{dc}/6$  or  $\pm V_{dc}/2$  depending on the state of the switches and therefore on the PWM method employed. At high switching frequencies, high  $dv/dt$  ratios (which could be obtained with rather smaller IGBT gate resistances), and high DC bus voltage levels, the CMVs generated result in performance problems in motor drives. Due to these CMVs, the capacitive nature of the high frequency model of the AC machines allows high frequency CMCs to flow from the stator windings to the ground (partially through bearings). CMCs may have large magnitude (comparable to the rated motor currents). Consequently, bearing damage (fluting) occurs and motor failure results [6]. The CMCs additionally

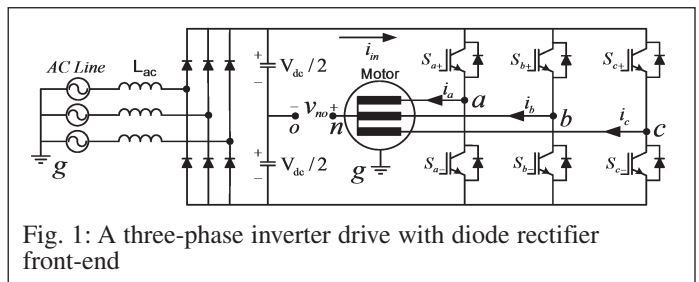


Fig. 1: A three-phase inverter drive with diode rectifier front-end

create noise in the electrical circuit resulting in nuisance trips of the drive or other equipment fed from the same power line [7].

In the standard PWM methods, CMV takes the values of  $\pm V_{dc}/6$  or  $\pm V_{dc}/2$ . PWM methods that eliminate the  $\pm V_{dc}/2$  level have been developed such that CMV is limited to  $\pm V_{dc}/6$ . The recently developed Reduced CMV PWM (RCMV-PWM) methods [4] such as Active Zero State PWM1 (AZSPWM1) [8], Remote State PWM3 (RSPWM3) [9], and Active Zero State PWM2 (AZSPWM2) [10, 11] exhibit performance constraints that prohibit their practical utilization [12]. All the recently developed RCMV-PWM methods are classified and widely discussed in [4] in detail and the reader is referred to [4] for the major attributes of such methods. This paper proposes a new RCMV-PWM method, the Near State PWM (NSPWM) method that exhibits low CMV, prevents instantaneous polarity reversals of line-to-line voltages, and has satisfactory PWM ripple performance [5]. First, the NSPWM method is described via space vector approach and its voltage linearity region is illustrated. Following, the performance characteristics of the method are studied in detail. The motor harmonic current and DC link harmonic current characteristics of the method are thoroughly investigated and compared to conventional methods. Detailed computer simulations of a motor drive illustrating the motor current ripple characteristics and detailed laboratory experiments demonstrating the CMV/CMC performance of the method are provided. Finally the experimental line-to-line voltage pattern performance of the method which illustrates its satisfactory performance for long cable application is demonstrated.

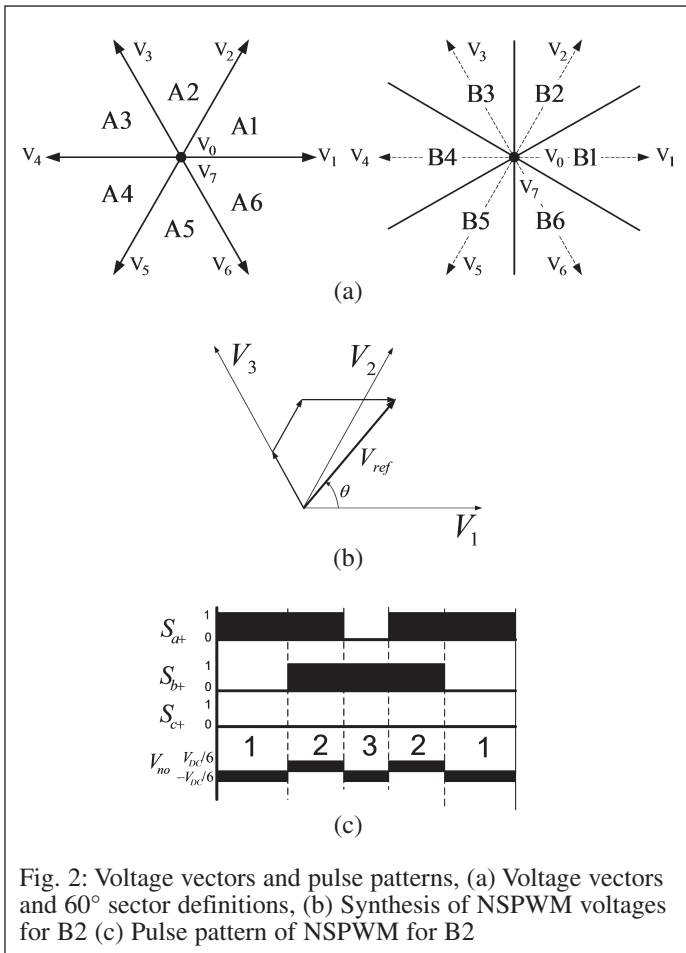


Fig. 2: Voltage vectors and pulse patterns, (a) Voltage vectors and 60° sector definitions, (b) Synthesis of NSPWM voltages for B2 (c) Pulse pattern of NSPWM for B2

### The Near State PWM (NSPWM) method

The Near State PWM (NSPWM) method utilizes a group of three neighbor voltage vectors to match the output and reference volt-seconds. These three voltage vectors are selected such that the voltage vector closest to reference voltage vector and its two neighbors (to the right and left) are utilized. Therefore, the utilized voltage vectors are changed in every 60° throughout the space. As shown in Fig. 2.a, to apply the method, the voltage vector space is divided into six segments. Defined with indices, voltage vectors  $V_{i-1}$ ,  $V_i$ , and  $V_{i+1}$  are utilized for region Bi. For example, for the region between 30° and 90° (B2), the applied voltage vectors are  $V_1$ ,  $V_2$ , and  $V_3$  (Fig. 2.b). As a result the PWM pulse pattern of the method in this region becomes as shown in Fig. 2.c. Notice that phase “c” is not switched within this cycle (thus over B2).

Utilizing the above defined near state voltage vectors, the complex variable volt-seconds balance equation and the PWM period constraint for NSPWM can be written in generalized form for region Bi in equations (2.a) and (2.b) where  $T_s$  is the PWM period. Normalizing the voltage vector on-time values, the vector duty cycles can be found as  $d_k = t_k / T_s$ , where  $k: i - 1, i, i + 1$ . Utilizing (2.a) and (2.b), the duty cycles of the required voltage vectors can be calculated for region Bi as in (3), (4), and (5).

$$V_{i-1}t_{i-1} + V_i t_i + V_{i+1}t_{i+1} = V_{ref}T_s \quad (2.a)$$

$$t_{i-1} + t_i + t_{i+1} = T_s \quad (2.b)$$

$$d_{i-1} = 1 - \frac{2\sqrt{3}}{\pi} M_i \sin\left(\theta - \frac{(i-2)\pi}{3}\right) \quad (3)$$

$$d_i = -1 + \frac{3}{\pi} M_i \cos\left(\theta - \frac{(i-2)\pi}{3}\right) + \frac{3\sqrt{3}}{\pi} M_i \sin\left(\theta - \frac{(i-2)\pi}{3}\right) \quad (4)$$

$$d_{i+1} = 1 - \frac{3}{\pi} M_i \cos\left(\theta - \frac{(i-2)\pi}{3}\right) - \frac{\sqrt{3}}{\pi} M_i \sin\left(\theta - \frac{(i-2)\pi}{3}\right) \quad (5)$$

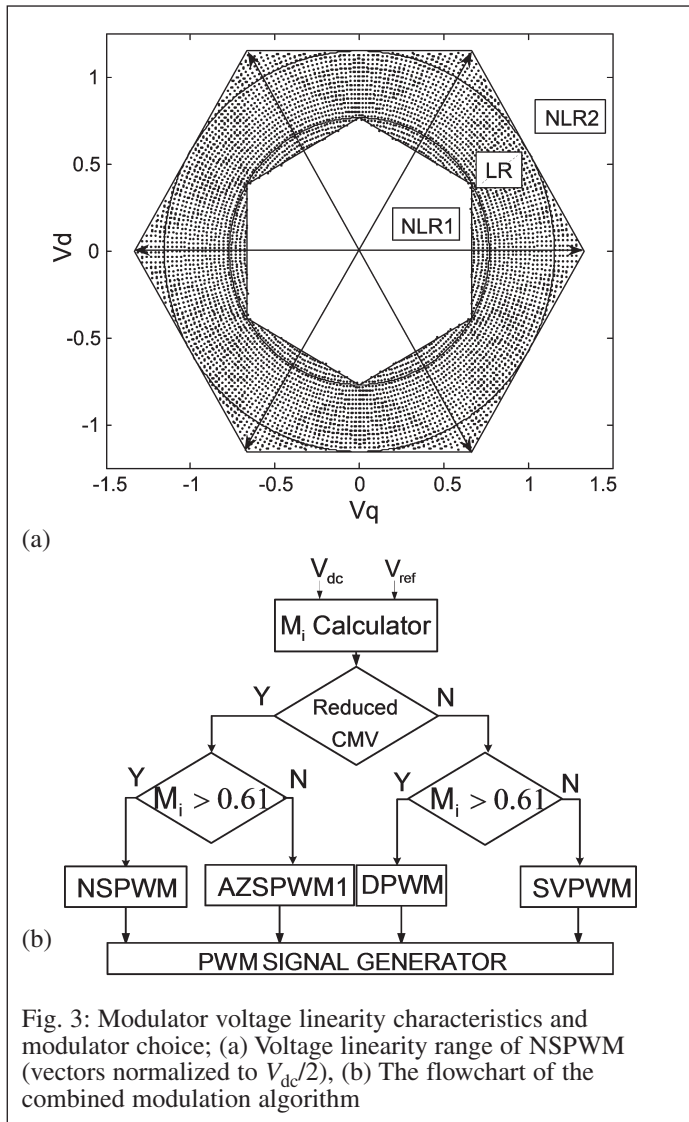
In the above equations,  $\theta = \omega_c t$  is the angle of the reference voltage vector, and  $M_i$  is the modulation index defined in (6) [1, 2], where  $V_m$  is the output voltage fundamental component magnitude and  $V_{dc}$  is the inverter DC bus voltage magnitude.

$$M_i = V_m / (2 V_{dc} / \pi). \quad (6)$$

Equations (3), (4), and (5) yield a valid solution only in region LR of the inverter voltage vector space as shown in Fig. 3.a and there is no solution elsewhere. A method with acceptable performance should be used in NLR1 (a combined PWM algorithm must be used). In the modulation algorithm shown in Fig.3.b, in NLR1, if low RCMV is required AZSPWM1, or if lower PWM ripple is required SVPWM or DPWM methods should be employed [13]. The transition between NSPWM and the alternative method can be done seamlessly and has no influence on the drive performance [13]. Region LR, where (3), (4), and (5) have a valid solution, corresponds to per fundamental cycle voltage linearity between the modulation indices of  $M_{iLmin} = \pi/(3\sqrt{3}) \cong 0.61$  and  $M_{iLmax} = \pi/(2\sqrt{3}) \cong 0.907$ . For the shaded region in Fig. 3.a, where NSPWM has a valid solution, the three voltage vectors may be combined in various sequences to program the required output voltage. With the constraints of minimum switching count, no simultaneous switchings of phase legs, and minimum CMV, only the sequence of  $V_{i+1} - V_i - V_{i-1} - V_i - V_{i+1}$  as a general form for region Bi remains feasible. For example, between 30° and 90° (B2), the optimal sequence is  $V_3 - V_2 - V_1 - V_2 - V_3$ . In this sequence state changes occur only between adjacent states and this is the only sequence which does not require simultaneous switching of the inverter legs. The sequences of NSPWM and other methods are shown in Table I for region definitions of Fig. 2.a. Given this sequence, CMV of NSPWM varies between  $-V_{dc}/6$  and  $+V_{dc}/6$  as shown in Fig. 2.c and its low value is favored as will be detailed in later sections.

The practical implementation of NSPWM is similar to that of DPWM methods and can be implemented by scalar PWM approach [2]. Its pulse pattern can be easily programmed by modern DSPs with flexible PWM modules (such as TI TMS320F2808 which has 6 pairs of CompA/CompB registers) [14]. Note that the space vector approach is mainly utilized to illustrate the principle of the method while the practical implementation preferably involves the scalar PWM approach. In the scalar approach, simple signal comparisons and zero sequence signal injection yield the discontinuous PWM pattern of NSPWM [12]. If the scalar implementation is employed as proposed in [12], then the NSPWM modulator can be utilized in the complete modulation range (NLR1, LR, and NLR2). In this case, the modulator behavior in LR is the same as the ideal NSPWM behavior. In NLR2, the over-modulation behavior is exactly the same as the conventional DPWM1 method as reported in [3, 15] and high modulator gain is the basic advantageous characteristic. In NLR1, however, with the scalar implementation, the modulator exhibits linear voltage gain characteristics. But, additional zero states are created and the

	A1	A2	A3	A4	A5	A6
CPWM	7210127	7230327	7430347	7450547	7650567	7610167
AZSPWM1	3216123	4321234	5432345	6543456	1654561	2165612
	B1	B2	B3	B4	B5	B6
NSPWM	21612	32123	43234	54345	65456	16561



RCMV property is lost. Besides, the PWM ripple becomes quite large compared to conventional methods. Thus, the utilization of the single scalar PWM method or combined PWM algorithm (as shown in Fig.3.b) is dependent on whether the application can tolerate high PWM current ripple or high CMV/CMC in the NLR1 region. In this paper, mainly the LR region performance of NSPWM is investigated.

NSPWM pulse pattern differs from many other RCMV-PWM pulse patterns with regard to the inverter blanking time (dead time). Most RCMV-PWM methods provide CMV reduction by selecting a sequence of active inverter voltage states that require simultaneous switching of two inverter legs during state transitions. RSPWM3 [9] and AZSPWM2 [10, 11] are two such methods. However, in the presence of inverter dead time, gate signal delay differences, and/or unidentical IGBT/diode switching characteristics, simultaneous switchings of two inverter legs can not be realized. Not only the CMV magnitude becomes as large as the conventional PWM methods ( $\pm V_{dc}/2$ ), but also the additionally created CMV pulses become narrow leading to exacerbation of the high frequency effects and overvoltages at the motor terminals. Therefore, such methods are not practical [4, 12]. The NSPWM method pulse pattern involves switching one inverter leg at a time. Thus, NSPWM is free of such problems and its performance is not affected by the inverter dead time [4, 12].

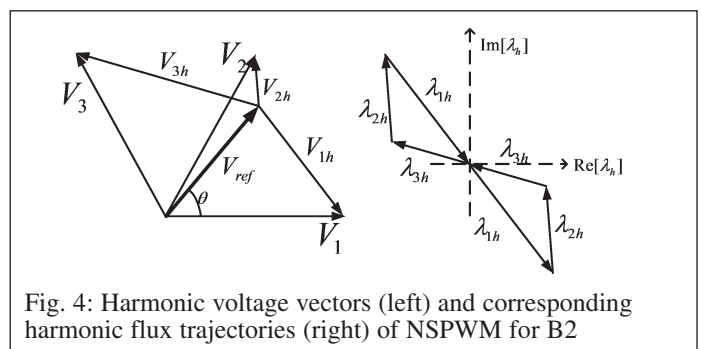
## Inverter output voltage/current harmonic distortion characteristics

The inverter output voltage waveform quality can be best studied with the aid of space vectors [1, 2]. The difference between the reference voltage vector and output voltage vector corresponds to the harmonic voltage vector. Since the switching frequency model of motor drives is the motor leakage inductance, the integral of the harmonic voltage vector is proportional to the harmonic current and therefore to the torque ripple in motor drives. Thus, output voltage waveform quality is generally investigated in terms of the normalized harmonic flux vector defined in (7) over an arbitrary PWM cycle ( $N^{\text{th}}$  cycle) [2].

$$\lambda_{\text{hn}}(M_i, \theta, V_{dc}) = \frac{\pi}{V_{dc} T_s} \int_{NT_s}^{(N+1)T_s} (V_k - V_{\text{ref}}) dt \quad (7)$$

Since each PWM method differs in the utilization of the voltage vectors and their sequence, the harmonic flux vector of each PWM method is unique. The harmonic flux trajectories of each PWM method vary depending on the angle and magnitude of the reference voltage vector. The harmonic voltage vector and harmonic flux trajectories of NSPWM are illustrated in Fig. 4. The flux trajectory resembles a butterfly shape. The butterfly's wings and size change with  $M_i$  and  $\theta$ . As Fig. 5.a illustrates for constant  $\theta$ , as  $M_i$  increases the harmonic flux trajectories get noticeably narrower. However, as Fig. 5.b illustrates, the  $\theta$  dependency of harmonic flux trajectories is not strong. Although the shapes of harmonic flux trajectories are different for different  $\theta$  values, all have similar size. In order to show the harmonic content clearly, the magnitude of the harmonic flux vector is illustrated over a half PWM cycle with the time axis normalized to  $T_s$  in Fig. 5.c. As the figure illustrates, the harmonic content slightly decreases as  $\theta$  approaches  $60^\circ$ .

In the following, the NSPWM harmonic flux trajectories will be discussed in comparison with those of DPWM1. Here DPWM1 is taken as base because for approximately  $M_i \geq 0.6$ , it has the best overall performance among conventional PWM methods [2], both methods have discontinuous switching, and their practical  $M_i$  range is also the same. Therefore, it is expected that their harmonic fluxes to be similar. Fig. 6 shows the harmonic flux trajectories of both methods for  $M_i = 0.9$  and two angles,  $\theta = 30^\circ$  and  $\theta = 60^\circ$ . In the figure the harmonic flux magnitudes over a half PWM cycle are also shown. For  $M_i = 0.9$  and  $\theta = 30^\circ$ , the duration of the zero vector for DPWM1 and duration of  $V_3$  for NSPWM are zero and both methods utilize the same voltage vectors with the same duration (Fig. 6, left, top). Therefore, the shapes and magnitudes of harmonic flux trajectories of both methods are the same. As  $\theta$  approaches  $60^\circ$ ,  $V_3$  for NSPWM and  $V_0$  for DPWM1 become more dominant (Fig. 6, bottom, left). Therefore, harmonic flux trajectories of the two methods differ. For all operating points other than  $\theta = 30^\circ$ , the magnitudes of harmonic flux vectors of



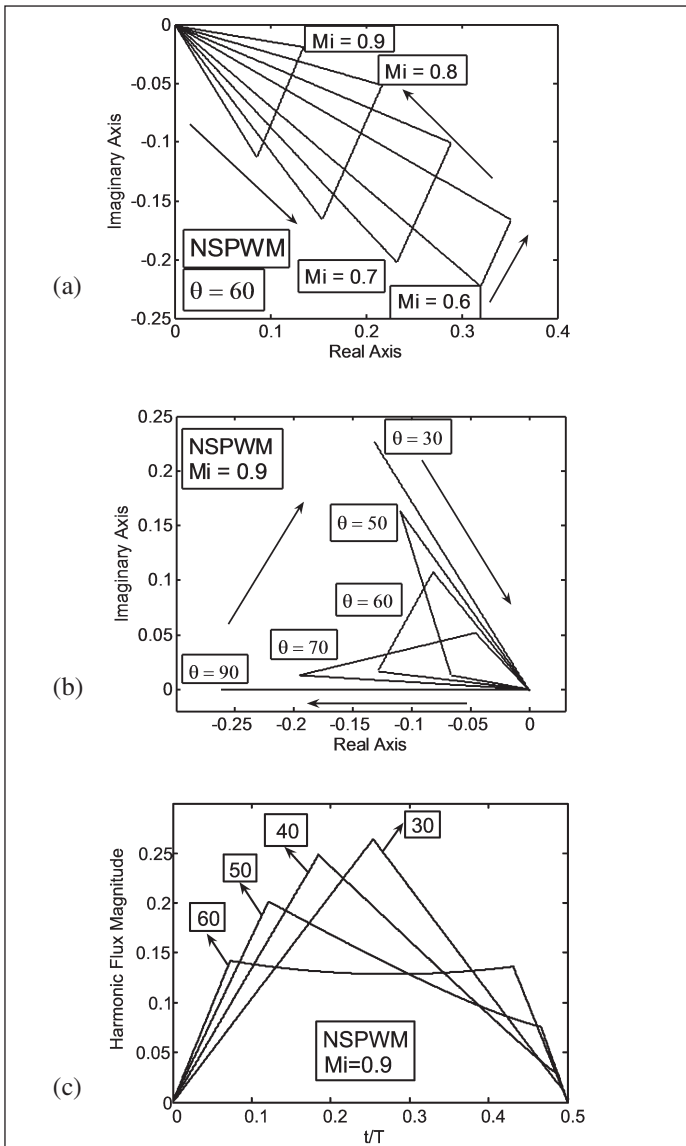


Fig. 5: NSPWM complex plane harmonic flux trajectories (a) & (b) and time dependent harmonic flux magnitude (c)

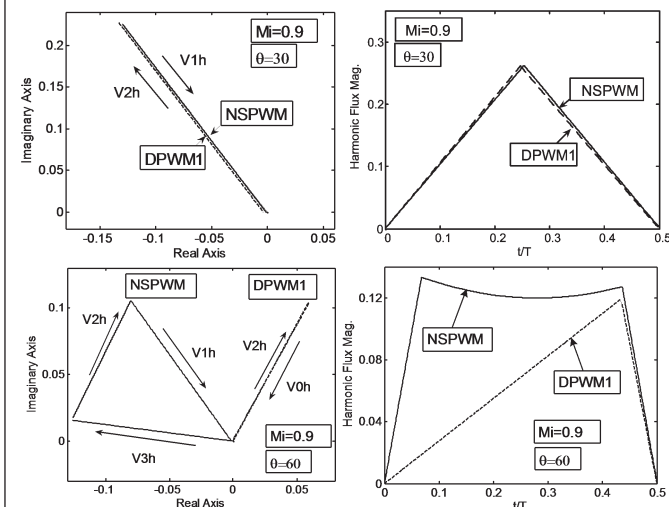


Fig. 6: Harmonic flux trajectories (complex domain, left) and magnitudes (time domain, right) for DPWM1 and NSPWM

NSPWM become slightly larger than those of DPWM1 (Fig. 6, right). Therefore, DPWM1 has less ripple than NSPWM in general, although the difference is space dependent and typically small. The harmonic flux trajectories are not convenient for overall comparison of ripple performance of PWM methods. For this purpose, the below defined integral quantities are employed.

The RMS harmonic flux over a PWM cycle (duty cycle  $\delta$  of 0 to 1),  $\lambda_{\text{hn-rms}}$ , and Harmonic Distortion Factor (HDF), which is the normalized form of  $\lambda_{\text{hn-rms}}$  over the full fundamental cycle, are the per PWM cycle (local) and per fundamental cycle (global) harmonic performance indices given as follows.

$$\lambda_{\text{hn-rms}}(M_i, \theta) = \sqrt{\int_0^1 \lambda_{\text{hn}}^2 d\delta} \quad (8)$$

$$HDF = f(M_i) = \frac{288}{\pi^2} \frac{1}{2\pi} \int_0^{2\pi} \lambda_{\text{hn-rms}}^2 d\theta \quad (9)$$

The local RMS harmonic flux characteristics of various PWM methods, including NSPWM, DPWM1, and other methods such as SVPWM are numerically evaluated under the criteria of equal average switching frequency for  $M_i = 0.61$  and  $M_i = 0.9$  and are illustrated in Fig. 7.a and 7.b respectively. At  $M_i = 0.61$ , the harmonic content of NSPWM is significantly higher than CPWM and DPWM methods. However, it is flat and much lower than other RCMV-PWM methods. At  $M_i = 0.9$ , the RMS harmonic flux of NSPWM is significantly less than SVPWM and RCMV-PWM methods, but slightly inferior to DPWM.

The HDF characteristics of the above discussed methods are all numerically calculated by (9) and shown in Fig. 8. Since NSPWM is linear in the  $0.61 < M_i < 0.907$  range, its curve is provided for a narrower range than other methods. Throughout its linearity range, NSPWM has the least harmonic distortion among all RCMV-PWM methods. In its lower linear  $M_i$  range, NSPWM has higher harmonic content than the conventional PWM methods. In the higher end of the linear modulation range, NSPWM performs better than CPWM methods and comparably with DPWM methods.

### DC link current ripple characteristics

The DC link current of the inverter  $i_{\text{in}}$  (Fig. 1) is important for DC bus capacitor sizing as the capacitor suppresses all PWM ripple current. The DC link ripple current has limiting effect on the capacitor lifetime so it should be as small as possible. Each PWM method has a unique DC link current ripple characteristic. Defined in (10),  $K_{\text{dc}}$  is the ratio of DC link current ripple square to output phase current RMS value square. Smaller  $K_{\text{dc}}$  implies smaller capacitor requirement and longer capacitor life. For NSPWM,  $K_{\text{dc}}$  is analytically calculated in (11) as a function of  $M_i$  and load power factor (PF) angle  $\varphi$ .

$$K_{\text{dc}} = I_{\text{inrms}}^2 / I_{\text{1rms}}^2 \quad (10)$$

$$K_{\text{dc}}^{\text{NSPWM}} = 1 + \left(\frac{24}{\pi^2} M_i - \frac{3\sqrt{3}}{\pi}\right) \cos 2\varphi - M_i^2 \frac{18}{\pi^2} \cos^2 \varphi \quad (11)$$

In Fig. 9,  $K_{\text{dc}}$  curves of various PWM methods including NSPWM are illustrated as a function of  $M_i$  with PF as parameter (PF =  $\cos \varphi$ ). The DC link harmonic content of NSPWM is strongly dependent on PF and  $M_i$ .  $K_{\text{dc}}$  of NSPWM decreases with increasing  $M_i$  and

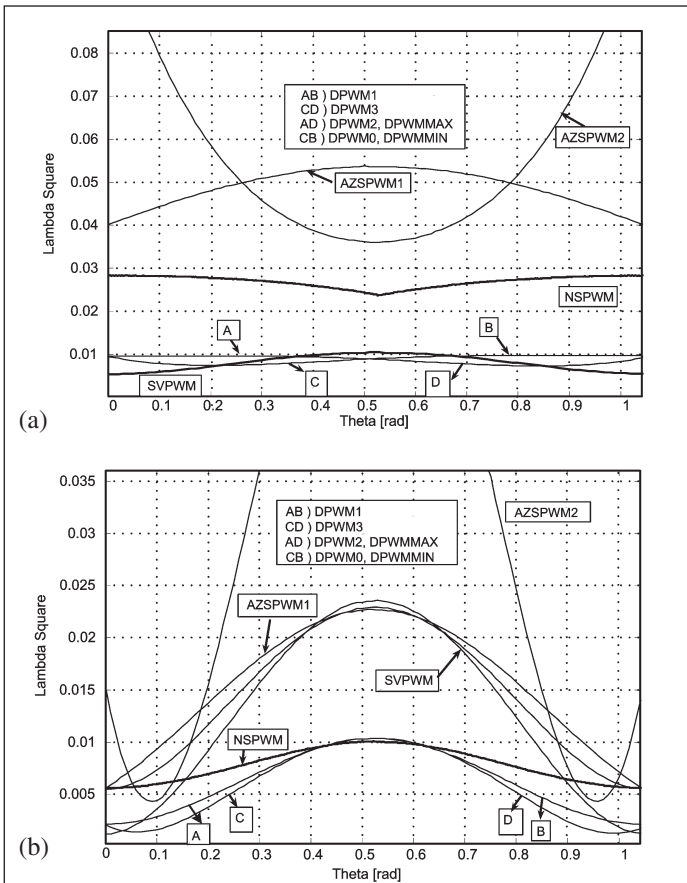


Fig. 7: Spatial harmonic flux variation  $\lambda^2 = f(\theta)$  for (a)  $M_1 = 0.61$ , (b)  $M_1 = 0.9$

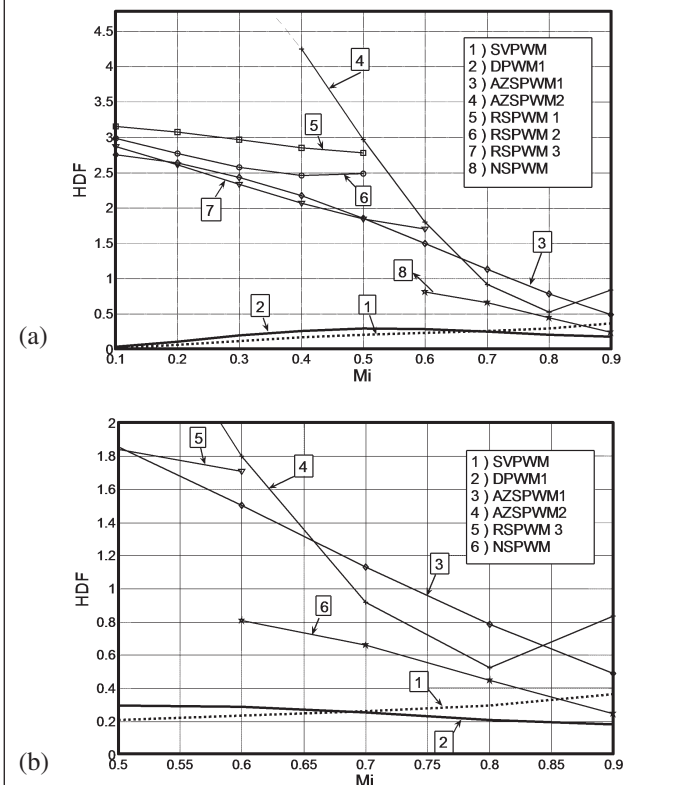


Fig. 8: HDF =  $f(M_1)$  for various PWM methods (a), zoom in view of the upper  $M_1$  region (b)

PF. For PF = 1, NSPWM has lower DC link ripple content than all other PWM methods. For PF of 0.8-0.9,  $K_{dc}$  of all PWM methods are similar. However, for PF lower than approximately 0.6,  $K_{dc}$  of NSPWM is inferior to other methods. At high PF, the superior  $K_{dc}$  of NSPWM can be explained by observing the per-carrier cycle behavior of the inverter. The DC link current is formed from current pulses associated with the inverter voltage vectors utilized. Since each PWM method has a unique PWM pulse pattern, the resulting DC link current also is unique to the method. Fig. 10 illustrates the DC link current of NSPWM and DPWM1 within a PWM cycle for unity and zero PF (lagging) load current,  $M_1 = 0.78$ ,  $\theta = 45^\circ$ , for region B2. For PF = 1, the DC link current pulses of NSPWM are closer to their average value compared to DPWM1. Spanning the whole vector space, the voltage vectors and their sequence and the phase currents (their magnitude and polarities) change, but the tendency of DC link current ripple remains the same. Hence, NSPWM has smaller  $K_{dc}$ . At low PF, this relation reverses and NSPWM performs poorly. For practical motor drive applications, at full-load PF approaches unity and the motor runs at the rated current. Although the motor current is large, due to high PF,  $K_{dc}$  is small. At no-load, the motor PF is poor but the motor current is quite small compared to rated case. Here,  $K_{dc}$  is large but the ripple current remains small compared to that of the rated load operating condition. As a result the capacitor ripple current becomes small over the complete operating range of the drive. Therefore, with NSPWM, the DC bus capacitor can be smaller compared to the conventional PWM methods.

It is worth mentioning that one basic property of NSPWM is that the DC link current is always present since always active inverter states are utilized. Utilizing the inverter switch state information along with only the DC link current measurement, the three phase currents can be reconstructed (for utilization in the motor control algorithm) and low cost current measurement can be achieved.

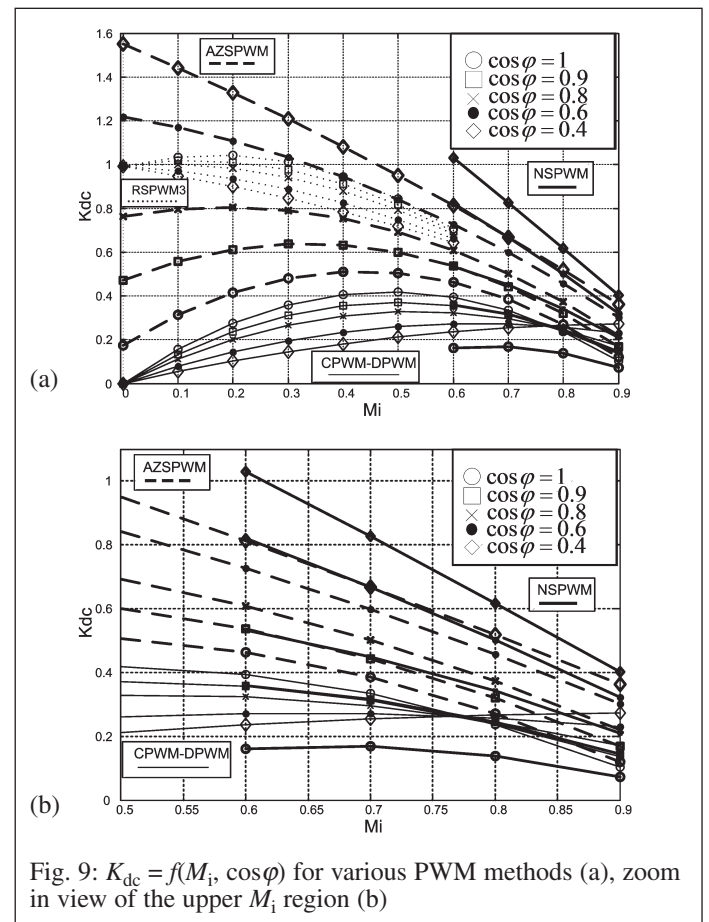


Fig. 9:  $K_{dc} = f(M_1, \cos \phi)$  for various PWM methods (a), zoom in view of the upper  $M_1$  region (b)

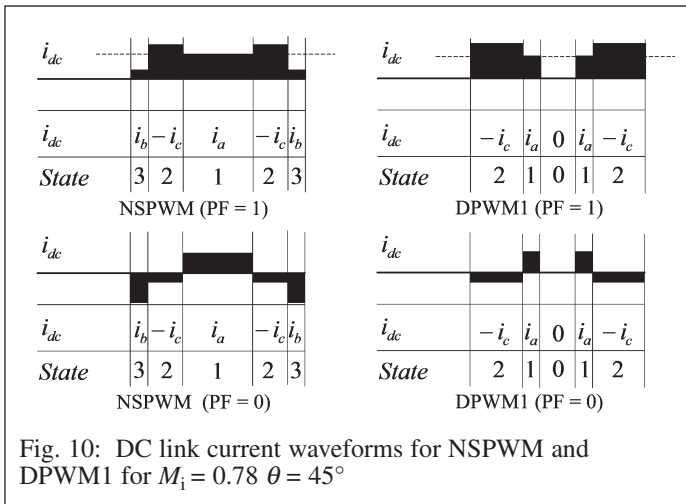


Fig. 10: DC link current waveforms for NSPWM and DPWM1 for  $M_i = 0.78$   $\theta = 45^\circ$

### CMV and line-to-line voltage pulse patterns

The pulse pattern of NSPWM is different from the pattern of conventional PWM methods. As a result, the Common Mode Voltage (CMV) pattern and the inverter output voltage pattern are different from the conventional patterns. While the CMV characteristics of NSPWM are favorable over the conventional methods, the line-to-line voltage pulse pattern may be problematic depending on the application. In the following, these issues will be addressed.

The inverter leg upper switch logic, CMV, and line-to-line voltage patterns for NSPWM, SVPWM, DPWM1, and AZSPWM1 are

shown in Fig. 11. SVPWM and DPWM1 have high CMVs (limits:  $\pm V_{dc}/2$ ). NSPWM and AZSPWM1 reduce the CMV (limits:  $\pm V_{dc}/6$ ). This is the main advantage of RCMV-PWM methods. Although the CMVs of RCMV-PWM methods are less than those of the conventional methods, the rate of change of CMV is the same for all methods. During a switching transition CMV always changes by  $|\Delta V| = V_{dc}/3$ . Thus the capacitive CMC during the switching transition is similar. Therefore, during switching transients CMC is high and comparable in all methods, while between switching instants the CMC of RCMV-PWM methods is significantly lower than other methods. As a result NSPWM has lower CMV, CMC, and leakage current than conventional methods and is more motor friendly [12].

In motor drive applications involving long cables, two consecutive voltage pulses with opposite polarity must be separated by a sufficient time interval to damp the switching induced overvoltage due to voltage reflection [16]. Methods with bipolar pulse pattern are not favorable unless the pulses are safely distant from each other. As Fig. 11 shows, the inverter output line-to-line voltage patterns of CPWM/DPWM methods are unipolar such that the polarity of the line-to-line voltage does not change within a PWM cycle (there is pulse-polarity consistency). In AZSPWM1 always two of the three line-to-line voltages have bipolar pattern while in NSPWM only one of them has bipolar pattern. One of the NSPWM phases is not switching within a PWM cycle while the AZSPWM1 switches are manipulated periodically. In NSPWM, when a pulse reversal occurs in the bipolar line-to-line voltage, there is always a sufficient zero voltage time between the positive and negative pulses. The narrowest time interval that occurs (at the edges of Bi regions,  $30^\circ$ ,  $90^\circ$ , etc.) is a function of  $M_i$  and it starts at 0 for  $M_i = 0.61$ , rapidly increases with  $M_i$ , and typically loses

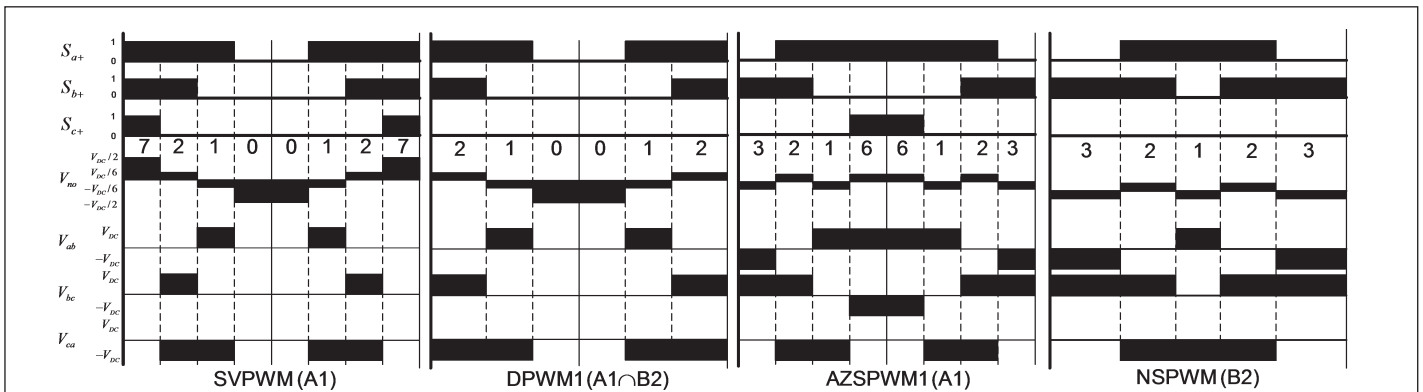


Fig. 11: PWM Pulse pattern of SVPWM, DPWM1, AZSPWM1, and NSPWM methods

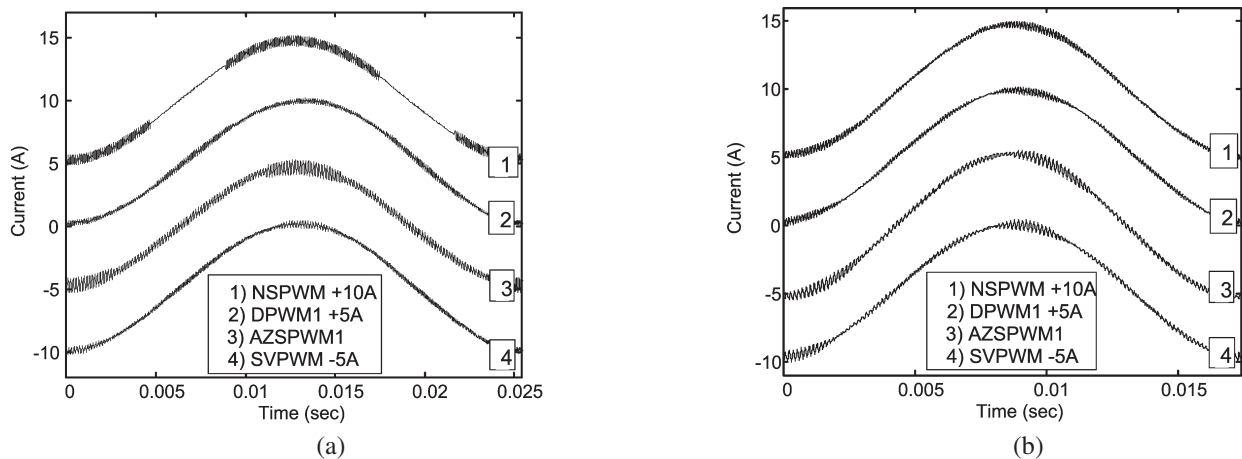


Fig. 12: Output current waveforms for various PWM methods (a)  $M_i = 0.6$  and (b)  $M_i = 0.9$

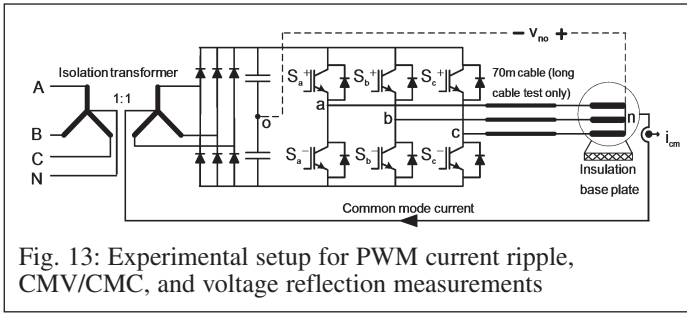


Fig. 12. At  $M_i = 0.6$ , SVPWM and DPWM1 have the least harmonic content, while AZSPWM1 is inferior to all. NSPWM current ripple is significantly space dependent but on the average it is superior to AZSPWM1. At  $M_i = 0.9$ , where the maximum linearity point is approached, NSPWM is comparable to DPWM1 and slightly better than other methods in terms of current ripple.

### Experimental results

To evaluate the overall performance of NSPWM and compare it to other methods, the experimental set-up shown in Fig. 13, which is suitable for CMC and pulse reversal based overvoltage measurement is established [12]. A DSP (TMS320F2808) is utilized to control the motor speed and program the PWM pulse pattern. The motor and drive ratings and parameters are the same as those in the simulations. Fig. 14 shows the phase current, CMC, CMV and the modulation signals for NSPWM, SVPWM, and DPWM1 at  $M_i = 0.8$ . The phase current waveforms are sinusoidal and the PWM current ripple is comparable in all the methods as predicted in the simulations. The CMV comparison indicates that both DPWM1 and SVPWM have high CMV compared to NSPWM. Comparing the CMC characteristics, the difference is not as emphasized as the CMV characteristic, because  $dv/dt$  is the same and dominant. At the switching instants sharp edge voltage pulses (measured as approximately  $3.6 \text{ kV}/\mu\text{s}$ ) cause large magnitude high frequency currents through the capacitive paths in all methods. Differences are still notable in terms of rms and peak values. The microscopic view in Fig. 14 (right), which shows the PWM cycle CMV/CMC waveforms, reveals the details. Since the PWM pulse pattern varies over a fundamental cycle, the PWM characteristics are  $\theta$  dependent. As a result, the CMV/CMC characteristics also vary in space. When comparing the CMV/CMC characteristics, the worst CMV/CMC points are selected for each method and

### Computer simulations illustrating the output current ripple performance

criticality at  $M_i = 0.65$  [12]. In AZSPWM1, regardless  $M_i$  the narrowest interval is zero. This result implies rapid line-to-line voltage reversals and large overvoltages at the motor terminals in long cable applications.

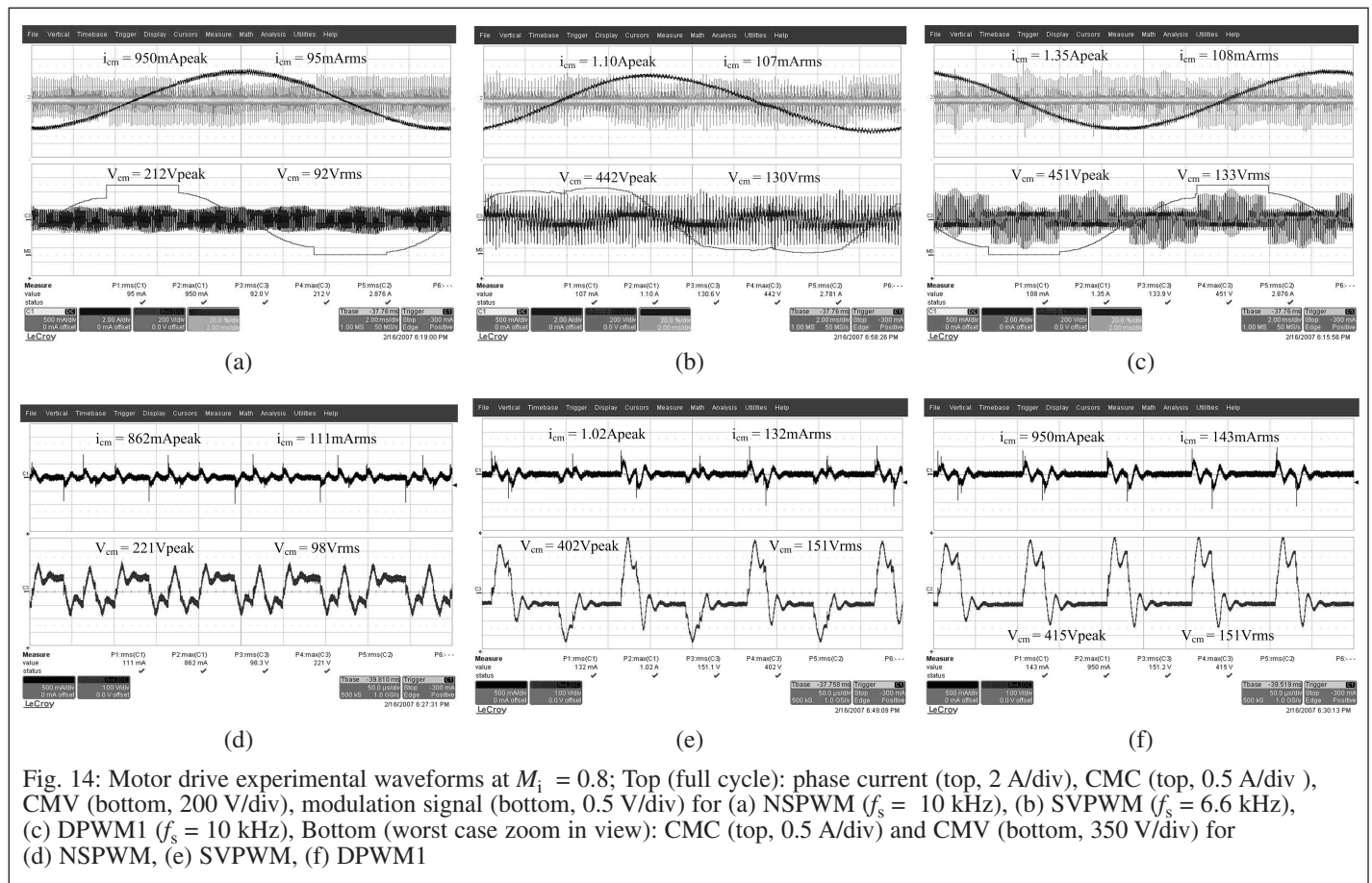


Fig. 14: Motor drive experimental waveforms at  $M_i = 0.8$ ; Top (full cycle): phase current (top, 2 A/div), CMC (top, 0.5 A/div), CMV (bottom, 200 V/div), modulation signal (bottom, 0.5 V/div) for (a) NSPWM ( $f_s = 10 \text{ kHz}$ ), (b) SVPWM ( $f_s = 6.6 \text{ kHz}$ ), (c) DPWM1 ( $f_s = 10 \text{ kHz}$ ), Bottom (worst case zoom in view): CMC (top, 0.5 A/div) and CMV (bottom, 350 V/div) for (d) NSPWM, (e) SVPWM, (f) DPWM1

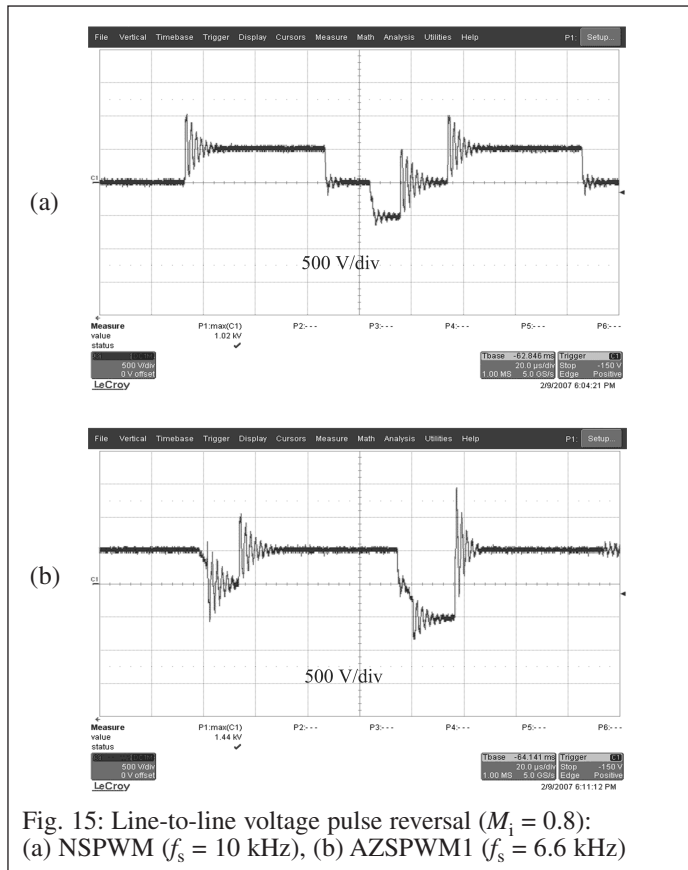


Fig. 15: Line-to-line voltage pulse reversal ( $M_1 = 0.8$ ):  
(a) NSPWM ( $f_s = 10$  kHz), (b) AZSPWM1 ( $f_s = 6.6$  kHz)

shown in the oscillograms. It can be seen that the CMV of DPWM1 and SVPWM are quite larger than those of NSPWM. The peak values of CMCs for all the methods are similar. The RMS value of CMC is slightly better for NSPWM compared to other methods.

The line-to-line voltage pulse pattern of NSPWM is superior to AZSPWM1 as discussed in an earlier section. The experimental waveform of Fig. 15 shows that NSPWM places sufficient zero voltage time interval before pulse reversal occurs while the AZSPWM1 method experiences rapid change with nearly zero time interval between pulses. As shown in the figure, in the worst case, in this long cable application (70 m), the AZSPWM1 method exhibits overvoltages ( $> 1400$  V) while NSPWM performs satisfactorily.

## Conclusions

The NSPWM method, which has low CMV and reduced switching losses compared to conventional PWM methods, is proposed. Utilizing the space vector approach, the vector duty cycles of the method are calculated. The optimal vector sequence is determined and simple scalar implementation is discussed. The output phase current and DC link current harmonic characteristics of NSPWM are investigated and it is shown that they are better than those of other RCMV-PWM methods and comparable with those of standard PWM methods. The NSPWM method has lower CMV than conventional methods and results in lower CMC. The line-to-line voltage pulses of the method are partially bipolar and pulse reversals occur in a similar manner to other RCMV-PWM methods. However, in NSPWM there is always sufficient distance between the voltage pulses such that line-to-line voltage pulse reversal of NSPWM does not cause significant overvoltages (unlike AZSPWM1). Computer simulations illustrating the PWM ripple performance of NSPWM and comparing to other methods are provided. Detailed laboratory experiments illustrating the PWM current ripple

performance, CMV, and CMC characteristics are conducted. The results show that NSPWM has superior overall performance over its voltage linearity range. Its PWM output current ripple is low and comparable to conventional methods. Furthermore, the long cable test with 70 m cable shows that line-to-line voltage pulse reversals do not cause significant overvoltages. Thus, the NSPWM method is a favorable method for motor drive applications operating in the upper half of the linear modulation range ( $M_1 > 0.6$ ). For  $M_1 < 0.6$ , AZSPWM1 may be utilized and combining NSPWM and AZSPWM1 yields a PWM algorithm which is capable of providing full inverter voltage utilization. Thus, a motor drive capable of operating in the full speed range and low common mode voltage and common mode current can be realized.

## References

- [1] J. Holtz: Pulsewidth Modulation for Electronic power Conversion, Proceedings of IEEE, vol. 8, pp. 1194-1214, August 1994.
- [2] A.M. Hava, R.J. Kerkman, T.A. Lipo: Simple Analytical and Graphical Methods for Carrier-Based PWM-VSI Drives, IEEE Trans. on Power Electronics, vol. 14, no: 1, pp. 49 – 61. Jan. 1999.
- [3] A.M. Hava, R.J. Kerkman, T.A. Lipo: A High Performance Generalized Discontinuous PWM Algorithm, IEEE Trans. Ind. Applicat., vol. 34, pp. 1059-1071, Sept./Oct. 1998.
- [4] A.M. Hava, and E. Ün: Performance Analysis of Reduced Common Mode Voltage PWM Methods and Comparison with Standard PWM Methods for Three-phase Voltage Source Inverters, IEEE Trans. on Power Electronics, vol. 24, no: 1, pp. 241-252. Jan. 2009.
- [5] E. Ün and A.M. Hava: Performance Characteristics of the Reduced Common Mode Voltage Near State PWM Method, EPE 2007 Conference, Aalborg, Denmark, September 2007, ISBN: 9789075815108.
- [6] J.M. Erdman, R.J. Kerkman, D.W. Schlegel, and G.L. Skibinski: Effect of PWM Inverters on AC Motor Bearing Currents and Shaft Voltages, IEEE Trans. Ind. Applicat., vol. 32, pp. 250-259, Mar./Apr. 1996.
- [7] G.L. Skibinski, R.J. Kerkman and D. Schlegel: EMI emissions of modern PWM AC drives, IEEE Ind. Applicat. Soc. Mag., vol. 5, pp. 47-81, Nov./Dec. 1999.
- [8] Y.S. Lai, F.S. Shyu: Optimal Common-Mode Voltage Reduction PWM Technique for Inverter Control with Consideration of the Dead-Time Effects-Part I: Basic Development, IEEE Trans. on Ind. Applicat., vol 40, no. 6, pp.1605 – 1612. Nov.-Dec. 2004.
- [9] M. Cacciato, A. Consoli, G. Scarcella, A. Testa: Reduction of Common-Mode Currents in PWM Inverter Motor Drives, IEEE Trans. on Ind. Applicat., vol. 35, no 2, pp. 469 – 476. March-April 1999.
- [10] J. Zitzelberger, W. Hofmann: Reduction of Bearing Currents in Inverter Fed Drive Applications by Using Sequentially Positioned Pulse Modulation, EPE Journal. Vol. 14, No. 4, 2004, pp. 19-25.
- [11] E. Ün: Common Mode Voltage and Current Reduction in Voltage Dource Inverter Driven Three Phase AC Motors, M.S. thesis, Middle East Tech. Univ., Ankara, Turkey, Nov. 2007.
- [12] E. Ün and A.M. Hava: A Near State PWM Method with Reduced Switching Losses and Reduced Common Mode Voltage for Three-Phase Voltage Source Inverters, IEEE Trans. Ind. Applicat., vol. 45, no. 2, pp. 782-793, March/April 2009.
- [13] E. Ün and A.M. Hava: A High Performance PWM Algorithm for Common Mode Voltage Reduction in Three-phase Voltage Source Inverters, in Proc. IEEE PESC'08, 2008, pp. 1528-1534.
- [14] Texas Instruments: TMS320x28xx, 28xxx Enhanced Pulse Width Modulator (ePWM) Module Reference Guide, Literature Number: SPRU791D, November 2004–Revised October 2007.
- [15] A.M. Hava, R.J. Kerkman, T.A. Lipo: Carrier Based PWM-VSI Over-



modulation Strategies: Analysis, Comparison, and Design, IEEE Trans. on Power Electronics, vol. 13, no: 4, pp. 674-689, July 1998.

- [16] R.J. Kerkman, D. Leggate, and G.L. Skibinski: Interaction of Drive Modulation and Cable Parameters on AC Motor Transients, IEEE Trans. Ind. Applicat., vol. 33, pp. 722-731, May/June 1997.

## Biographies



Emre Ün was born in Ankara, Turkey, in 1983. He received the B.S. and M.S. degrees in electrical engineering from Middle East Technical University, Ankara, in 2004 and 2007, respectively. From 2004 to 2008, he was a research assistant with Middle East Technical University, Department of Electrical and Electronics Engineering. Since July 2009 he has been employed at Aselsan Inc., Defense Systems Technologies Division, as a design engineer. His research interests include voltage-source inverters,

PWM methods, and common-mode noise and reduction methods in ac motors.

ASELSAN Inc., Defense Systems Technologies Division  
P.O. Box 1, 06172 Yenimahalle-Ankara, TURKEY  
emreun@aselsan.com.tr  
Phone: +90-312-592-3770  
Fax: +90-312-592-3030



Ahmet M. Hava was born in Mardin, Turkey, in 1965. He received the B.S. degree from Istanbul Technical University, Istanbul, Turkey, in 1987, and the M.Sc. and Ph.D. degrees from the University of Wisconsin, Madison, in 1991 and 1998, respectively, all in electrical engineering. In 1995, he was with Rockwell Automation-Allen Bradley Company, Mequon, Wisconsin, USA. From 1997 to 2002, he was with Yaskawa Electric America, Inc., Waukegan, Illinois, USA. Since 2002, he has been an Assistant Professor with the Department of Electrical and Electronics

Engineering, Middle East Technical University, Ankara, Turkey. His research interests include power electronics, motor drives, and electric power quality.

Department of Electrical and Electronics Engineering  
Middle East Technical University  
İnönü Bulvarı, 06531 Ankara, TURKEY  
hava@metu.edu.tr  
Phone: +90-312-210-2377  
Fax: +90-312-210-2304

