

## Performance Characteristics Of The Reduced Common Mode Voltage Near State PWM Method

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### Keywords

Inverter, VSI, PWM, Common mode voltage, Common mode current, EMI, Harmonic, ASD, Long cable.

### Abstract

The Near State PWM (NSPWM) method, which has low common mode voltage/current is proposed for three-phase voltage source inverter drives. The method is described and its voltage linearity, output current ripple, DC bus current ripple, common mode voltage and output line-to-line pulse patterns are thoroughly studied and compared with classical PWM methods. The theory, simulation, and laboratory experiments illustrate that NSPWM has low common mode voltage, results in less common mode current, has low switching losses comparable to those of DPWM methods, has low current ripple compared to the classical methods, and exhibits no significant overvoltage problems in long cable applications as its pulse pattern involves a sufficient distance between the polarity reversing voltage pulses.

### Introduction

Most AC induction and permanent magnet machines are driven through three-phase Voltage Source Inverters (VSI) which allow the motor voltage and frequency to be freely controlled such that high drive motion quality and high energy efficiency obtained. With the availability of the high performance power semiconductors such as Insulated Gate Bipolar Transistors (IGBTs), the inverter switches are operated at high switching frequency (a few kHz and above) such that the motor current/torque ripple is low and dynamic performance is high. Pulse Width Modulation (PWM) is the standard approach to operate the inverter switches in order to generate the required output voltages. Conventional Continuous PWM (CPWM) methods such as Space Vector PWM (SVPWM) and Discontinuous PWM (DPWM) methods such as DPWM1 [1], perform satisfactorily in terms of voltage linearity, output current ripple, DC bus current ripple, and average switching frequency requirements. However, they have poor Common Mode Voltage (CMV) and Common Mode Current (CMC) characteristics which result in performance problems in the application field. CMV is defined as the potential of the star point of the load with respect to the center of the DC bus of the Voltage Source Inverter (VSI) ( $V_{no}$  in Fig. 1.) and is expressed as follows.

$$V_{no} = (V_{ao} + V_{bo} + V_{co}) / 3 \quad (1)$$

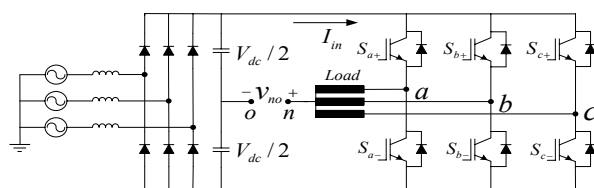


Fig. 1: A three-phase inverter drive with diode rectifier front-end

Depending on the VSI type (two-level, neutral point clamped three-level, etc.) the CMV may have various levels. In the two-level VSI, which is the standard topology that this paper investigates, CMV may be  $\pm V_{dc}/6$  or  $\pm V_{dc}/2$  depending on the state of the switches and therefore on the PWM method employed. At high switching frequencies, high  $dv/dt$  ratios (which could be obtained with rather smaller IGBT gate resistances), and high DC bus voltage levels, the CMVs generated result in performance problems in motor drives. Due to these CMVs, the capacitive nature of the high frequency model of the AC machines allows high frequency CMCs to flow from the stator windings to the ground (partially through bearings). CMCs can have large magnitude (comparable to the rated motor currents). Consequently, bearing damage (fluting) occurs and motor failure results. The CMCs additionally create noise in the electrical circuit resulting in nuisance trips of the drive or other equipment fed from the same power line.

In the standard PWM methods, CMV takes the values of  $\pm V_{dc}/6$  or  $\pm V_{dc}/2$ . PWM methods that eliminate the  $\pm V_{dc}/2$  level have been developed such that CMV is limited to  $\pm V_{dc}/6$ . The recently developed Reduced CMV PWM (RCMV-PWM) methods such as AZSPWM1 [2], RSPWM [3], and AZSPWM2 [4] exhibit performance constraints that prohibit their practical utilization [5]. This paper proposes a new RCMV-PWM method, the Near State PWM (NSPWM) method, that exhibits low CMV, prevents instantaneous polarity reversals of line-to-line voltages, and has satisfactory PWM ripple performance. First, the NSPWM method is described via space vector approach and its voltage linearity region is illustrated. Following, the performance characteristics of the method are studied in detail. The motor harmonic current and DC link harmonic current characteristics of the method are thoroughly investigated and compared to conventional methods. Detailed computer simulations of a motor drive illustrating the motor current ripple characteristics and detailed laboratory experiments demonstrating the CMV/CMC performance of the method are provided. Finally the experimental line-to-line voltage pattern performance of the method which illustrates its satisfactory performance for long cable application is demonstrated.

## The Near State PWM (NSPWM) Method

The Near State PWM (NSPWM) method utilizes a group of three neighbor voltage vectors to match the output and reference volt-seconds. These three voltage vectors are selected such that the voltage vector closest to reference voltage vector and its two neighbors (to the right and left) are utilized. Therefore, the utilized voltage vectors are changed in every  $60^\circ$  throughout the space. As shown in Fig. 2.a, to apply the method, the voltage vector space is divided into six segments. Defined with indices, voltage vectors  $V_{i-1}$ ,  $V_i$ , and  $V_{i+1}$  are utilized for region Bi. For example, for the region between  $30^\circ$  and  $90^\circ$  (B2), the applied voltage vectors are  $V_1$ ,  $V_2$ , and  $V_3$  (Fig. 2.b). As a result the PWM pulse pattern of the method in this region becomes as shown in Fig.2.c. Notice that phase ‘‘c’’ is not switched within this cycle (thus over B2).

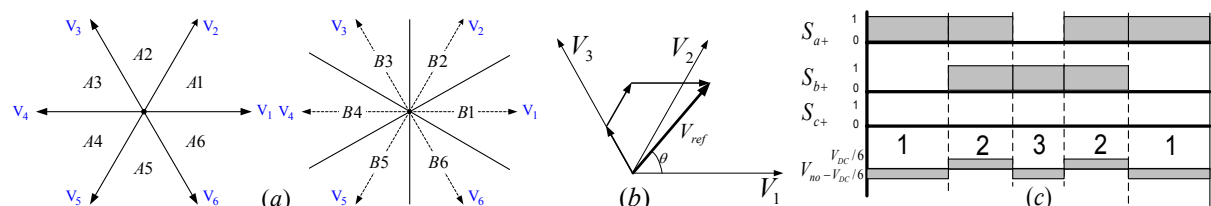


Fig. 2: Voltage vectors and pulse patterns, (a) Voltage vectors and  $60^\circ$  sector definitions, (b) Synthesis of NSPWM voltages for B2 (c) Pulse pattern of NSPWM for B2

Utilizing the above defined near state voltage vectors, the complex variable volt-seconds balance equation and the PWM period constraint for NSPWM can be written in generalized form for region Bi in equations (2.a) and (2.b) where  $T_s$  is the PWM period. Normalizing the voltage vector on-time values, the vector duty cycles can be found as  $d_k = t_k / T_s$ , where  $k: i-1, i, i+1$ . Utilizing (2.a) and (2.b), the duty cycles of the required voltage vectors can be calculated for region Bi as in (3), (4), and (5).

$$V_{i-1}t_{i-1} + V_i t_i + V_{i+1}t_{i+1} = V_{ref} T_s \quad (2.a)$$

$$t_{i-1} + t_i + t_{i+1} = T_s \quad (2.b)$$

$$d_{i-1} = 1 - \frac{2\sqrt{3}}{\pi} M_i \sin\left(\theta - \frac{(i-2)\pi}{3}\right) \quad (3)$$

$$d_i = -1 + \frac{3}{\pi} M_i \cos\left(\theta - \frac{(i-2)\pi}{3}\right) + \frac{3\sqrt{3}}{\pi} M_i \sin\left(\theta - \frac{(i-2)\pi}{3}\right) \quad (4)$$

$$d_{i+1} = 1 - \frac{3}{\pi} M_i \cos\left(\theta - \frac{(i-2)\pi}{3}\right) - \frac{\sqrt{3}}{\pi} M_i \sin\left(\theta - \frac{(i-2)\pi}{3}\right) \quad (5)$$

In the above equations,  $\theta = \omega_c t$  is the angle of the reference voltage vector, and  $M_i$  is the modulation index ( $M_i = V_m / (2V_{dc}/\pi)$ ) [1]. Equations (3), (4), and (5) yield a valid solution only in region LR shown in Fig. 3.a and there is no solution elsewhere. A method with acceptable performance should be used in NLR1. In the modulation algorithm shown in Fig.3.b, in NLR1, if low RCMV is required AZSPWM1, or if lower PWM ripple is required SVPWM or DPWM methods should be employed. The transition between NSPWM and the alternative method can be done seamlessly and has no effect on the drive performance. Region LR, where (3), (4), and (5) have a valid solution, corresponds to per fundamental cycle voltage linearity between  $M_{iLmin} = \pi / (3\sqrt{3}) \cong 0.61$  and  $M_{iLmax} = \pi / (2\sqrt{3}) \cong 0.907$ . For the shaded region of Fig. 3.a, where NSPWM has a valid solution, the three voltage vectors may be combined in various sequences to program the required output voltage. With the constraints of minimum switching count, no simultaneous switchings of phase legs, and minimum CMV, only the sequence of  $V_{i+1}-V_i-V_{i-1}-V_i-V_{i+1}$  as a general form for region Bi remains feasible. For example, between  $30^\circ$  and  $90^\circ$  (B2), the optimal sequence is  $V_3-V_2-V_1-V_2-V_3$ . In this sequence state changes occur only between adjacent states and this is the only sequence which does not require simultaneous switching of the inverter legs. The sequences of NSPWM and other methods are shown in Table I for region definitions of Fig. 2.a. Given this sequence, CMV of NSPWM varies between  $-V_{dc}/6$  and  $+V_{dc}/6$  as shown in Fig. 2.c and its low value is favored as will be detailed in later sections.

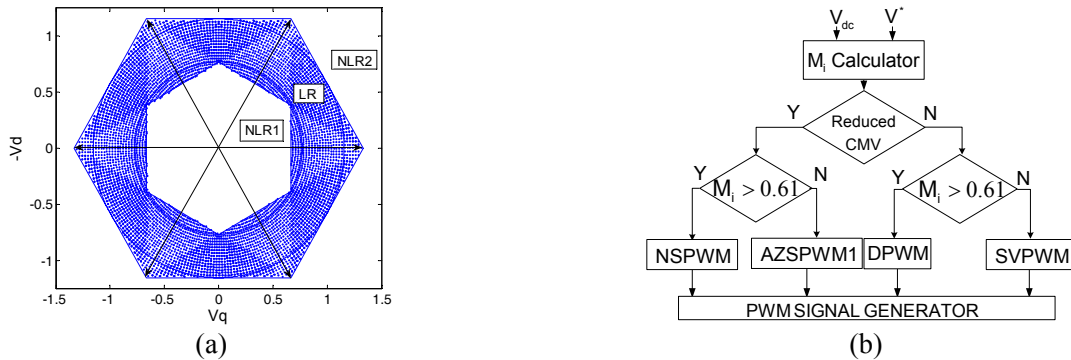


Fig. 3: Modulator voltage linearity characteristics and modulator choice; (a) Voltage linearity range of NSPWM (vectors normalized to  $V_{dc}/2$ ), (b) The flowchart of a combined modulation algorithm

Table I: Voltage Vector Patterns Of Various PWM Methods

	A1	A2	A3	A4	A5	A6
CPWM	7210127	7230327	7430347	7450547	7650567	7610167
AZSPWM1	3216123	4321234	5432345	6543456	4561654	5612165
	B1	B2	B3	B4	B5	B6
NSPWM	21612	32123	43234	54345	65456	16561

The practical implementation of NSPWM is similar to that of DPWM methods and can be implemented by scalar PWM approach. Its pulse pattern can be easily programmed by modern DSPs with flexible PWM modules (such as TI TMS320F2808 which has 6 pairs of CompA/CompB registers). Note that the space vector approach is mainly utilized to illustrate the principle of the method while the practical implementation preferably involves the scalar PWM approach. In the scalar approach, simple signal comparisons and zero sequence signal injection yield the discontinuous PWM pattern of NSPWM [5].

## Inverter Output Voltage/Current Harmonic Distortion Characteristics

The inverter output voltage waveform quality can be best studied with the aid of space vectors. The difference between the reference voltage vector and output voltage vector corresponds to the harmonic voltage vector. Since the switching frequency model of motor drives is the motor leakage inductance, the integral of the harmonic voltage vector is proportional to the harmonic current and therefore to the torque ripple in motor drives. Thus, output voltage waveform quality is generally investigated in terms of the normalized harmonic flux vector defined in (6) over an arbitrary PWM cycle ( $N^{\text{th}}$  cycle).

$$\lambda_{hn}(M_i, \theta, V_{dc}) = \frac{\pi}{V_{dc} T_s} \int_{NT_s}^{(N+1)T_s} (V_k - V_{ref}) dt \quad (6)$$

Since each PWM method differs in the utilization of the voltage vectors and their sequence, the harmonic flux vector of each PWM method is unique. The harmonic flux trajectories of each PWM method vary depending on the angle and magnitude of the reference voltage vector. The harmonic voltage vector and harmonic flux trajectories of NSPWM are illustrated in Fig. 4. The trajectory resembles a butterfly shape. The butterfly's wings and size change with  $M_i$  and  $\theta$ . As Fig. 5.a illustrates for constant  $\theta$ , as  $M_i$  increases the harmonic flux trajectories get noticeably narrower. However, as Fig. 5.b illustrates, the  $\theta$  dependency of harmonic flux trajectories is not strong. Although the shapes of harmonic flux trajectories are different for different  $\theta$  values, all have similar size. In order to show the harmonic content clearly, the magnitude of the harmonic flux vector is illustrated over a half PWM cycle with the time axis normalized to  $T_s$  in Fig. 5.c. As the figure illustrates, the harmonic content slightly decreases as  $\theta$  approaches  $60^\circ$ .

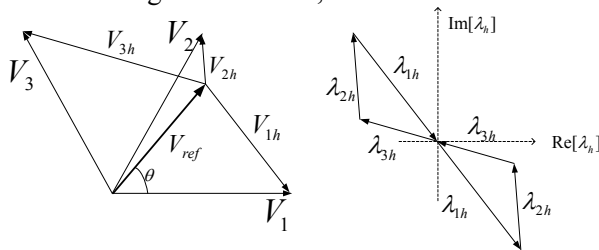


Fig. 4: Harmonic voltage vectors and corresponding harmonic flux trajectories of NSPWM for B2

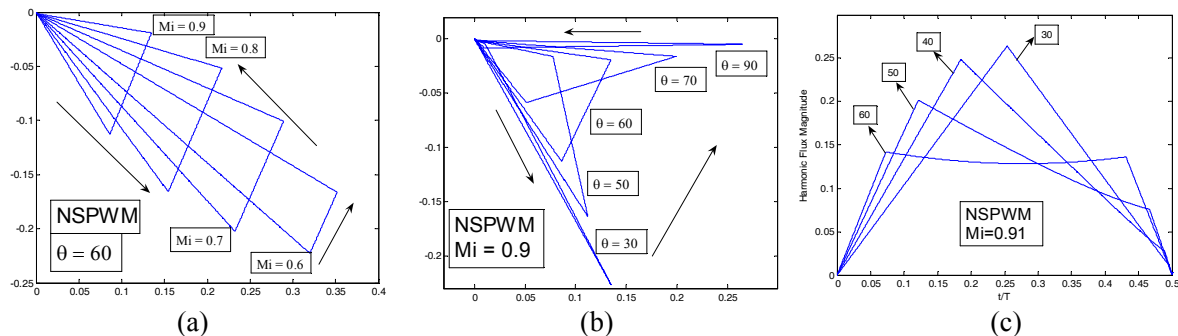


Fig. 5: Complex plane harmonic flux trajectories (a) & (b) and time dependent harmonic flux magnitude (c)

In the following, the NSPWM harmonic flux trajectories will be discussed in comparison with those of DPWM1. Here DPWM1 is taken as base because for approximately  $M_i \geq 0.6$ , it has the best overall performance among conventional PWM methods [1], both methods have discontinuous switching, and their practical  $M_i$  range is also the same. Therefore it is expected that their harmonic fluxes to be similar. Figure 6 shows the harmonic flux trajectories of both methods for  $M_i=0.9$  and two angles,  $\theta=30^\circ$  and  $\theta=60^\circ$ . In the figure the harmonic flux magnitudes over a half PWM cycle are also shown. For  $M_i=0.9$  and  $\theta=30^\circ$ , the duration of the zero vector for DPWM1 and duration of  $V_3$  for NSPWM are zero and both methods utilize the same voltage vectors with the same duration (Fig. 6, left). Therefore the shapes and

magnitudes of harmonic flux trajectories of both methods are the same. As  $\theta$  approaches  $60^\circ$ ,  $V_3$  for NSPWM and  $V_0$  for DPWM1 become more dominant (Fig. 6, right). Therefore, harmonic flux trajectories of the two methods differ. For all operating points other than  $\theta=30^\circ$ , the magnitudes of harmonic flux vectors of NSPWM become slightly larger than those of DPWM1. Therefore, DPWM1 has less ripple than NSPWM in general, although the difference is space dependent and typically small. The harmonic flux trajectories are not convenient for overall comparison of ripple performance of PWM methods. For this purpose, the below defined integral quantities are employed.

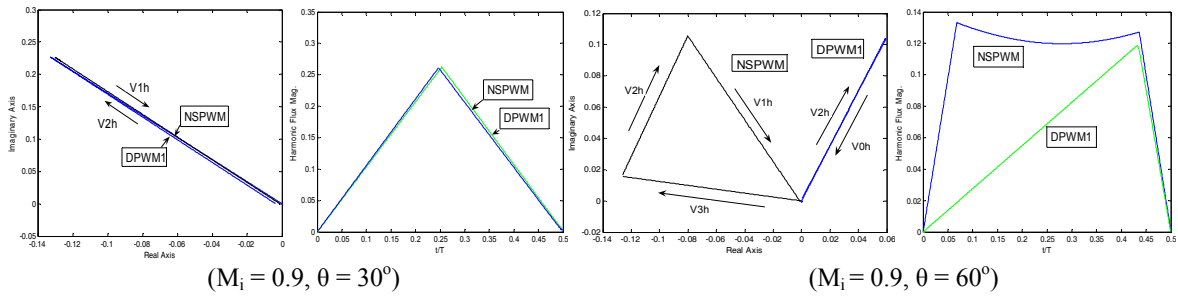


Fig. 6: Harmonic flux trajectories and magnitudes for DPWM1 and NSPWM

The RMS harmonic flux over a PWM cycle (duty cycle  $\delta$  of 0 to 1),  $\lambda_{hn-rms}$ , and Harmonic Distortion Factor (HDF), which is the normalized form of  $\lambda_{hn-rms}$  over the full fundamental cycle, are the per PWM cycle (local) and per fundamental cycle (global) harmonic performance indices given as follows.

$$\lambda_{hn-rms}(M_i, \theta) = \sqrt{\int_0^1 \lambda_{hn}^2 d\delta} \quad (7) \quad HDF = f(M_i) = \frac{288}{\pi^2} \frac{1}{2\pi} \int_0^{2\pi} \lambda_{hn-rms}^2 d\theta \quad (8)$$

The local RMS harmonic flux characteristics of various PWM methods, including NSPWM, DPWM1, and other methods such as SVPWM are numerically evaluated under the criteria of equal average switching frequency for  $M_i=0.61$  and  $M_i=0.9$  and are illustrated in Fig. 7.a and 7.b respectively. At  $M_i=0.61$ , the harmonic content of NSPWM is significantly higher than CPWM and DPWM methods. However, it is flat and much lower than other RCMV-PWM methods. At  $M_i=0.9$ , the RMS harmonic flux of NSPWM is significantly less than SVPWM and RCMV-PWM methods, but slightly inferior to DPWM.

The HDF characteristics of the above discussed methods are all numerically calculated and shown in Fig. 8. Since NSPWM is linear in the  $0.61 < M_i < 0.907$  range, its curve is provided for a narrower range than other methods. Throughout its linearity range, NSPWM has the least harmonic distortion among all RCMV-PWM methods. In its lower linear  $M_i$  range, NSPWM has higher harmonic content than the conventional PWM methods. In the higher end of the linear modulation range, NSPWM performs better than CPWM methods and comparably with DPWM methods.

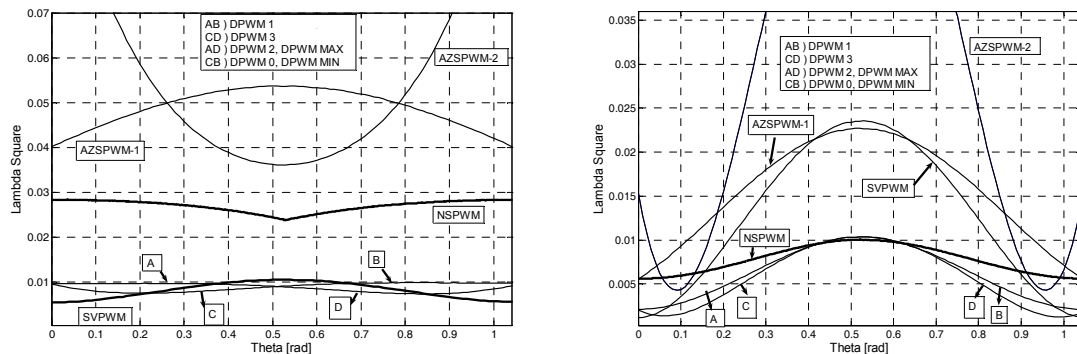


Fig. 7: (a)  $\lambda_i^2=f(\theta)$  spatial variation for  $M_i=0.61$ , (b)  $\lambda_i^2=f(\theta)$  spatial variation for  $M_i=0.9$

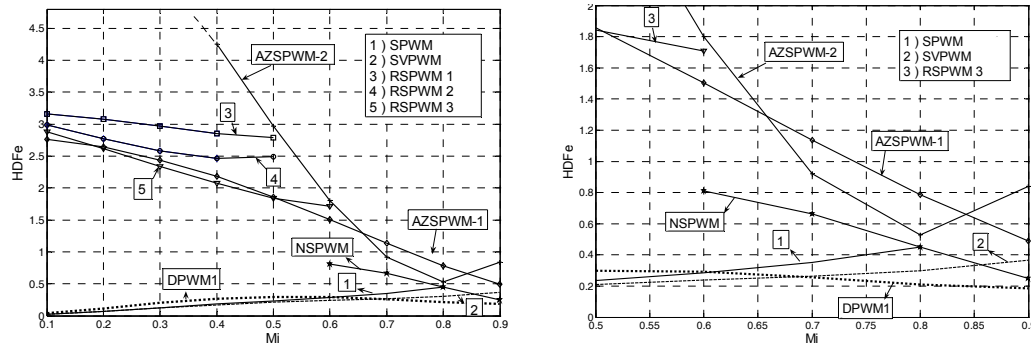


Fig. 8:  $HDF_e = f(M_i)$  for various PWM methods (left), zoom in view of the right half (right)

## DC Link Current Ripple Characteristics

The DC link current of the inverter  $i_{in}$  (Fig. 1) is important for DC bus capacitor sizing as the capacitor suppresses all PWM ripple current. The DC link ripple current has limiting effect on the capacitor lifetime so it should be as small as possible. Each PWM method has a unique DC link current ripple characteristic. Defined in (9),  $K_{dc}$  is the ratio of DC link current ripple square to output phase current RMS value square. Smaller  $K_{dc}$  implies smaller capacitor requirement and longer capacitor life. For NSPWM,  $K_{dc}$  is analytically calculated in (10) as a function of  $M_i$  and load power factor (PF) angle  $\varphi$ .

$$K_{dc} = I_{inrms}^2 / I_{1rms}^2 \quad (9)$$

$$K_{dc}^{NSPWM} = 1 + (M_i \frac{24}{\pi^2} - \frac{3\sqrt{3}}{2\pi}) \cos 2\varphi - M_i^2 \frac{18}{\pi^2} \cos^2 \varphi \quad (10)$$

In Fig. 9,  $K_{dc}$  curves of various PWM methods including NSPWM are illustrated as a function of  $M_i$  with PF as parameter. The DC link harmonic content of NSPWM is strongly dependent on PF and  $M_i$ .  $K_{dc}$  of NSPWM decreases with increasing  $M_i$  and PF. For PF=1, NSPWM has lower DC link ripple content than all other PWM methods. For PF of 0.8-0.9,  $K_{dc}$  of all PWM methods are similar. However, for PF lower than approximately 0.6,  $K_{dc}$  of NSPWM is inferior to other methods. At high PF, the superior  $K_{dc}$  of NSPWM can be explained by observing the per-carrier cycle behavior of the inverter. The DC link current is formed from current pulses associated with the inverter voltage vectors utilized. Since each PWM method has a unique PWM pulse pattern, the resulting DC link current also is unique to the method. Fig. 10 illustrates the DC link current of NSPWM and DPWM1 within a PWM cycle for unity and zero PF (lagging) load current,  $M_i=0.78$ ,  $\theta=45^\circ$ , for region B2. For PF=1, the DC link current pulses of NSPWM are closer to their average value compared to DPWM1. Spanning the whole vector space, the voltage vectors and their sequence and the phase currents (their magnitude and polarities) change, but the tendency of DC link current ripple remains the same. Hence, NSPWM has smaller  $K_{dc}$ . At low power factor, this relation reverses and NSPWM performs poorly. For practical motor drive applications, at full-load PF approaches unity and the motor runs at the rated current. Although the motor current is large, due to high PF,  $K_{dc}$  is small. At no-load, the motor PF is poor but the motor current is quite small compared to rated case. Here,  $K_{dc}$  is large but the ripple current remains small compared to that of the rated load operating condition. As a result the capacitor ripple current becomes small over the complete operating range of the drive. Therefore, with NSPWM, the DC bus capacitor can be smaller compared to the conventional PWM methods.

It is worth mentioning that one basic property of NSPWM is that the DC link current is always present since always active inverter states are utilized. Utilizing the inverter switch state information along with only the DC link current measurement, the three phase currents can be reconstructed (for utilization in the motor control algorithm) and low cost current measurement can be achieved.

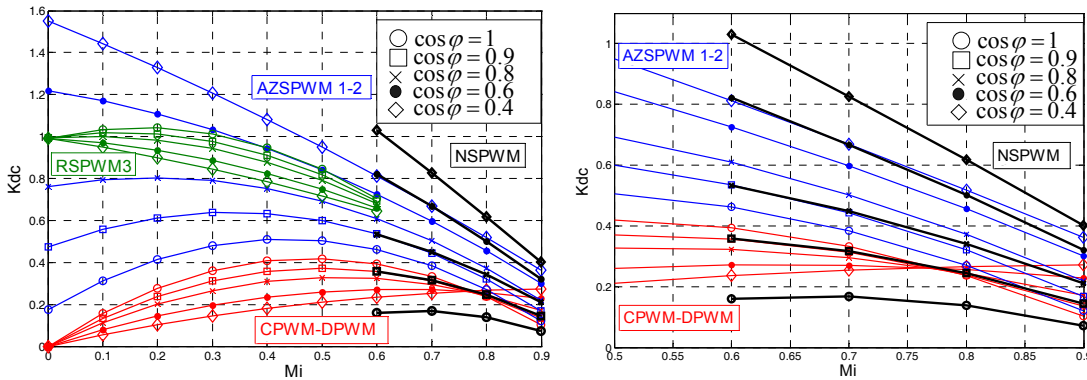


Fig. 9:  $K_{dc}=f(M_i, \cos\phi)$  for various PWM methods (left), zoom in view (right)

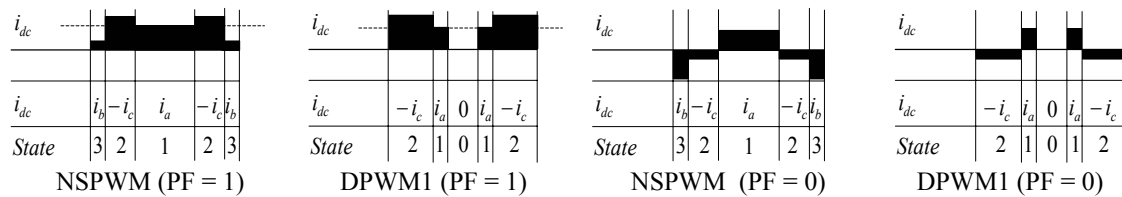


Fig. 10: DC link current waveforms for NSPWM and DPWM1 for  $M_i = 0.78 \theta = 45^\circ$

### CMV and Line-to-line Voltage Pulse Patterns

The pulse pattern of NSPWM is different from the pattern of conventional PWM methods. As a result, the Common Mode Voltage (CMV) pattern and the inverter output voltage pattern are different from the conventional patterns. While the CMV characteristics of NSPWM are favorable over the conventional methods, the line-to-line voltage pulse pattern may be problematic depending on the application. In the following, these issues will be addressed.

The inverter leg upper switch logic, CMV, and line-to-line voltage patterns for NSPWM, SVPWM, DPWM1, and AZSPWM1 are shown in Fig. 11. SVPWM and DPWM1 have high CMVs (limits:  $\pm V_{dc}/2$ ). NSPWM and AZSPWM1 reduce the CMV (limits:  $\pm V_{dc}/6$ ). This is the main advantage of RCMV-PWM methods. Although the CMVs of RCMV-PWM methods are less than those of the conventional methods, the rate of change of CMV is the same for all methods. During a switching transition CMV always changes by  $|\Delta V|=V_{dc}/3$ . Thus the capacitive CMC during the switching transition is similar. Therefore, during switching transients CMC is high and comparable in all methods, while between switching instants the CMC of RCMV-PWM methods is significantly lower than other methods. As a result NSPWM has lower CMV, CMC, and leakage current than conventional methods and is more motor friendly [5].

In motor drive applications involving long cables, two consecutive voltage pulses with opposite polarity must be separated by a sufficient time interval to damp the switching induced overvoltage due to voltage reflection. Methods with bipolar pulse pattern are not favorable unless the pulses are safely distant from each other. As Fig. 11 shows, the inverter output line-to-line voltage patterns of CPWM/DPWM methods are unipolar such that the polarity of the line-to-line voltage does not change within a PWM cycle (there is pulse-polarity consistency). In AZSPWM1 always 2 of 3 line-to-line voltages have bipolar pattern while in NSPWM only one of them has bipolar pattern. One of the NSPWM phases is not switching within a PWM cycle while the AZSPWM1 switches are manipulated periodically. In NSPWM, when a pulse reversal occurs in the bipolar line-to-line voltage, there is always a sufficient zero voltage time between the positive and negative pulses. The narrowest time interval that occurs (at the edges of Bi regions,  $30^\circ$ ,  $90^\circ$ , etc.) is a function of  $M_i$  and it starts at 0 for  $M_i=0.61$ , rapidly increases with  $M_i$ , and typically loses criticality at  $M_i=0.65$  [5]. In AZSPWM1, regardless  $M_i$  the narrowest interval is zero meaning rapid line-to-line voltage reversals and large overvoltages at the motor terminals in long cable applications.

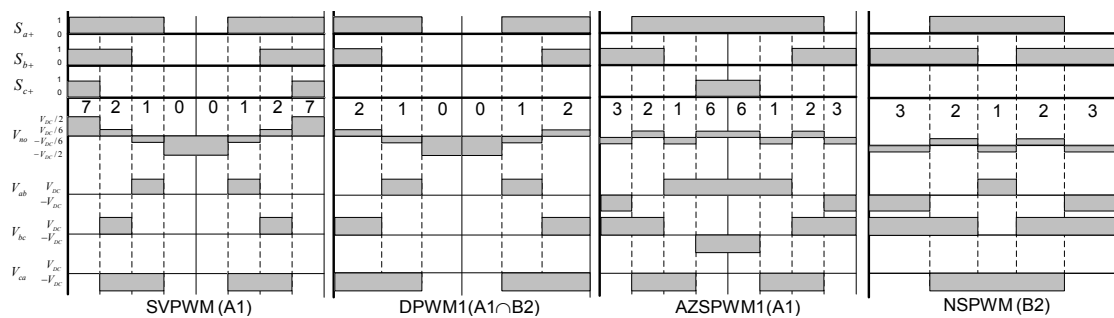


Fig. 11: PWM Pulse pattern of SVPWM, DPWM1, AZSPWM1, and NSPWM methods

## Computer Simulations Illustrating The Output Current Ripple Performance

To illustrate the output current PWM ripple characteristics of NSPWM and other methods, a 4-kW, 380-V, 4-pole, 1440-min<sup>-1</sup> induction motor driven by an inverter has been simulated. The drive is at no-load, and constant V/f algorithm is employed (176.7 V<sub>rms</sub>/50 Hz). The DC bus voltage is fixed at 500 V. The PWM ripple performance of NSPWM is investigated and compared to various PWM methods. The carrier frequency is 6.66 kHz for SVPWM and AZSPWM1. For NSPWM and DPWM1 10 kHz is utilized ( $f_{s\_ave}=6.66$  kHz). All methods are simulated for various  $M_i$  values and the motor phase current waveforms at  $M_i=0.6$  (137.6 V<sub>rms</sub>/38.8 Hz) and  $M_i=0.9$  (201.4 V<sub>rms</sub>/57.3 Hz) corresponding  $M_{iL,min}$  and  $M_{iL,max}$  of NSPWM respectively are shown in Fig. 12. At  $M_i=0.6$ , SVPWM and DPWM1 have the least harmonic content, while AZSPWM1 is inferior to all. NSPWM current ripple is significantly space dependent but on the average it is superior to AZSPWM1. At  $M_i=0.9$ , where the maximum linearity point is approached, NSPWM is comparable to DPWM1 and slightly better than other methods in terms of current ripple.

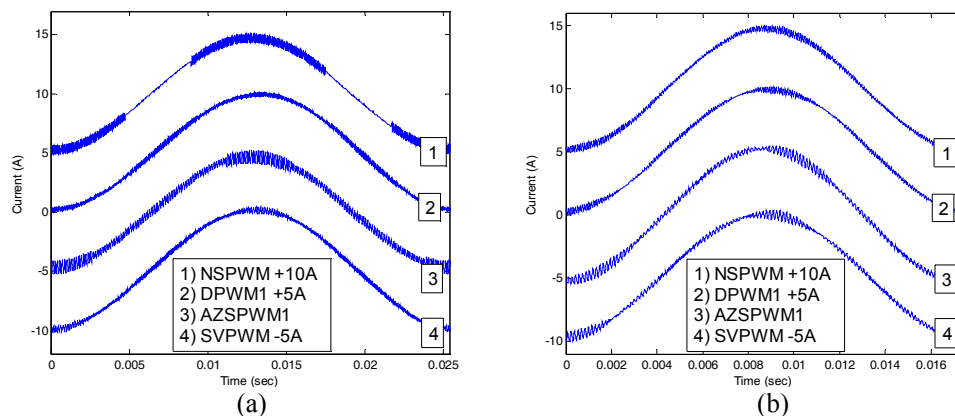


Fig. 12: Output current waveforms various PWM methods (a)  $M_i=0.6$  and (b)  $M_i=0.9$

## Experimental Results

To evaluate the overall performance of NSPWM and compare it to other methods, the experimental set-up shown in Fig. 13, which is suitable for CMC and pulse reversal based overvoltage measurement is established [5]. A DSP (TMS320F2808) is utilized to control the motor speed and program the PWM pulse pattern. The motor and drive ratings and parameters are the same as those in the simulations. Figure 14 shows the phase current, CMC, CMV and the modulation signals for NSPWM, SVPWM, and DPWM1 at  $M_i=0.8$ . The phase current waveforms are sinusoidal and the PWM current ripple is comparable in all the methods as predicted in the simulations. The CMV comparison indicates that both DPWM1 and SVPWM have high CMV compared to NSPWM. Comparing the CMC characteristics, the difference is not as emphasized as the CMV characteristic, because  $dv/dt$  is the same and dominant. At the switching instants sharp edge voltage pulses (measured as approximately 3.6 kV/ $\mu$ s) cause large magnitude high frequency currents through the capacitive paths in all methods. Differences are still notable in terms of



rms and peak values. The microscopic view in Fig. 14 (right), which shows the PWM cycle CMV/CMC waveforms, reveals the details. Since the PWM pulse pattern varies over a fundamental cycle, the PWM characteristics are  $\theta$  dependent. As a result, the CMV/CMC characteristics also vary in space. When comparing the CMV/CMC characteristics, the worst CMV/CMC points are selected for each method and shown in the oscillograms. It can be seen that the CMV of DPWM1 and SVPWM are quite larger than those of NSPWM. The peak values of CMCs for all the methods are similar. The RMS value of CMC is slightly better for NSPWM compared to other methods.

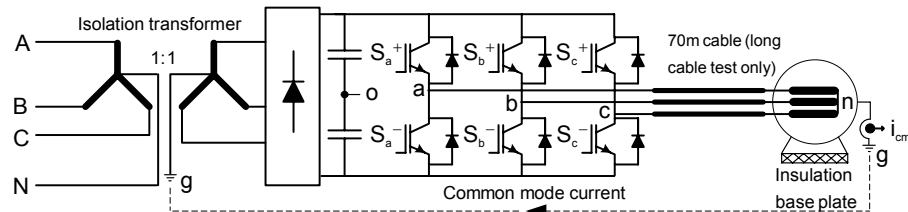


Fig. 13: Experimental setup for PWM current ripple, CMV/CMC, and voltage reflection measurements

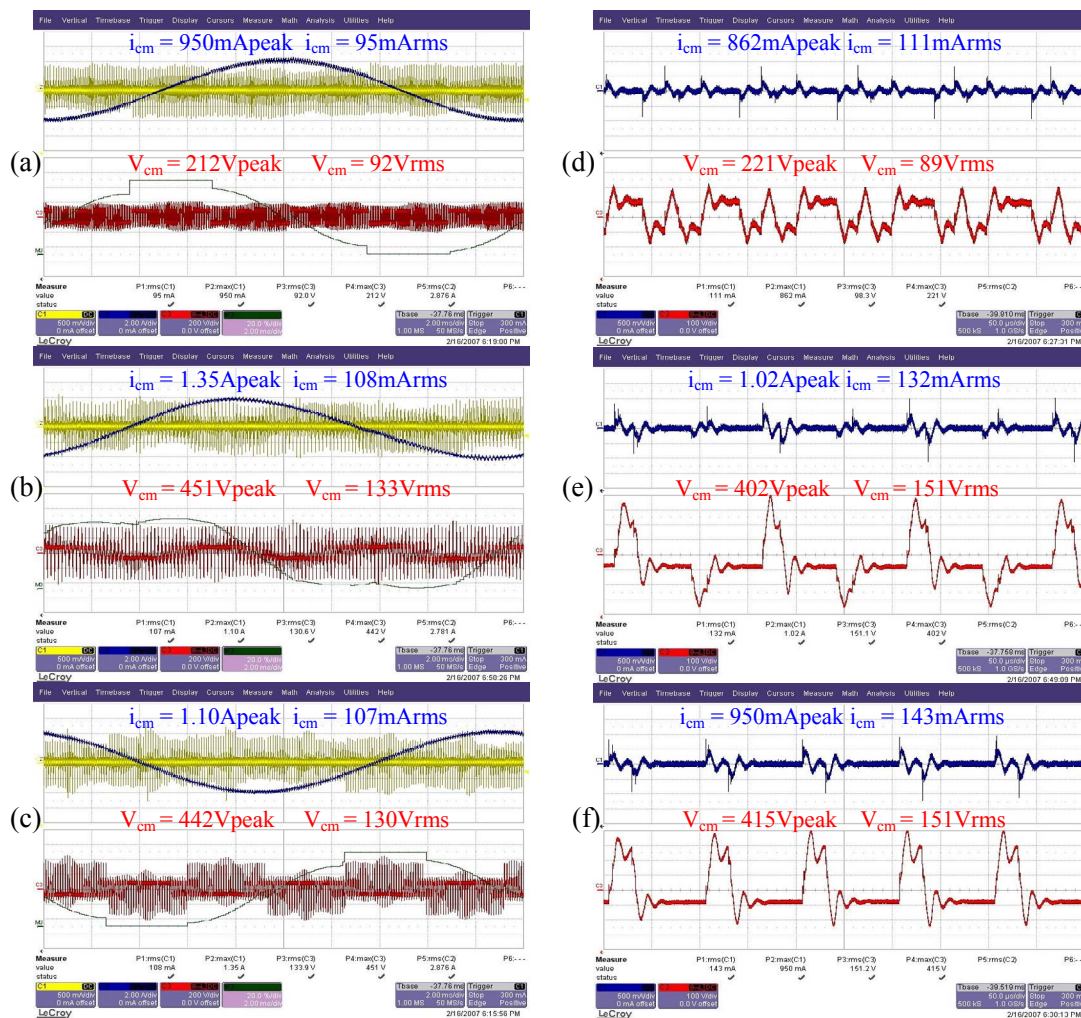


Fig. 14: Experimental waveforms, left: phase current (blue, 1A/div), CMC (yellow, 0.5A/div), CMV (red, 200V/div), modulation signal (green, 0.5V/div) waveforms at M<sub>i</sub>=0.8 for (a) NSPWM (f<sub>s</sub>=10kHz), (b) SVPWM (f<sub>s</sub>=6.6kHz), (c) DPWM (f<sub>s</sub>=10kHz), right: zoom in view of the CMC (blue 0.5 A/div) and CMV (red 350V/div) waveforms for the worst case operating condition (d) NSPWM, (e) SVPWM, (f) DPWM

The line-to-line voltage pulse pattern of NSPWM is superior to AZSPWM1 as discussed in an earlier section. The experimental waveform of Fig. 15 shows that NSPWM places sufficient zero voltage time interval before pulse reversal occurs while the AZSPWM1 method experiences rapid change with nearly zero time interval between pulses. As shown in the figure, in the worst case, in this long cable application (70m), the AZSPWM1 method exhibits overvoltages ( $>1400V$ ) while NSPWM performs satisfactorily.

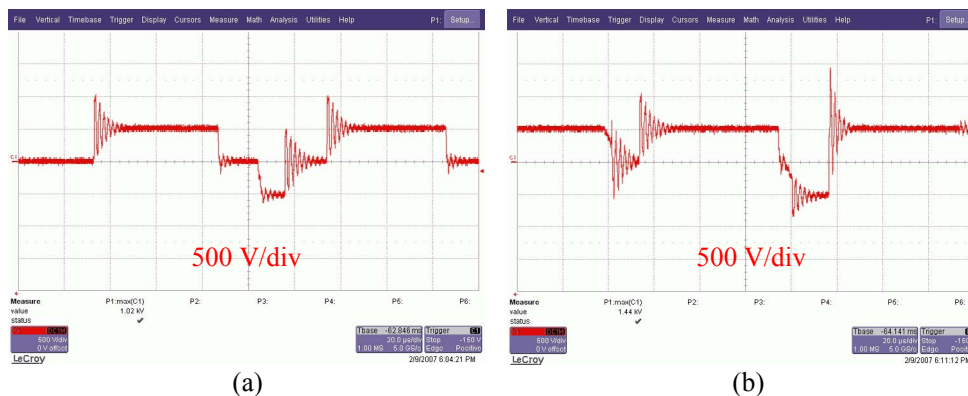


Fig. 15: Line-to-line voltage pulse reversal ( $M_i=0.8$ ): (a) NSPWM ( $f_s=10kHz$ ), (b) AZSPWM1 ( $f_s=6.6kHz$ )

## Conclusions

The NSPWM method, which has low CMV and reduced switching losses compared to conventional PWM methods, is proposed. Utilizing the space vector approach the vector duty cycles of the method are calculated. The optimal vector sequence is determined and simple scalar implementation is discussed. The output phase current and DC link current harmonic characteristics of NSPWM are investigated and it is shown that they are better than those of other RCMV-PWM methods and comparable with those of standard PWM methods. The method has lower CMV than conventional methods and results in lower CMC. The line-to-line voltage pulses of the method are partially bipolar and pulse reversals occur, in a similar manner to other RCMV-PWM methods. However, in NSPWM there is always sufficient distance between the voltage pulses such that line-to-line voltage pulse reversal of NSPWM does not cause significant overvoltages (unlike AZSPWM1). Computer simulations illustrating the PWM ripple performance of NSPWM and comparing to other methods are provided. Detailed laboratory experiments illustrating the PWM current ripple performance, CMV, and CMC characteristics are conducted. The results show that NSPWM has superior overall performance over its voltage linearity range. Furthermore, the long cable test with 70m cable shows that line-to-line voltage pulse reversals do not cause significant overvoltages. Thus, the method is a favorable method for motor drive applications operating in the upper half of the linear modulation range ( $M_i > 0.6$ ). The method must be combined with a method with high CMV/CMC performance and low current ripple for  $M_i < 0.6$  for practical use.

## References

- [1] A.M. Hava, R.J. Kerkman, T.A. Lipo, "Simple analytical and graphical methods for carrier-based PWM-VSI drives," *IEEE Trans. on Power Electronics*, vol. 14, no: 1, pp. 49 – 61. Jan. 1999.
- [2] Y.S. Lai, F.S. Shyu, "Optimal common-mode voltage reduction PWM technique for inverter control with consideration of the dead-time effects-part I: basic development," *IEEE Trans. on Ind. Applicat.*, vol 40, no. 6, pp.1605 – 1612. Nov.-Dec. 2004.
- [3] M. Cacciato, A. Consoli, G. Scarcella, A. Testa, "Reduction of common-mode currents in PWM inverter motor drives," *IEEE Trans. on Ind. Applicat.*, vol. 35, no 2, pp. 469 – 476. March-April 1999.
- [4] E. Ün, A.M. Hava, "Performance analysis and comparison of reduced common mode voltage PWM and standard PWM techniques for three-phase voltage source inverters," *IEEE-APEC Conf.*, pp. 303-309, March 19-23, 2006.
- [5] E. Ün, A.M. Hava "A Near State PWM Method With Reduced Switching Frequency And Reduced Common Mode Voltage For Three-Phase Voltage Source Inverters" *IEEE-IEMDC Conf.*, pp. 235-240, May 2-5, 2007.