ANALYSIS, DESIGN, AND IMPLEMENTATION OF A 5 KW ZERO VOLTAGE SWITCHING PHASE-SHIFTED FULL-BRIDGE DC/DC CONVERTER BASED POWER SUPPLY FOR ARC WELDING MACHINES

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ABSTRACT

ANALYSIS, DESIGN, AND IMPLEMENTATION OF A 5 KW ZERO VOLTAGE SWITCHING PHASE-SHIFTED FULL-BRIDGE DC/DC CONVERTER BASED POWER SUPPLY FOR ARC WELDING MACHINES

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Modern arc welding machines utilize controllable high frequency DC/DC power supply with high dynamic and steady state current regulation performance. In the design robustness, small size and low weight, low complexity, and high efficiency are the defining criteria. The most suitable approach for a 5 kW arc welding machine power supply application is the high frequency Full-Bridge Phase-Shifted Zero Voltage Switching (FB-PS-ZVS) DC/DC converter with an isolation transformer. This converter not only gives the advantage of zero voltage switching for a wide load current range, it also provides reduced Electromagnetic Interference (EMI) and reduced component stress compared to standard PWM converters. In this thesis a FB-PS-ZVS DC/DC converter with 5 kW power rating is designed for modern arc welding machine applications. IGBTs are utilized at 50 kHz switching frequency for high efficiency and control bandwidth. The output current of the DC/DC converter is controlled via a Digital Signal Processor (DSP) control platform. The performance of

the designed DC/DC converter is evaluated via the computer simulations and the experimental study of the constructed prototype.

Keywords: Power supply, DC/DC, full-bridge DC/DC converter, zero voltage switching, phase-shifted PWM, arc welding.

ÖZ

ARK KAYNAĞI MAKİNALARI İÇİN 5 KW SIFIR GERİLİMDE ANAHTARLAMALI FAZ-KAYMALI TAM-KÖPRÜ DC/DC DÖNÜŞTÜRÜCÜ TABANLI GÜÇ KAYNAĞININ ANALİZ, TASARIM VE İMALATI

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Modern kaynak makinaları dinamik ve statik akım regülasyon performansı yüksek olan yüksek frekans DC/DC güç kaynağı kullanmaktadır. Tasarımda sağlamlık, küçük boyut ve hafiflik, basitlik ve yüksek verimlilik tanımlayıcı özelliklerdir. 5 kW'lık bir ark kaynak makinası için en uygun güç kaynağı yaklaşımı yüksek frekanslı, izolasyon transformatörlü, faz-kaymalı sıfır gerilimde anahtarlamalı tam-denetimli köprü (FB-PS-ZVS) DC/DC dönüştürücüdür. FB-PS-ZVS DC/DC dönüştürücü geniş bir yük akımı çalışma bölgesinde sıfır gerilimde anahtarlama üstünlüğüne ek olarak, düşük elektromanyetik gürültü açısından da standart DC/DC dönüştürücülerden üstündür. Bu tezde ark kaynağı uygulamaları için 5 kW'lık bir FB-PS-ZVS DC/DC dönüştürücü tasarımı verilmiştir. Yüksek verim ve denetim bantgenişliği için IGBT anahtarlar 50 kHz'de kullanılmıştır. DC/DC dönüştürücü yük akım denetimini sayısal işaret işleyici tabanlı bir denetim platformu sağlamaktadır. Tasarımı yapılan dönüştürücünün başarımı, bilgisayar benzetimi ve

imal edilen dönüştürücü prototipiyle yapılan deneysel çalışmalarından elde edilen sonuçlarla değerlendirilmiştir.

Anahtar Kelimeler: Güç kaynağı, DC/DC, Tam-denetimli köprü DC/DC dönüştürücü, sıfır gerilimde anahtarlama, faz-kaymalı darbe genişlik modülasyonu (PWM), ark kaynağı.

To My Parents,
Aynur and Mehmet Uslu
for their patience and support
in all aspects of my life

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CHAPTER 1

INTRODUCTION

1.1 Switch Mode Power Supplies

DC voltage power supplies are utilized in most electrical/electronic equipment in order to meet the power requirement of the electronic circuits in the equipment. The power supply used to obtain regulated DC voltage from AC power line may be either a linear regulator or a Switch Mode Power Supply (SMPS).

Linear regulators may be convenient for the power supply applications where the unregulated input voltage is close to and more than the desired regulated output voltage since inefficiency is the main drawback of these type of regulators. The low noise level and simplicity are the two advantages of the linear regulators.

The SMPS technology offers several advantages over the linear regulator technology such as higher efficiency, higher bandwidth (better regulation), smaller size, and lower weight. The semiconductor switching device in an SMPS is operated either in cut-off mode (blocking high voltages) or saturation mode (carrying high currents). Since no current flows through the semiconductor switch in cut-off (off) state and the voltage across the device is low in saturation (on) state, the conduction power loss is low. Likewise, the very high speed switching nature of the power semiconductors leads to low switching losses. Thus, the low conduction and switching losses result in higher efficiency of SMPSs than linear regulators. An SMPS regulates the output voltage closely in spite of the changes in the input supply voltage and the load current, with almost no change in efficiency. Due to the high operating switching frequencies of the semiconductor switching devices; transformers, inductors, and

capacitors utilized in an SMPS are getting smaller in size and lower in weight which results in smaller, lighter, and more economical power supplies.

The power range of an SMPS can be from several watts, up to hundreds of kilowatts. Typical applications of an SMPS include computer power supplies, house appliance power supplies, battery chargers, welding machines, telecommunication power supplies, DC motor drives, etc.

Generally an SMPS system consists of the basic elements presented in the block diagram in Figure 1.1 [1]. In an SMPS, when the unregulated input voltage is supplied from the AC grid, typically, the AC line voltage that is either single-phase or three-phase is rectified to DC voltage by a diode bridge rectifier. The diode bridge output voltage is filtered by a large electrolytic capacitor so that ripple voltage magnitude of the unregulated DC voltage is reduced. The heart of an SMPS system is formed by a switch mode DC/DC converter that outputs regulated DC voltage. The DC/DC converter block mainly utilizes power semiconductor devices (switches), passive filter components, and an isolation transformer when galvanic isolation is necessary. The power semiconductor devices may be either gate controlled switching devices including Bipolar Junction Transistors (BJTs), Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), Insulated Gate Bipolar Transistors (IGBTs) or uncontrolled (naturally commutated) devices which are power diodes. The passive components are utilized either for AC voltage and current conversion with isolation (transformers) or for energy storage (inductors and capacitors). The output sensor and controller block consists of measurement and control circuits. The measured DC/DC converter circuit variables such as load voltage, load current and input unregulated DC voltage are scaled and input to the controller for feedback purpose in order to regulate the output. The controller of the DC/DC converter can be implemented either by analog/digital hardware or by digital software. The control method is determined by utilizing the desired specifications of the system. An analog/digital hardware implementation has the main advantage of rapid response at the output to a change in the line or load due to the continuous sampling and processing. However, digital software implementations increase flexibility while

eliminating the dependence on environmental effects and aging, and reducing the amount of external hardware components. Complex control algorithms can also be implemented using digital software controllers in a simpler manner. The controller generates control signals for the Pulse Width Modulation (PWM) block which outputs the gate signals of the controllable semiconductor switch.

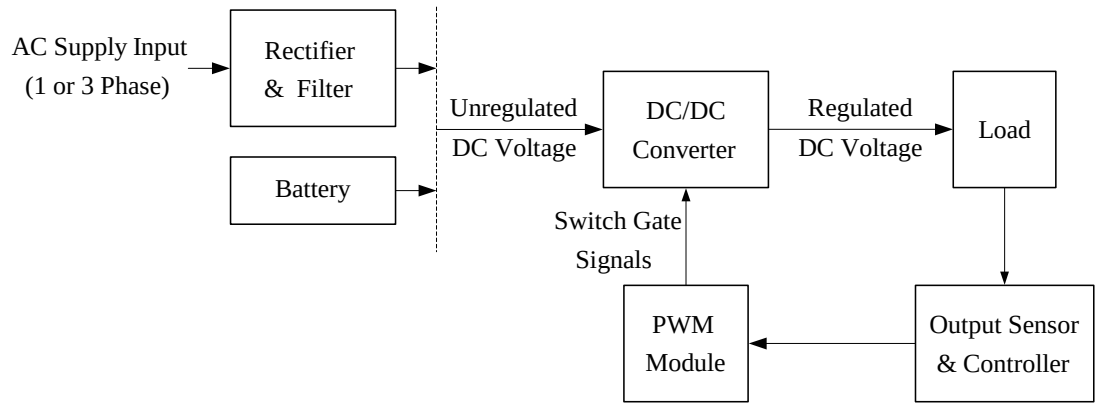


Figure 1.1 Generalized block diagram of an SMPS system.

The circuit topology of the switch mode DC/DC converter fully defines its functional attributes and performance [2]. There are various types of DC/DC converter circuit topologies utilized in SMPSs based on the system requirements such as input to output voltage relationship, power rating, and the need for galvanic isolation.

The simplest and most basic two DC/DC converter topologies are the step-down and step-up converters. All DC/DC converter topologies can be derived from these two. Derived from these, are the widely utilized single-switch flyback and forward converters that have electrical isolation between the input and output. Such converters are typically utilized at low power (much less than a kilowatt) and in low cost applications. At higher power, voltage, or current ratings more complex power converters become necessary. The half-bridge and full-bridge DC/DC converters which are derived from the step-down converter are the highest performance converters. When galvanic isolation and/or a significant voltage/current level change are required, these converters are accompanied with an isolation transformer also.

Industrial applications such as welding, plasma cutting, induction heating, and surface hardening require a large regulated DC current at low voltage. In such applications, the power ratings start at kilowatts and can reach hundreds of kilowatts. These applications generally require a power supply that behaves as a current source. Biomedical equipment such as X-Ray machines operate at a very high DC voltage, where voltage is increased via a step up transformer. Telecommunication systems require 48V regulated DC supplies and the power rating can be of several kilowatts and further increase in power may be required via paralleling such converters (in this case, also providing redundancy). This application requires a voltage source type power supply.

In some of the above applications such as welding power supplies, an isolation transformer is involved in trading the high input voltage for high output current required by the application. Thus, a step-down transformer is involved. The isolation transformer in applications such as welding and plasma cutting also provides safety measures. In most such applications the power rating is no less than a kilowatt and the highest power rating may exceed several hundred kilowatts. In all these applications the favorable power converter topology is the full-bridge DC/DC converter due to its high performance. With the circuit topology and control method being complex, design of such power converters becomes a nontrivial task. This thesis involves the detailed analysis, design, and implementation of the full-bridge DC/DC converter with the welding power supply application being the main application field.

Arc welding machines are widely used in industry such as in the processes of melting, joining, cutting etc. An arc welding machine power supply is required to control the load current/voltage in a wide range (e.g. 5 to 500 A, 14 to 40 V, and 80 V for ignition). Modern DC welding machines generally utilize switch mode DC/DC power supply which outputs high DC current and low DC voltage. Switch mode DC/DC power supplies can be operated at high switching frequencies due to the advances in semiconductor technology providing fast switches with small rise and fall times yielding high frequency operation with low loss. Due to the high switching

frequency operation of the DC/DC power supply, the size and weight of the welding machine can be reduced since the size of magnetic components in the power supply can be made smaller, which results in more light and portable welding machine. In such welding power supplies the size and weight are reduced while the performance is increased, which results in portable welding machines having improved welding quality. Another requirement of the welding power supplies is galvanic isolation between the input and output. Increasing switching frequency also increases the current control bandwidth, which is necessary for high quality weld. The workpiece where the welding action takes place, completes the electric circuit path at the output. For safety reasons, the input supply of the welding machine must be electrically isolated from output, where the arc load exists. Therefore, an isolation transformer must be utilized in the power supply of a welding machine. Since the arc load behaves as a nonlinear resistor, it is also required that the static and dynamic current regulation performance of these DC/DC power supplies must be high for better welding performance [3].

Based on the output voltage/current characteristics, the arc welding machine power supplies are classified in two categories; constant current or constant voltage power supplies [4]. The operating principle of a constant current welding machine power supply is to keep the output current constant in spite of the variations in the arc length (the distance between the workpiece and the tip point of the electrode of the welding machine) which affects the stability and quality of the weld. In the constant voltage welding machines, the output voltage does not vary with the changes in the distance between the workpiece and the electrode, which is under the control of the welding machine operator. The curves showing the voltage/current characteristics for the constant current and constant voltage welding power supplies are shown in Figure 1.2, where a typical operating point is marked as P on the curves.

The welding current is adjusted by utilizing the welding process type and material properties. The welding voltage, which is the arc voltage also, depends on the arc length. In consumable electrode arc welding processes, pulsed current is applied for metal transfer to obtain better performance as shown in Figure 1.3. The peak current

(I_{pk}) causes melting and drop detachment from the electrode in the high pulse duration. The tip of the electrode and the pendant drop short circuits the output with the workpiece and the drop detaches in the low pulse duration, while in this mode the output current is reduced to the base current (I_b).

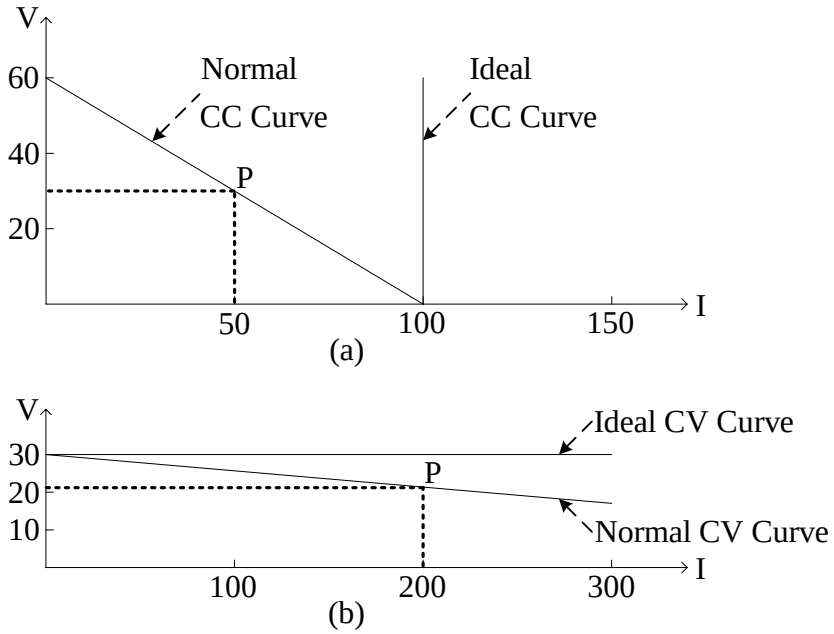


Figure 1.2 Typical voltage/current relationships for: (a) constant current welding power supplies, and (b) constant voltage welding power supplies.

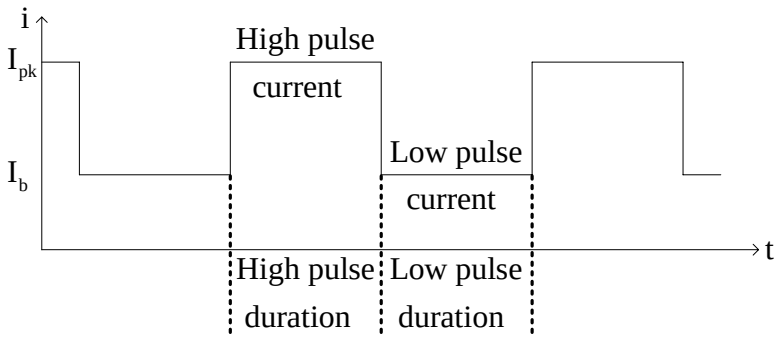


Figure 1.3 Output current waveform for the pulsed current output welding machines.

The load range of the arc welding process is very wide such that the power supply is expected to operate from open-circuit (no-load condition) to short-circuit (when the electrode sticks to the workpiece for a short span of time). Also the transients occur during the striking of the arc, rapid arc length changes and metal transfer across the arc. The power supply must respond to these changes rapidly. A precise control of the arc in all welding conditions listed above leads to an improved welding quality. When the tip of the electrode sticks to the workpiece, which is an almost unavoidable case, a short circuit occurs and is detected by the load current sensor. The uncontrolled rapid increase of the current melts the welded area and results in a ruined weld. In the old generation welding machines, a large output filter inductance is utilized to limit the rate of the output current rise to prevent the rapid load changes. However, inverter based welding machines do not include such a large filter inductance due to the rapid dynamic response capability of the inverter power supply controllers. The high switching frequency operation provides the fast dynamic response, where the control bandwidth must be around 1 kHz for an effective weld [5].

The welding machines with 50/60 Hz transformer and the diode or thyristor rectifier took place in the industry up to 80's [6]. These machines were too bulky and inefficient. Through the advances in the switching frequencies of the thyristors and BJTs, low switching frequency (3-8 kHz) inverters were utilized in the welding power supplies. With the development in the power semiconductor technology, better and lower cost power semiconductor devices have recently become available. Therefore, presently, the high frequency switch mode power supplies are becoming popular. Modern welding machines generally utilize switch mode DC/DC power supplies, which output regulated high DC current and low DC voltage. Due to high power handling capability and better utilization of the transformer and switches, among all the DC/DC converters, the most suitable topology which responds the requirements of the arc welding machine is the full-bridge DC/DC converter.

1.2 The Full-Bridge Phase-Shifted Zero Voltage Switching DC/DC Converter

The basic configuration of the full-bridge DC/DC converter, which is shown in Figure 1.4, employs a full-bridge inverter, an isolation transformer, and an output rectifier. The full-bridge inverter utilizes fully controllable semiconductor switches and outputs high frequency AC voltage waveform by utilizing the input DC voltage. Then, the inverter output voltage is isolated and scaled (if required) by the high frequency transformer. Following, the transformer output voltage is rectified by the diode bridge rectifier (half-bridge or full-bridge, depending on the application requirements) and finally filtered to provide smooth DC voltage or current. It should be kept in mind that the DC/DC converter system consists of mainly two stages, DC/AC and AC/DC stages. Thus, the name DC/DC converter here is attributed to the system, rather than the individual converter topologies.

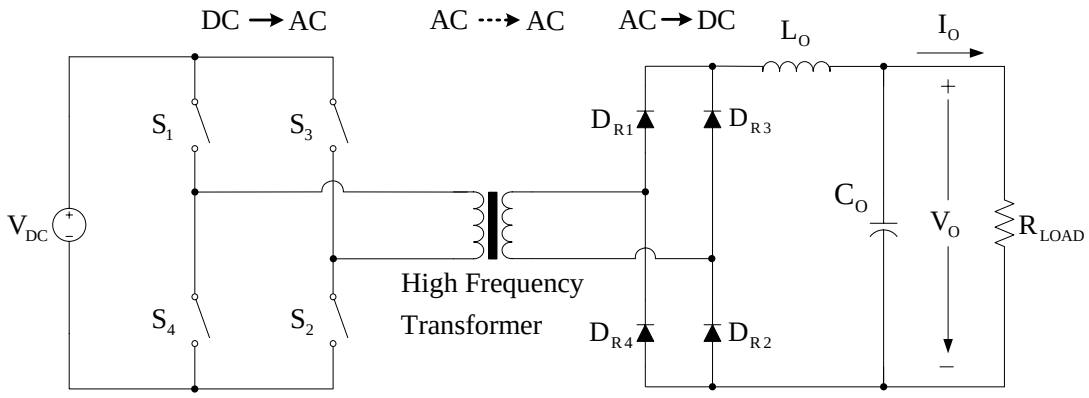


Figure 1.4 The full-bridge DC/DC converter basic circuit configuration.

With no auxiliary components in the converter circuit, the switches are considered to be under hard-switching operating condition, which corresponds to the switch voltage and current simultaneously being large during the switching intervals and implies considerable switching loss and stress on the switching devices. Generally in all hard-switching converters and most practically in high power converters the switching losses are a major limiting factor on the switching frequency. In order to maintain a high energy efficiency and acceptable cost in the converter, the switching frequency is confined to a practically acceptable range. The reduced switching

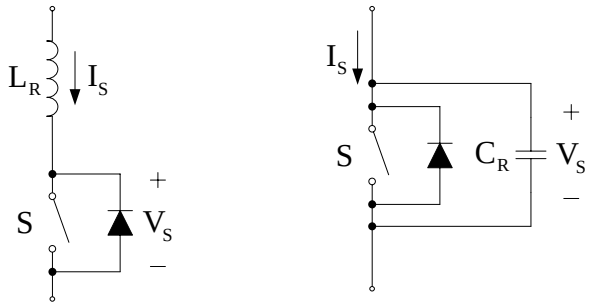
frequency results in larger passive components (transformer, inductor, capacitor) and heavier DC/DC converters, which is a considerable drawback of the industrial equipment power supply.

Soft-switching techniques, when applicable to a power converter, aid in energy efficiency enhancement, switching frequency increase (passive component size and weight reduction), switching device electrical/thermal stress reduction, EMI reduction, and cost reduction [7]. In a soft-switching circuit, the switches commutate at zero voltage or current. Thus, the switching power losses on the device are annihilated. Soft-switching is obtained by adding resonant components (inductors and capacitors) to or using the parasitic components of a power converter circuit.

Soft-switching process is provided in the DC/DC converter circuit with a resonant switch, which consists of a controllable semiconductor switch (S), a reverse parallel external diode (freewheeling diode), and a resonant inductor (L_R) or a resonant capacitor (C_R). Soft-switching of the controllable switch can be provided using either Zero Current Switching (ZCS) or Zero Voltage Switching (ZVS) technique. Figure 1.5 illustrates the resonant switches utilized for the ZCS and ZVS conditions. Whether a circuit can operate with the soft-switching principle depends on the ability of the resonant part of the circuit to reset itself. If the circuit is capable of self resetting, then soft- switching is applicable. Otherwise, soft-switching is not possible. With additional external circuit components most circuits can be made to operate with soft-switching, however for most circuits the solution is cost prohibitive. Thus, the technique is mostly applied to circuits that have self resetting capability.

For the resonant switch providing ZCS operation, a resonant inductor (L_R) is connected in series with the controllable switch, as shown in Figure 1.5.a. When the switch is in off-state, the inductor current is zero, an opportunity exists for soft turn-on. Since the inductor current is continuous and can not change instantaneously, with sufficient L_R the device fully turns-on (the voltage across the switch (V_S) is reduced to the on-state value) before the inductor current reaches a significant value. Hence, there exists only a small amount of switching power loss at turn-on process. The

turn-off process for ZCS operation is accomplished by the resonance operation between L_R and an external capacitor which is not included in Figure 1.5.a. The capacitor may be connected either in series with or parallel to the resonant switch based on the converter circuit topology. Once the resonance transition begins, the current decreases to zero. Thus, the opportunity for zero current turn-off is created. As a result of this resonance, V_S starts to increase after I_S is reduced to zero, hence ZCS is satisfied during turn-off switching interval also.



(a) (b)

Figure 1.5 The elementary resonant switches for: (a) ZCS, and (b) ZVS operation.

The resonant switch for the ZVS operation is provided by the connection of a resonant capacitor (C_R) across the switch, as shown in Figure 1.5.b. This resonant capacitor may be the internal parasitic capacitance of the semiconductor switch or an externally added capacitor if required. The turn-off of the switch is completed with low switching power loss due to C_R, which slows down the rise of V_S, hence the switch is completely turned-off (I_S is reduced to zero) before V_S reaches a significant value. The turn-on of the switch for ZVS operation is carried out by the resonance of C_R with an external inductor, which is connected to the resonant switch either in series or parallel. Due to resonance, I_S starts to increase after V_S is reduced to zero, resulting in a ZVS operation during turn-on switching interval.

The full-bridge DC/DC converter is one conventional topology that favors soft-switching with minor or no circuit topology modifications and specific operating modes. The circuit can be modified for operation under either ZCS or ZVS condition.

The semiconductor switching device parasitic output capacitance can be utilized for ZVS operation. Thus, except for specific operating conditions (such as cases where switch dead-times become a limiting factor), there is no need for external circuit components. Otherwise, additional capacitors are connected in parallel to the switches to complete the circuit for ZVS operation.

For ZVS operation of the full-bridge DC/DC converter, the operating method of the converter plays a critical role. Under phase-shifted switch pulse pattern operation (the switch logic signals of one leg are phase-shifted with respect to the other), the converter can operate with self resetting capability. Thus, this PWM method is favorable when combined with ZVS of the converter. Operating under ZVS condition permits to increase the switching frequency, which results in smaller size, lower weight, and higher bandwidth. When the full-bridge DC/DC converter is operated with the phase-shifted PWM method, the converter and its switch pulse pattern are identified with the name “Full-Bridge Phase-Shifted (FB-PS) DC/DC Converter.” Further, when this converter is operated under ZVS condition, it is so called as “FB-PS-ZVS DC/DC Converter.” In the circuit, the resonance that provides ZVS operation is between the switch output capacitance and the transformer leakage inductance. Figure 1.6 shows the DC/DC converter system with the resonant components emphasized.

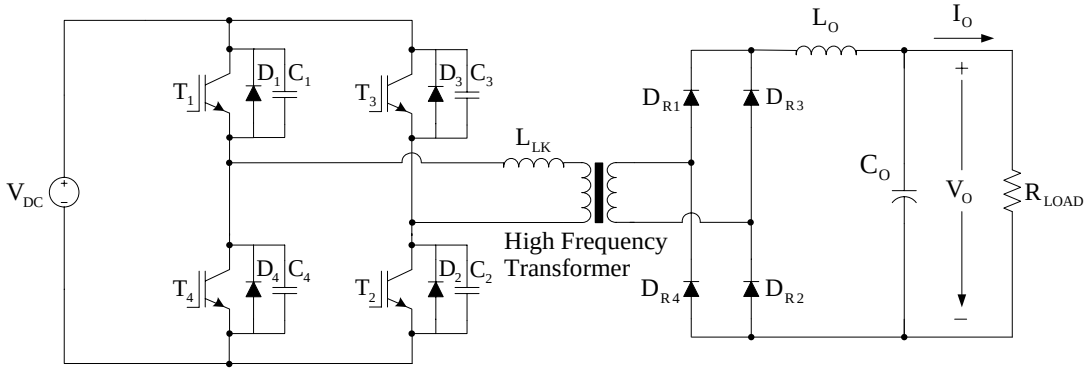


Figure 1.6 The FB-PS-ZVS DC/DC converter circuit diagram emphasizing the device parasitic capacitance or the externally added capacitors and the transformer parasitic leakage inductance.

This thesis is dedicated to the analysis, design, and implementation of a FB-PS-ZVS DC/DC converter with the main application being a welding power supply. In the following the thesis scope and outline will be provided.

1.3 Scope of The Thesis

This thesis mainly focuses on the analysis, design, and implementation of the FB-PS-ZVS DC/DC converter, which is a convenient converter circuit topology for the arc welding power supply due to the stated reasons in the previous section.

Due to the complexity of the circuit topology and operating behavior, it is usually difficult to analyze the system and provide an efficient method for analytical design of such a converter system. This thesis provides a thorough analysis of the converter operating modes and investigates the circuit behavior in detail. As a result, the influence of circuit parameters on the converter behavior becomes clearer and guideline for proper design of such a converter becomes possible. The study then continues with a methodical design approach for a 5 kW welding power supply. The analytical design approach, which is the exhaustive search method based design procedure, carries out an exhaustive search of the design parameters considering the dead-time constraint for the utilized switches (IGBTs). In the design not only the power converter, but also the high frequency transformer design is considered in detail after determining the most convenient design parameter set via a detailed performance evaluation. As a result, with concise analysis and design approach, a high performance welding power supply could be developed and manufactured. Therefore, the contribution of this thesis is towards analysis and methodical design of the FB-PS-ZVS DC/DC converter. Additionally, Digital Signal Processor (DSP) based digital control of the power supply is a contribution that follows the recent trend in control of switch mode DC/DC power supplies.

The organization of this thesis is given as follows. The second chapter gives a switch mode DC/DC converter overview classifying the popular circuit topologies in two main groups; the nonisolated and isolated DC/DC converters. Among these

topologies, the two-switch forward and full-bridge DC/DC converters are reviewed in detail, since they are widely utilized power supply topologies in the welding machines. For the full-bridge DC/DC converter, the phase-shifted PWM method is discussed in detail.

In the third chapter, the detailed analysis of the FB-PS-ZVS DC/DC converter is given with the operating modes including the equivalent circuits for each mode. The derivations regarding the ZVS range for the corresponding load current and the DC voltage conversion ratio of the converter are also included in this chapter.

The fourth chapter gives the analytical design of a 5 kW FB-PS-ZVS DC/DC converter. First, the conventional iterative design procedure is explained. However, it is not utilized in the converter design since this design procedure is not favorable for power converters employing semiconductor switches, which have a significant dead-time constraint. Therefore, an exhaustive search method based design procedure, which first establishes the search boundaries and then sweeps a range of the design parameters considering the dead-time constraint, is introduced. Then, the converter performance analysis for a range of parameters is conducted and of the parameter sets the most favorable design parameter set is selected by taking these analytical performance evaluation results into account. Then, the design of the high frequency isolation transformer is carried out by utilizing the selected design parameter set. With all the passive circuit component parameters of the converter being defined, the on paper design of the 5 kW FB-PS-ZVS DC/DC converter is finalized.

In the fifth chapter, for the given 5 kW design detailed computer simulations are carried out and the obtained results are presented to predict the performance of the FB-PS-ZVS DC/DC converter system. The computer simulation model of the FB-PS-ZVS DC/DC converter system is constructed by utilizing the device level models of the semiconductor switches to illustrate realistic switching performance (hard-switching or ZVS conditions) of the utilized semiconductor devices. The converter waveforms and efficiency are presented by utilizing these results. Also the dead-time effect on the converter efficiency is shown by utilizing the simulation results. Some

important results regarding the dead-time, circuit parameters, and energy efficiency of the converter are reported. Then, the controller stage of the closed loop current controlled FB-PS-ZVS DC/DC converter system is designed with the assistance of the obtained reduced order system model. Although the controller study is based on current control, voltage mode control can be applied instead, according to the application requirement. Finally, the steady-state and dynamic control performance of the designed system is investigated by means of computer simulations.

The sixth chapter reports the manufacturing process and the experimental results of the 5 kW FB-PS-ZVS DC/DC converter system. First, the hardware implementation of the converter prototype is explained in detail. Then, the experimental results, which show the performance of the power converter and output current controller, and the efficiency of the converter system system, are presented. The experimental results verify the analytical results of Chapter 4 and computer simulation results of Chapter 5, which shows the strong correlation between the theory, simulations, and experiments.

The final chapter summarizes the contribution of the thesis, provides the concluding remarks, and recommends future work.

CHAPTER 2

SWITCH MODE DC/DC CONVERTERS

2.1 Introduction

The switch mode DC/DC converter is the main part of an SMPS. There are various types of DC/DC converter circuit topologies utilized in the SMPSs based on the system requirements such as output to input voltage relationship, power rating, and the need for galvanic isolation.

This chapter reviews the popular DC/DC converter circuit topologies and their basic operation principles. The DC/DC converters are investigated in two groups based on the need of galvanic isolation. Of the reviewed converters, being the focus of the thesis, the full-bridge DC/DC converter, is discussed in detail. For the full-bridge DC/DC converter, the phase-shifted PWM method is discussed after the conventional PWM method for the DC/DC converters is given. Thus, this chapter builds the basic background for the FB-PS-ZVS DC/DC converter study of the thesis.

2.2 Switch Mode DC/DC Converter Overview

Switch mode DC/DC converters can be investigated in two classes based on the demand for isolation [1]. If electrical (galvanic) isolation is required due to the safety reasons, a transformer is utilized in the DC/DC converter. The most popular DC/DC converter topologies belonging to both nonisolated and isolated converter classes are listed in Figure 2.1. Topologically, the step-down and step-up converters are the basic topologies and the rest can be derived from these two converters.

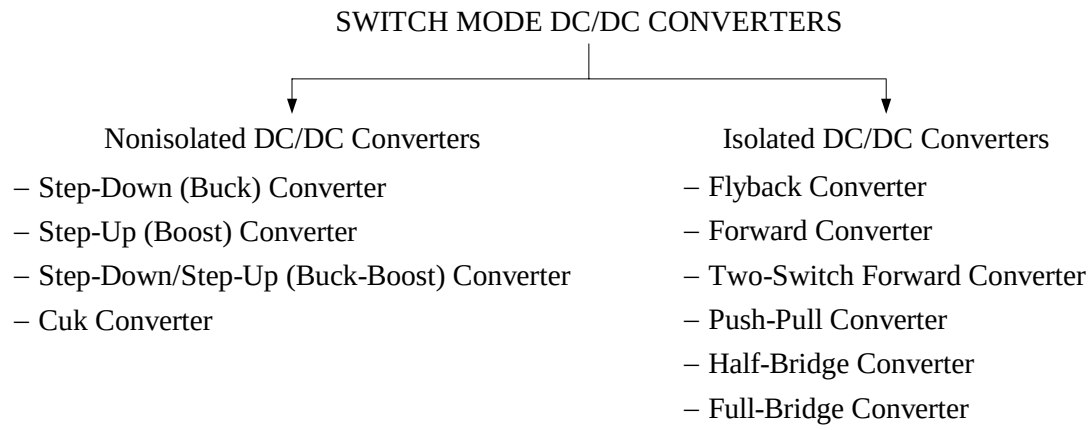


Figure 2.1 Topological classification of the popular switch mode DC/DC converters.

In this section, the listed DC/DC converter circuit topologies in Figure 2.1 are reviewed by utilizing their basic circuit configuration. The circuit topologies discussed are in their basic form and modified forms are not discussed in this review. Thus the switching (commutation) behavior of the switches is not altered from the form inherent to the circuit. Therefore, the switches are generally considered to be under hard-switching operating condition, which corresponds to the voltage and current simultaneously being large during switching and implies considerable switching loss and stress on the device. Hence, there will be high switching losses and stress during the turn-on and turn-off process that limits the switching frequency of the controllable switch.

2.2.1 Nonisolated DC/DC Converters

The nonisolated DC/DC converters, which include the basic DC/DC converter topologies, usually utilize a single controllable semiconductor switching device and a diode. These topologies are mostly employed up to the power rating of a few hundred watts and where electrical isolation is not needed. The overview on the nonisolated DC/DC converter types which are classified in Figure 2.1 is given in the following.

First, the operating principles of the step-down (buck) DC/DC converter, which is shown in Figure 2.2, are overviewed. As the converter name implies, the regulated output voltage (V_O) is lower than the input voltage (V_{DC}). While the controlled semiconductor switch (S) is conducting, power is transferred from source to load and at the same time the filter inductor (L) is charged. When the switch is turned-off, the diode (D) becomes forward-biased and forms a conduction path for the filter inductor current. Manipulating the switch periodically, the output voltage can be regulated. The relationship between the input voltage and the output voltage (DC voltage conversion ratio) can be obtained from the filter inductor volt-second balance rule, which states that along a switching period of a steady-state operation the filter inductor average voltage is zero. Considering the switch is on for the duration of $d \cdot T_S$, where d is the duty cycle of the switch and T_S is the switching period, the voltage across the filter inductor in this time interval is the difference between the input voltage and the output voltage. When the switch is off for the time interval of $(1\text{-}d) \cdot T_S$, the voltage across the filter inductor is the reverse of the output voltage. The DC voltage conversion ratio is obtained by equating the sum of the products of the formed voltage levels across the filter inductor with the corresponding time intervals to zero in a switching period. The resulting equality originating from the filter inductor volt-second balance rule is given in (2.1). Then, by utilizing (2.1) the DC voltage conversion ratio for the step-down DC/DC converter is obtained as in (2.2). Since the duty cycle of the switch can not be greater than one, the output voltage is always lower than the input voltage.

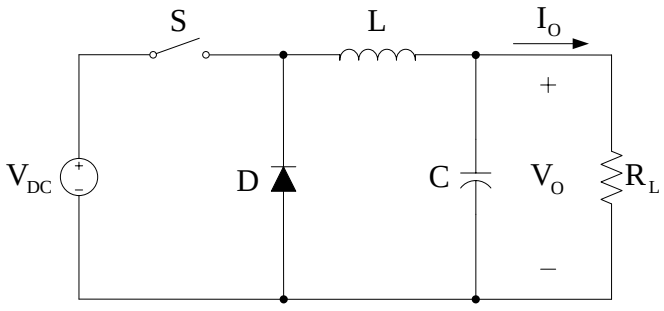


Figure 2.2 The step-down DC/DC converter circuit diagram.

$$\left(V_{DC} - V_O\right) \cdot d \cdot T_S = V_O \cdot \left(1 - d\right) \cdot T_S \tag{2.1}$$

$$\frac{V_O}{V_{DC}} = d \tag{2.2}$$

The step-up DC/DC converter, shown in Figure 2.3, is also known as “the boost converter” due to its voltage boosting function. While the switch (S) is conducting, the inductor (L) is charged and the regulation of the load is provided by the stored filter capacitor (C) energy. When the switch is turned-off, the diode (D) becomes forward-biased and power is transferred from source to load including the stored energy in the inductor. The filter capacitor also stores energy in this time interval. The output voltage is always greater than the input voltage as can be observed from the DC voltage conversion ratio given in (2.3). This equation is also derived using the inductor volt-second balance rule. In practice, however, as the duty cycle approaches 100% the DC voltage conversion ratio can not increase to very large values due to the effects of the parasitic components (specifically, the losses of the equivalent series resistance of the filter inductor) of the circuit elements.

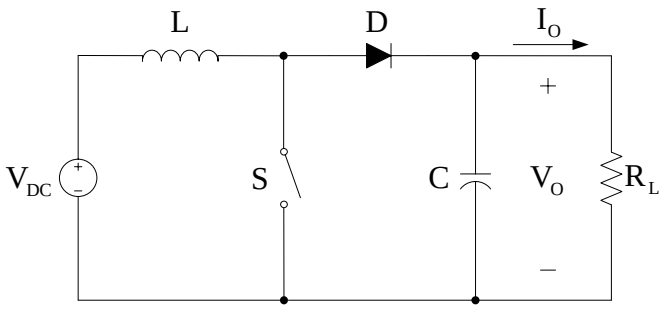


Figure 2.3 The step-up DC/DC converter circuit diagram.

$$\frac{V_O}{V_{DC}} = \frac{1}{1 - d} \tag{2.3}$$

The step-down/step-up (buck-boost) DC/DC converter, shown in Figure 2.4, regulates the output voltage either as a step-down or a step-up converter based on the

applied duty cycle to the switch (S). While the switch is conducting, the inductor (L) is charged and the stored energy in the filter capacitor (C) is utilized to regulate the output. When the switch is turned-off, the diode (D) becomes forward-biased and conducts the inductor current. Due to the inductor current direction, polarity of the diode and output voltage is reversed with respect to the input voltage polarity. As can be concluded from the DC conversion ratio for the buck-boost converter given in (2.4), this converter is utilized as either a step-down or a step-up converter for the duty cycle values smaller or greater than 0.5, respectively.

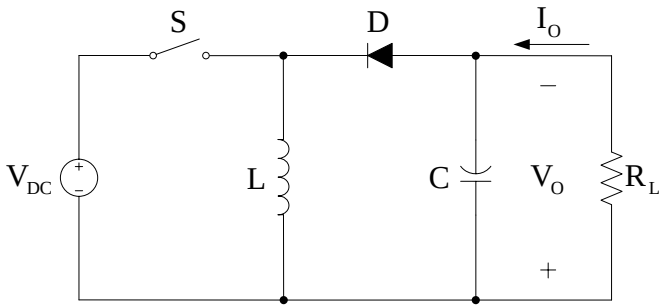


Figure 2.4 The buck-boost DC/DC converter circuit diagram.

$$\frac{V_O}{V_{DC}} = \frac{d}{1-d} \tag{2.4}$$

Shown in Figure 2.5, the Cúk converter is derived by applying the duality principle to the buck-boost converter topology. The final converter topology is obtained after adding the filter inductor (L_2) and the filter capacitor (C) components at the output. While the switch (S) is conducting, the input inductor (L_1) is charged by the input voltage source and the filter inductor (L_2) is charged by the stored energy in the capacitor (C_1), which reverse biases the diode (D). In this interval, both inductor currents flow through the switch. When the switch is turned off, C_1 is charged by the input voltage source and the stored energy in the input inductor. The output current (I_O) is supplied to the load by the stored energy in L_2. In this interval, both inductor currents flow through the diode. As in the buck-boost converter, the output voltage has reverse polarity with respect to the input voltage. Applying the inductor volt-

second balance rule to the input and the filter inductors, the DC conversion ratio of the converter is found the same as that of the buck-boost converter given in (2.4), which states that the converter can be utilized either as a step-down or a step-up converter.

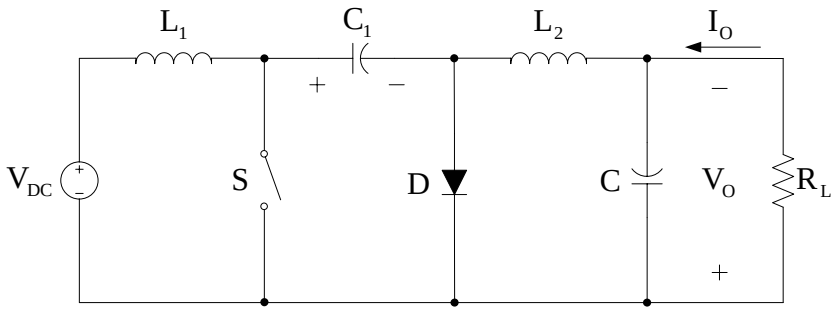


Figure 2.5 The Cúk converter circuit diagram.

2.2.2 Isolated DC/DC Converters

Isolated DC/DC converters utilize a high frequency transformer to provide electrical isolation between the load and the input line due to safety reasons mainly. The isolated DC/DC converter topologies listed in Figure 2.1 are derived from the basic nonisolated DC/DC converter topologies. These converters have a wide power range of application from a few watts to hundreds of kilowatts. In the following, an overview of the most popular isolated DC/DC converters is given.

The flyback DC/DC converter, shown in Figure 2.6, is derived from the buck-boost converter. The inductor in the buck-boost converter is substituted with the flyback transformer which behaves like an inductor practically. By winding the secondary of the transformer in reverse polarity with respect to the primary, the polarity of the diode and capacitor is reversed with respect to the buck-boost converter. While the switch (S) is conducting, the magnetizing inductance of the transformer is charged by the DC voltage source (V_{DC}) and the transformer secondary voltage reverse biases the diode (D) resulting in no power transfer from input to the output. When the

switch is turned off, the stored energy in the magnetizing inductance supplies the load current through the diode. The DC conversion ratio for the flyback converter, which is given in (2.5), is derived by utilizing the inductor volt-second balance rule which is applied to the magnetizing inductance of the transformer. Since the applied voltage to the primary winding is always at the same polarity, the flux induced in the flyback transformer core is in one direction only, which means the core is utilized only in the first quadrant of the B-H curve. Due to the poor magnetic core utilization, the flyback DC/DC converters can be utilized up to a few hundred watts only.

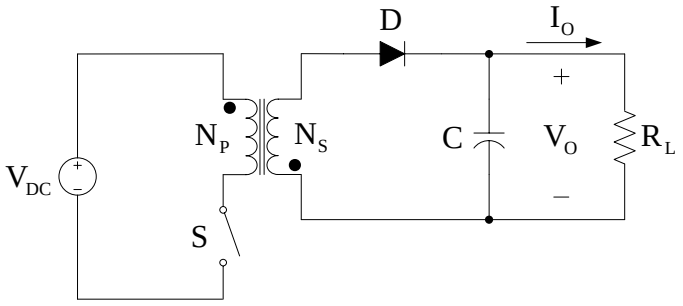


Figure 2.6 The flyback DC/DC converter circuit configuration.

$$\frac{V_O}{V_{DC}} = \frac{N_S}{N_P} \cdot \frac{d}{1-d} \tag{2.5}$$

The forward DC/DC converter, shown in Figure 2.7, is based on the step-down converter. The power transfer from the input voltage source to the load occurs while the switch (S) is conducting. In this operation mode D_1 conducts the current which charges the inductor (L) and also supplies the output current (I_O). When the switch is turned off, D_2 freewheels the inductor current. The voltage applied to the primary winding is always at the same polarity, so the flux induced in the isolation transformer core must be canceled to prevent the saturation of the transformer core. The flux cancellation is provided by the demagnetization branch which consists of N_D turns of extra winding around the transformer core and a diode (D_3) having reverse polarity to reset the magnetizing current. Based on the specified N_P and N_D, there exists a maximum switch duty cycle to reset the transformer core. Using the

inductor volt-second balance rule, the DC conversion ratio for the forward DC/DC converter can be obtained as given in (2.6).

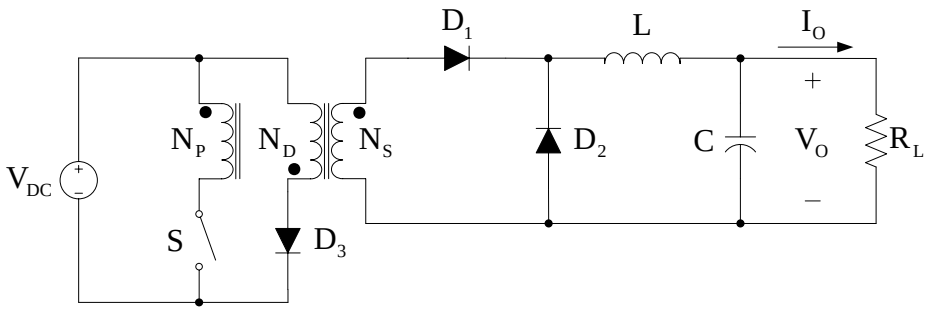


Figure 2.7 The forward DC/DC converter circuit configuration.

$$\frac{V_O}{V_{DC}} = \frac{N_S}{N_P} \cdot d \tag{2.6}$$

The basic operation of the two-switch forward DC/DC converter is the same as in the single-switched version, where the demagnetization of the transformer is provided by utilizing the diagonal diodes (D_1 and D_2) instead of an extra transformer winding. As shown in Figure 2.8, only one primary winding and only one secondary winding is required for this topology. The switches (T_1 and T_2) having a voltage rating of V_{DC}, which is much less than of that in the single-switch topology, are manipulated simultaneously. No demagnetization winding is required as the diodes provide commutation path for the transformer primary current. However, the two-switch forward DC/DC converter topology is only suitable for the low power applications due to the poor utilization of the tansformer (single quadrant operation of the magnetic circuit). The DC conversion ratio of the two-switch forward DC/DC converter is found the same as that of the single-switched version given in (2.6), where d is the duty cycle of each switch that can not exceed 0.5 due to the demagnetization of the transformer.

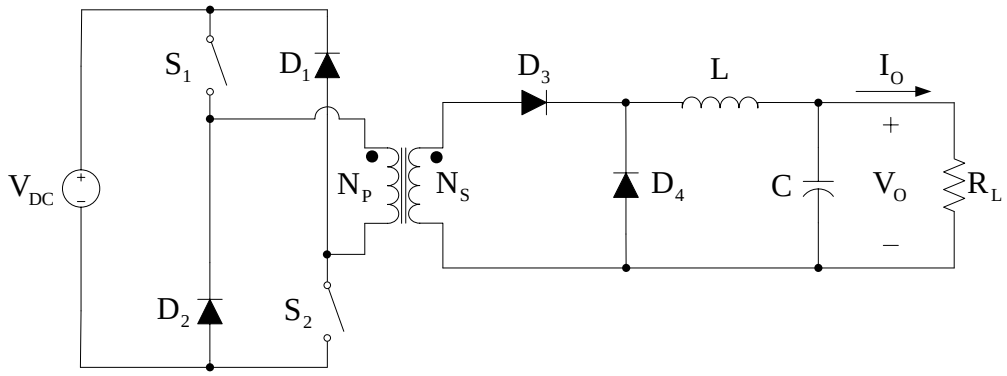


Figure 2.8 The two-switch forward DC/DC converter circuit configuration.

In all the single-switch DC/DC converters and the two-switch forward converter studied so far, DC/DC conversion is achieved by processing input DC voltage including the stages of chopping and filtering to obtain a smooth DC output voltage at desired level. Unlike in the single-switch DC/DC converters and the two-switch forward converter, DC/DC conversion for the push-pull, half-bridge and full-bridge DC/DC converters is provided by utilizing three conversion stages which are the DC/AC, AC/AC (for isolation and scaling), and AC/DC conversion. These stages are realized with the high frequency inverter, the high frequency isolation transformer, and the rectifier, respectively. The high frequency inverter, which includes controllable switching devices, outputs rectangular high frequency AC voltage waveform utilizing the DC input voltage as a result of appropriate PWM signals applied to the switches. The inverter applies the high frequency AC voltage to the primary winding of the transformer, where the isolation and also the scaling of the voltage and current is provided. The magnetic flux induced in the transformer core by the inverter output AC voltage is bidirectional. Thus, the core is operated in the first (positive) and third (negative) quadrant of the B-H curve, which results in a better utilization of the transformer core. The isolated and scaled AC voltage at the transformer secondary winding is converted to DC voltage again either with a half-bridge (center-tap) or a full-bridge diode rectifier. The half-bridge diode rectifier utilizes two diodes, which results in reduced voltage drop and conduction power loss in the rectifier with respect to the full-bridge diode rectifier, where four diodes are utilized in. Thus, the half-bridge rectifier topology is advantageous for the

applications that require very high current and low voltage at the output. However, a high frequency transformer comprising two secondary windings with same features is required for the half-bridge rectifier while the full-bridge rectifier does not need an extra secondary winding. For the sake of simplicity, the rectifiers shown in the circuit diagrams of the push-pull, half-bridge and full-bridge DC/DC converters are illustrated as a half-bridge rectifier. Depending on the application requirement, the rectifier may be replaced by a full-bridge rectifier as in Figure 1.4.

The push-pull DC/DC converter, shown in Figure 2.9, is also based on the step-down converter. During the power transfer, either S_1 and D_1 or S_2 and D_2 are conducting simultaneously to supply the load current while charging the inductor (L). While S_1 and S_2 are off, the output current (I_O), which is shared equally by the diodes D_1 and D_2, is supplied from the stored energy at the inductor. The DC conversion ratio of the push-pull DC/DC converter is given in (2.7), where d is the duty cycle of each switch which can not exceed 0.5.

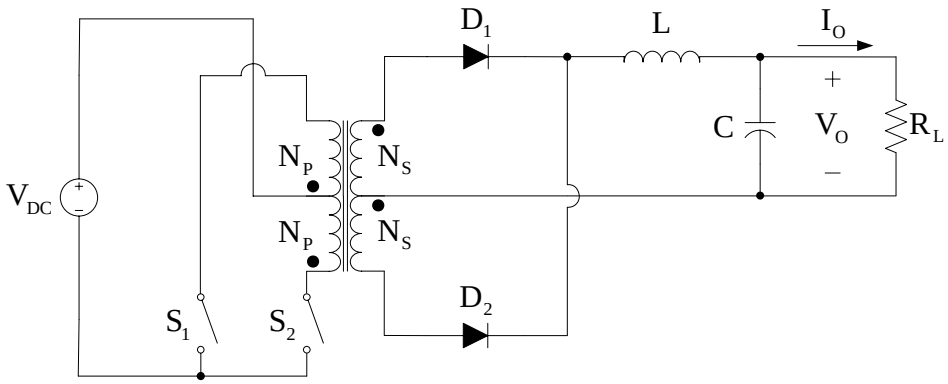


Figure 2.9 The push-pull DC/DC converter circuit configuration.

$$\frac{V_O}{V_{DC}} = 2 \cdot \frac{N_S}{N_P} \cdot d \qquad (2.7)$$

The half-bridge DC/DC converter, shown in Figure 2.10, also originates from the step-down converter and is operated in the same manner as the push-pull converter. Equal valued capacitors C_1 and C_2 are inserted across the input DC voltage source in

series, forming a half V_{DC} point (a center point) to the primary winding terminal of the high frequency transformer. Hence, the DC voltage levels of $-V_{DC}/2$ or $V_{DC}/2$ is applied to the transformer primary while the switch S_1 or S_2 is conducting with the same duty cycle. The circuit behavior at the secondary side of the transformer is the same as in the push-pull converter. The DC conversion ratio of the half-bridge converter is given in (2.8), where d can have a maximum value of 0.5.

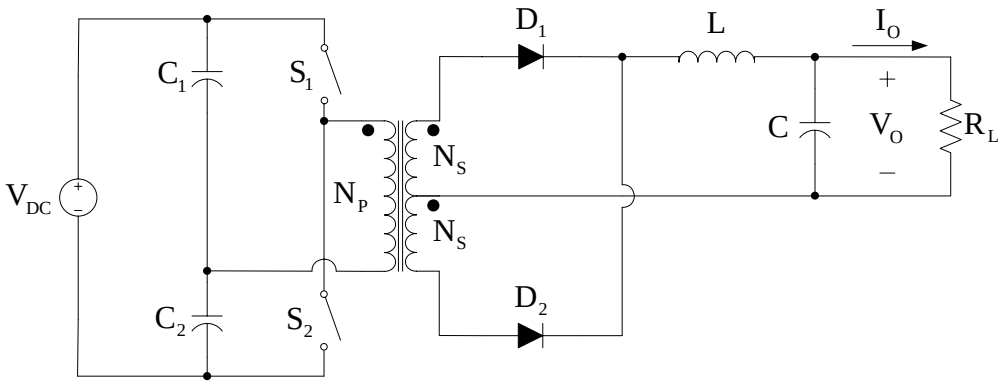


Figure 2.10 The half-bridge DC/DC converter circuit configuration.

$$\frac{V_O}{V_{DC}} = \frac{N_S}{N_P} \cdot d \tag{2.8}$$

The full-bridge DC/DC converter, shown in Figure 2.11, is derived from the step-down converter and is obtained simply by replacing the capacitors C_1 and C_2 in the half-bridge DC/DC converter with the controllable switching devices. The basic operating scheme of this converter is providing the conduction of the switch pairs (S_1 and S_2, S_3 and S_4) alternately with the same duty cycle, which results in the voltage levels of $-V_{DC}$ or V_{DC} applied to the transformer primary winding. The circuit operations carried out at the output stage are the same as in the push-pull DC/DC converter. The DC voltage conversion ratio of the full-bridge DC/DC converter is obtained from the filter inductor (L) volt-second balance rule. When one of the switch pairs (S_1 and S_2 or S_3 and S_4) is on for the duration of $d \cdot T_S$, the voltage across the filter inductor is the difference between the referred input voltage to the secondary side and the output voltage. When all of the switches are off for the time

interval of $(1\text{-}d)\cdot T_S$, the voltage across the filter inductor is the reverse of the output voltage. This operation is completed in a half switching period interval. In the other interval the switches of the other switch pair are on for the duration of $d\cdot T_S$ again. Thus, the total duration of the power transfer is $2\cdot d\cdot T_S$. The resulting equality derived from the filter inductor volt-second balance rule is given in (2.9), where d can be 0.5 at most. By utilizing (2.10), the DC voltage conversion ratio for the full-bridge DC/DC converter is obtained as in (2.10). Although the circuit topologies of the full-bridge DC/DC converter and the push-pull DC/DC converter differ from each other, their DC conversion ratio is the same. While the push-pull DC/DC converter is typically rated at less than a kilowatt, the full-bridge DC/DC converter has a wide power range, up to hundreds of kilowatts.

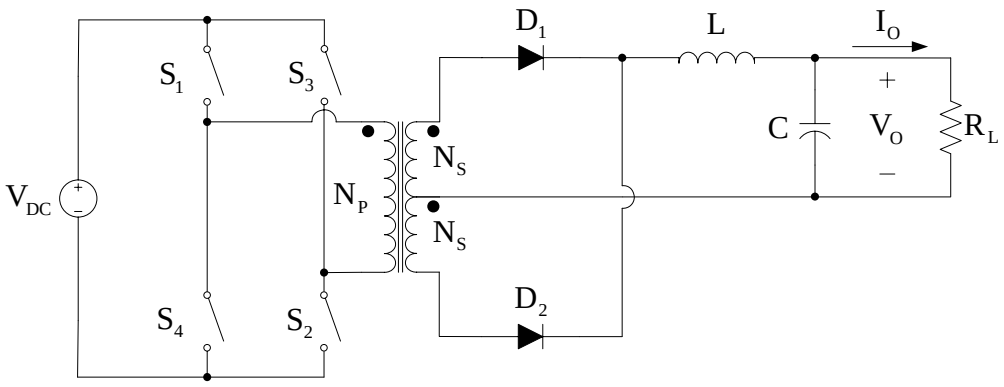


Figure 2.11 The full-bridge DC/DC converter circuit configuration.

$$\left(\frac{N_S}{N_P}V_{DC}-V_O\right)\cdot 2\cdot d\cdot T_S = V_O\cdot(1-2\cdot d)\cdot T_S \tag{2.9}$$

$$\frac{V_O}{V_{DC}} = 2\cdot\frac{N_S}{N_P}\cdot d \tag{2.10}$$

2.3 Selection of The Suitable DC/DC Converter Topologies for The Welding Power Supply Application

With the advances in the power semiconductor devices, high frequency switch mode DC/DC converters are widely utilized in the welding machine power supplies [6]. In the low power range, where the emphasis is on cost reduction but not on energy efficiency maximization and size minimization, the two-switch forward DC/DC converter suffices. Thus, in welding applications with power ratings less than several kilowatts, this converter topology is favored. For higher power rating applications the full-bridge DC/DC converter is generally employed in a welding machine due to its superior energy efficiency, and magnetic circuit utilization properties.

The utilization of the full-bridge DC/DC converter in the welding power supply application involves operation at high frequency switching (typically above several tens of a kilohertz) for lower size and cost as well as higher bandwidth. With the use of the basic topology, depending on the operating point the switching behavior of the circuit may involve hard-switching or soft-switching. Thus, the loss characteristics and the energy efficiency characteristics vary and may be insufficient for applications requiring high energy efficiency. Based on the output voltage and current ratings the high-frequency rectifier utilized at the output of the transformer may be of full-bridge or half-bridge (center-tap) type. Shown in Figure 2.12, for high current (low voltage) applications typically the half-bridge rectifier topology is favored due to the higher energy efficiency property of this topology. In applications involving an output voltage in the range of hunderd volts and above, the full-bridge rectifier topology is utilized. In this thesis, the full-bridge inverter and full-bridge high-frequency rectifier based DC/DC converter will be considered and from here on the topology in Figure 1.6 will be implied as the welding power supply converter. Furthermore, with focus being on high performance, the soft-switching operation, which requires circuit modifications, will be emphasized. Thus, in the following chapter the topological modifications will be studied in detail.

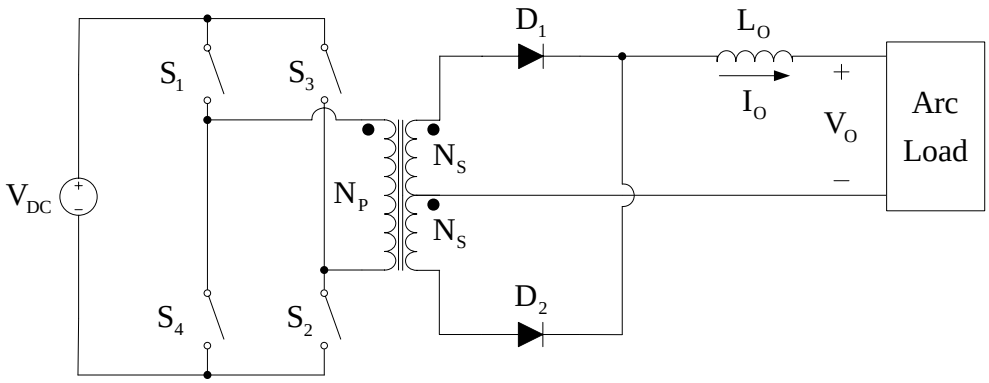


Figure 2.12 The full-bridge DC/DC converter topology with half-bridge high-frequency rectifier, utilized in welding power supplies.

2.4 PWM Methods for The Switch Mode DC/DC Converters

The switch gate PWM signals of the switch mode DC/DC converters are generated by utilizing the reference voltage, which is calculated in the power supply control block using the measured and scaled feedback signals. In the analog implementation, the reference voltage is compared with a suitable sawtooth (or triangular) carrier voltage waveform to obtain the PWM signal for the controllable switch gate. In the conventional PWM method the sawtooth carrier waveform is fixed and the reference voltage magnitude is varied to regulate the output. However, in the phase-shifted PWM method the phase difference between the sawtooth carrier waveforms of the inverter legs is varied while the reference voltage is kept constant.

2.4.1 Conventional PWM Methods

The switch gate PWM signals of the single-switch DC/DC converters (for the step-down, step-up, buck-boost, Cúk, flyback, and forward converter) are generated by comparing the calculated reference voltage in the control block, with a sawtooth carrier voltage waveform at the selected switching frequency. In the single loop voltage control mode, the reference voltage is obtained by the compensation of the error voltage, which is the difference between the measured output voltage of the

DC/DC converter and the desired reference output voltage. As illustrated in Figure 2.13, the switch is on in the intervals, where the reference voltage is higher than the sawtooth voltage, and the switch is off otherwise.

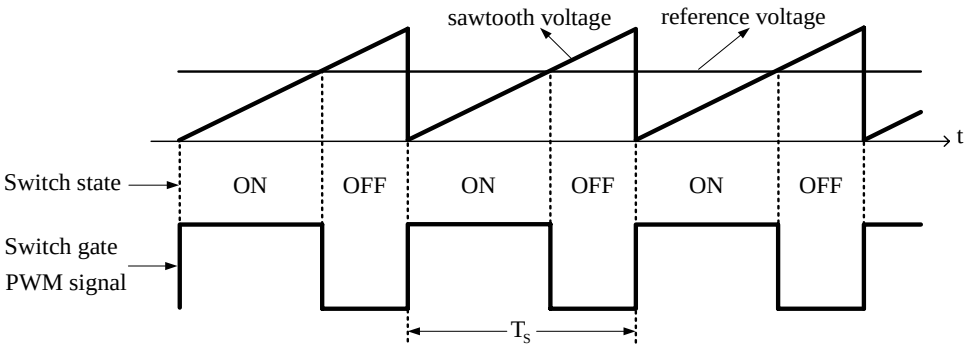


Figure 2.13 Conventional PWM signal generation scheme for the single-switch DC/DC converters.

For the push-pull, half-bridge and full-bridge DC/DC converters, a reference voltage that specifies the duty cycle of each switch is compared with a sawtooth carrier voltage waveform at twice the switching frequency. The alternating switch or switch pair is on during the interval that the reference voltage is higher than the sawtooth voltage and for the reverse case all of the switches are off. The sawtooth and reference voltage waveforms are shown and the resulting conducting switches in the corresponding time intervals are stated for these DC/DC converters in Figure 2.14. Also the applied transformer primary voltage waveform is shown in the same figure. As illustrated in Figure 2.14, the voltage levels at the transformer primary are $-V_{DC}/2$ and $V_{DC}/2$ for the half-bridge DC/DC converter, and $-V_{DC}$, 0, and V_{DC} for the push-pull and full-bridge DC/DC converters.

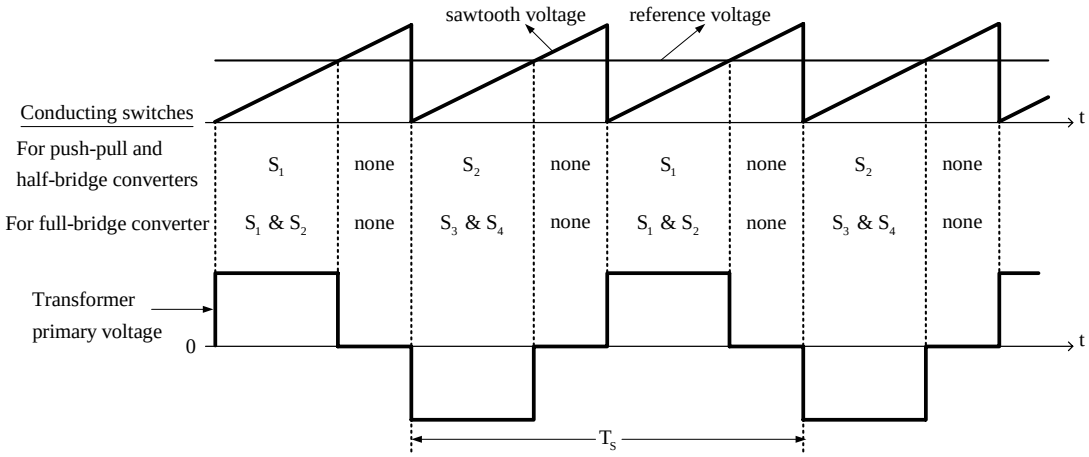


Figure 2.14 Conventional PWM signal generation scheme for the push-pull, half-bridge, and full-bridge DC/DC converters.

2.4.2 Phase-Shifted PWM Method

The switch gate PWM signals of the full-bridge DC/DC converter can also be generated by utilizing the phase-shifted PWM method. While the generated switch PWM signals are the same, the generation method of these signals is different from the conventional PWM method. In this PWM method while keeping the sawtooth carrier voltage waveform of one inverter leg constant, the output is regulated by phase shifting the carrier sawtooth voltage waveform of other leg as illustrated in Figure 2.15. To implement this method two sawtooth voltage waveforms, each for two switches of one inverter leg, are compared with the reference voltage (V_R) which has a constant magnitude of half of the peak value of the sawtooth voltage waveform. Hence, all of the switches have the same duty cycle of 50%, ideally. The compensated error voltage is converted to the phase angle (ϕ) between the two carrier sawtooth voltage waveforms. Hence, in this PWM method, instead of the reference voltage, the phase angle is utilized as the control variable.

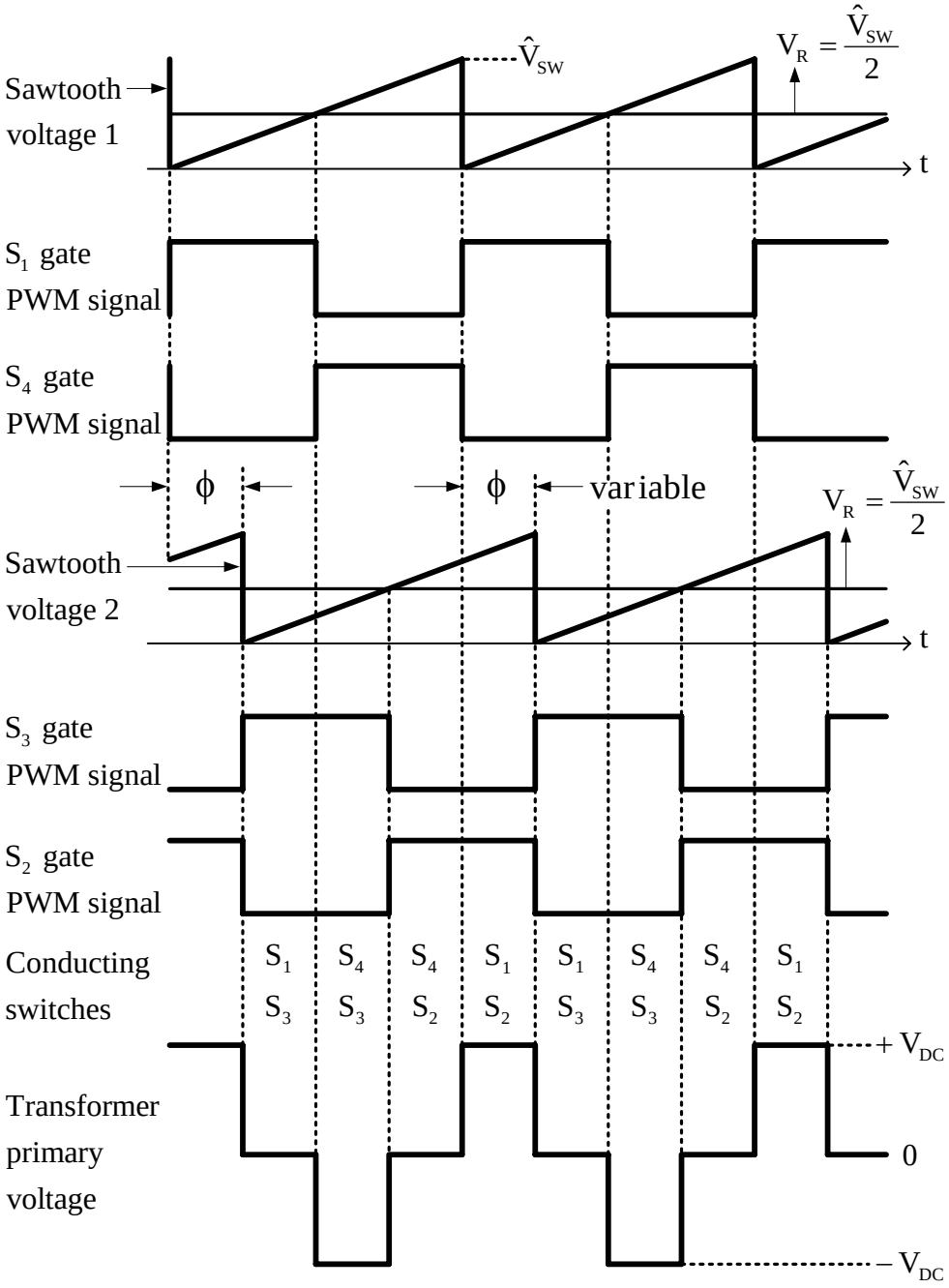


Figure 2.15 Phase-shifted PWM signal generation scheme for the full-bridge DC/DC converter.

2.5 Soft-Switching Operation of The FB-PS DC/DC Converter

With some circuit modifications, the full-bridge DC/DC converter with the phase-shifted PWM pattern, can be soft-switched such that it satisfies either a ZVS or ZCS condition as discussed in Chapter 1. Thus, the phase-shifted PWM method provides advantageous attributes to the full-bridge DC/DC converter.

When the phase-shifted full-bridge DC/DC converter operates at zero voltage switching condition, the converter is called the Full-Bridge Phase-Shifted Zero Voltage Switching (FB-PS-ZVS) DC/DC converter. Operating in ZVS mode, this converter is a member of the resonant-transition type of resonant converters [1]. In ZVS type of the resonant-transition topologies, the resonance operation occurs only at the switching transitions and the switches turn on at zero voltage. Due to the slow rise of the switch voltage, the turn-off is achieved with low switching power loss. Also the peak voltage of the switch clamps to the input DC voltage at the end of the resonance operation.

In the FB-PS-ZVS DC/DC converter, soft-switching is provided by the phase-shifted PWM method which satisfies the ZVS operation with the assistance of the resonance action between the switch output capacitance and the transformer leakage inductance. The steps describing the converter circuit operation are complex and require a detailed analysis. Therefore, the analysis of the FB-PS-ZVS DC/DC converter is given in the following chapter in detail.

CHAPTER 3

ANALYSIS OF THE FULL-BRIDGE PHASE-SHIFTED ZERO VOLTAGE SWITCHING DC/DC CONVERTER

3.1 Introduction

The detailed analysis of the FB-PS-ZVS DC/DC converter system is involved due to the large number of circuit modes and the complexity of the converter operating behavior. Establishing an accurate path for the analytical design of such a converter system requires in depth understanding and a methodical analysis of the converter system. This chapter provides a thorough analysis of the converter operating modes and investigates the circuit behavior in detail. The FB-PS-ZVS DC/DC converter is given with the operating modes including the equivalent circuits for each mode. The derivations regarding the ZVS range for the corresponding load current and the DC voltage conversion ratio of the converter are also included in this chapter.

3.2 The FB-PS-ZVS DC/DC Converter Circuit Topology

The FB-PS-ZVS DC/DC converter which forms the power supply unit of the arc welding machine is shown in Figure 3.1 [8], [9]. This converter utilizes a full-bridge inverter, a high frequency transformer, a full-bridge diode rectifier (which may be replaced with a center-tap diode rectifier for high current applications), and a low-pass filter (consisting of the passive components L_O and C_O) at the output. The gate PWM signals for the switches in the full-bridge inverter are generated by utilizing the phase-shifted PWM method, which facilitates ZVS operation for the switches.

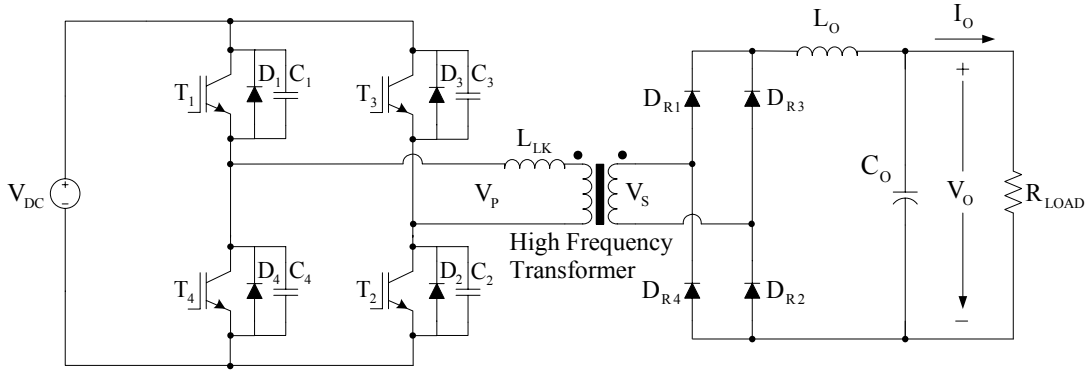


Figure 3.1 The FB-PS-ZVS DC/DC converter circuit diagram.

The full-bridge inverter section of the FB-PS-ZVS DC/DC converter is fed from the DC bus, which is represented by a constant voltage source (V_{DC}) in Figure 3.1. The single phase full-bridge inverter consists of four gate controlled semiconductor switches (T_1, T_2, T_3, and T_4) such as IGBTs (as illustrated in Figure 3.1) with their freewheeling diodes (D_1, D_2, D_3, and D_4). All switches in the full-bridge inverter operate with a duty cycle of 50%, ideally. In the phase-shifted PWM method, the gate PWM signals of T_2 and T_3 are delayed (phase-shifted) with respect to those of the switches T_1 and T_4. The full-bridge inverter applies three different voltage levels to the transformer primary winding such as $+V_{DC}$ (while T_1 and T_2 are conducting simultaneously), $-V_{DC}$ (while T_3 and T_4 are conducting simultaneously), and 0 (while T_1 and T_3 or T_2 and T_4 are conducting simultaneously). High frequency AC voltage at the transformer secondary winding is rectified and then filtered by a low-pass filter (L_O and C_O) to obtain a smooth DC voltage at the output of the DC/DC converter.

The capacitors (C_1, C_2, C_3, and C_4), which are connected across the switches in Figure 3.1, emphasize the parasitic output capacitances of the switches. If required, additional external capacitors can be inserted across the switches while keeping the same values for the total capacitance across the switches in the same inverter leg ($C_1 = C_4$ and $C_2 = C_3$). The inductor (L_{LK}), which is connected in series with transformer primary winding, emphasizes the parasitic leakage inductance of the high frequency transformer. If required, an additional inductor can be connected in series with the transformer primary winding. The two parasitic components (the switch output

capacitance and transformer leakage inductance), which normally decrease the performance of the DC/DC converters under hard-switching condition, are utilized advantageously in the phase-shifted PWM method to achieve ZVS. These parasitic components of the circuit elements are used as the main circuit elements to provide resonant transitions during the switching time intervals. The switches turn on under ZVS condition as a result of these resonant transitions. Due to the elimination of the switching losses, the FB-PS-ZVS DC/DC converter is a convenient converter topology for high frequency and high power applications.

3.3 Switch Gate PWM Signals Utilized in The FB-PS-ZVS DC/DC Converter

The gate PWM signals required for the switches of the FB-PS-ZVS DC/DC converter operated with phase-shifted PWM method and the resulting transformer primary voltage are shown in Figure 3.2. In this figure S_{T1}, S_{T2}, S_{T3}, and S_{T4} represent the gate PWM signals of the switches and d_{T1}, d_{T2}, d_{T3}, and d_{T4} represent the switch duty cycles. The gate PWM signals of T_1 and T_4 lead the gate PWM signals of T_2 and T_3 by an angle of φ. T_2 (or T_3) is turned on after the turn on of T_1 (or T_4) with a time delay of $(\varphi / 360^{O}) \cdot T_S$, where T_S is the switching period. The inverter leg including the switches T_1 and T_4 is called the "leading leg" and the other inverter leg with the switches T_2 and T_3 is called the "lagging leg." In the phase-shifted PWM method, all switches are operated with a duty cycle of 50%, ideally.

In practice, due to the finite turn-on and turn-off times of the switches, a short time blanking interval between the gate PWM signals of the switches of the same inverter leg (T_1 and T_4 or T_2 and T_3) is introduced. During this short time blanking interval (t_d), also called the dead-time, formerly conducting switch completes its turn-off process and after the dead-time ends, the complementary switch in the same inverter leg is turned on safely. Both switches in the same inverter leg are off during the dead-time resulting in a switch duty cycle lower than 50%. On the other hand, if the dead-time is not introduced, short-circuit of DC bus may take place due to the conduction of both switches in the same inverter leg. The so called shoot-through fault condition may damage the converter completely.

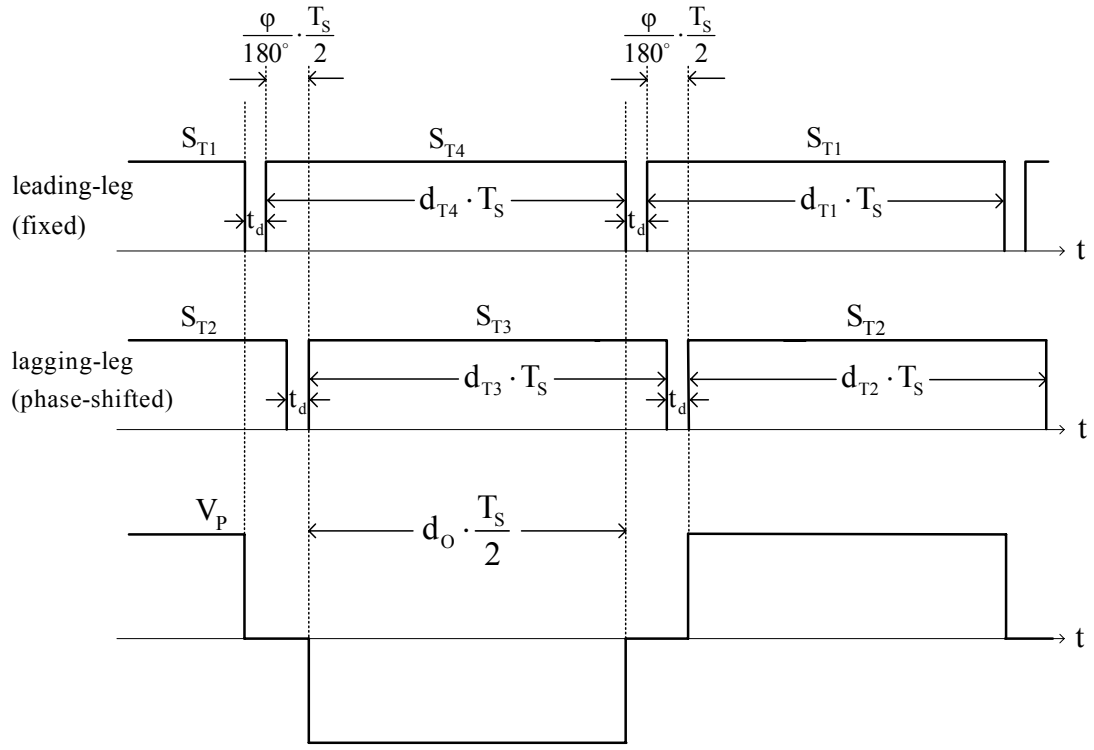


Figure 3.2 Switch gate PWM signals and the resulting transformer primary voltage.

Application of the above described switch gate PWM signals to the switches results in the transformer primary voltage waveform (V_P) shown in Figure 3.2. It can be observed from the figure that when the diagonal switches in the full-bridge inverter are conducting together, $+V_{DC}$ or $-V_{DC}$ is applied to the transformer primary winding. The ratio of the total duration of the voltage ($+V_{DC}$ and $-V_{DC}$) applied to the transformer primary winding in a switching period, to the switching period is symbolized as d_O and stated on the transformer primary voltage waveform.

The desired inverter output voltage is obtained by introducing adequate phase-shift angle (φ). The relationship between d_O and φ including the effect of the dead-time can be deduced from Figure 3.2 and is given in (3.1).

$$d_O = 1 - \frac{\varphi}{180^o} - \frac{2 \cdot t_d}{T_S} \tag{3.1}$$

According to the expression in (3.1), the output voltage of the DC/DC converter can be increased by decreasing the phase shift angle or vice versa.

3.4 Operating Principle of The FB-PS-ZVS DC/DC Converter

The transformer primary voltage (V_P), primary current (I_P) and secondary voltage (V_S) waveforms of the FB-PS-ZVS DC/DC converter are given in Figure 3.3 for the steady-state operating condition. Since the secondary current is the scaled version of the primary current (ideally), the secondary current waveform is not given in the figure.

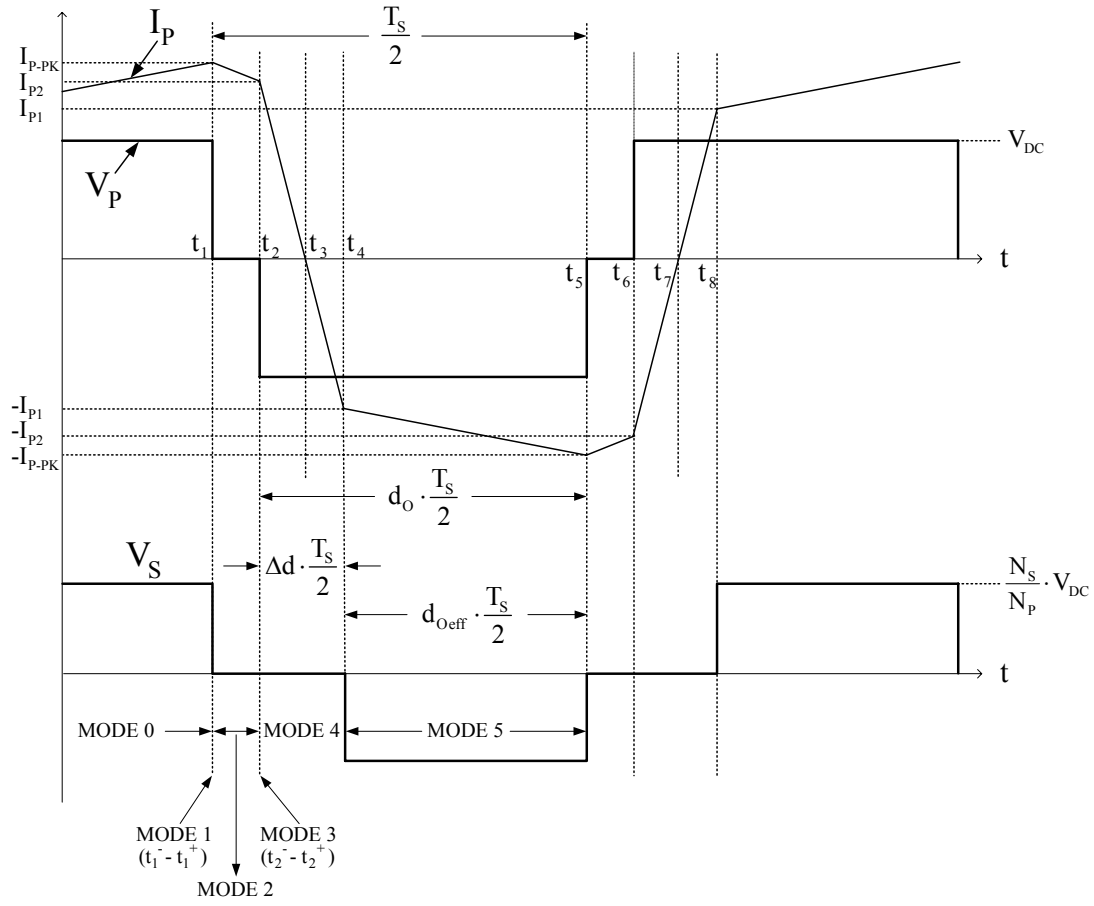


Figure 3.3 Transformer primary voltage, primary current, and secondary voltage waveforms of the FB-PS-ZVS DC/DC converter.

During a half switching period, mode by mode operation of the FB-PS-ZVS DC/DC converter is explained in 6 circuit modes for steady-state operation. In the second half of the period events repeat in the same manner as in the first half. Therefore, only the first half is discussed.

3.4.1 Mode 0

In this mode the switches T_1 and T_2 are conducting and the power is transferred from the input to the output. In Figure 3.4, the primary and secondary current conduction paths for this mode are indicated on the converter circuit diagram in bold lines and the primary voltage and current waveforms are given in the same figure, where the voltage and current waveform sections belonging to this mode are marked in bold.

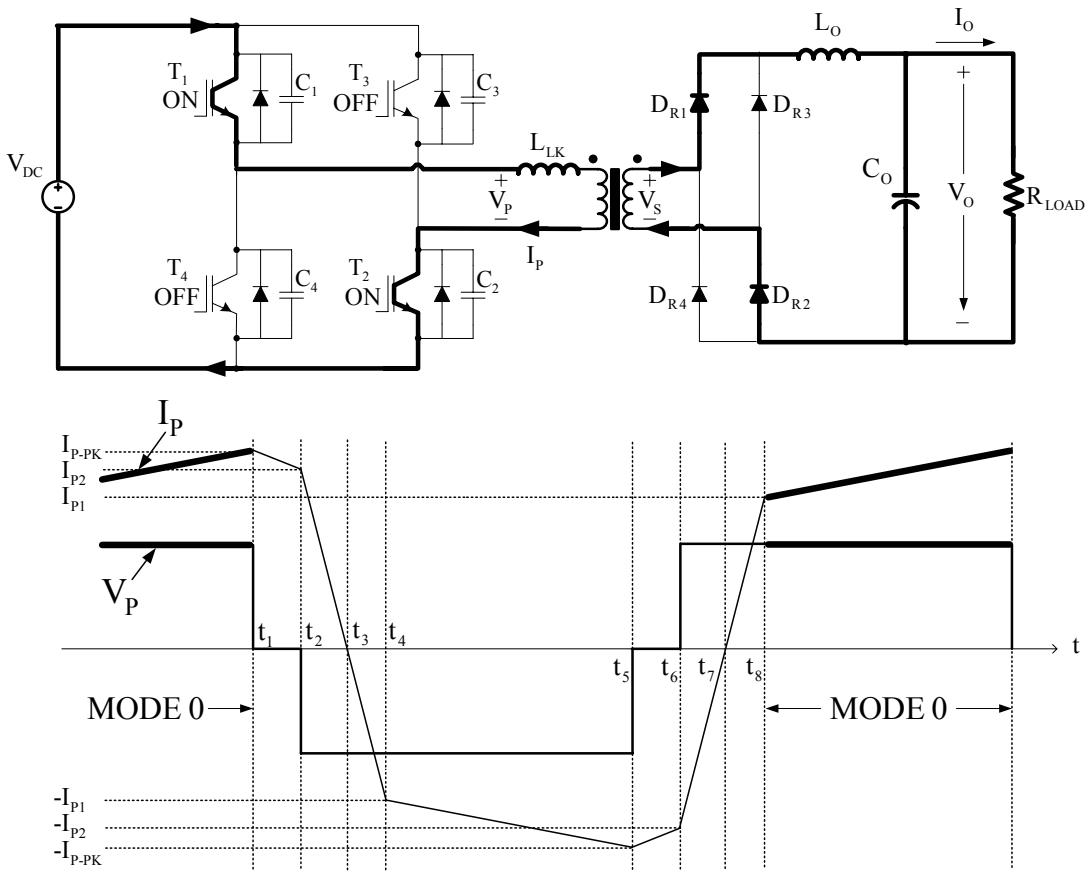


Figure 3.4 The circuit diagram and primary voltage and primary current waveforms of the FB-PS-ZVS DC/DC converter in mode 0.

The rise of the transformer primary current in this mode can be explained with the aid of the equivalent circuit diagram of the converter for mode 0. As shown in Figure 3.5, the full-bridge inverter output is modeled as a DC voltage source, the transformer is modeled with its T equivalent circuit and the output section of the DC/DC converter is modeled with the primary referred filter inductor (L_O') and primary referred output DC voltage source (V_O'). Since the magnetizing inductance (L_M) of the transformer is much larger than the transformer leakage inductance (L_{LK1} + L_{LK2}'), the parallel branch, where L_M exists, behaves as open-circuit ideally (that's why in Figure 3.5 L_M is connected in the equivalent circuit with dashed lines). In this mode, the slope of the primary current is $(V_{DC} - V_O')/L_O'$. Since the leakage inductance is significantly lower than the primary referred filter inductor value, it is neglected in the primary current slope expression. At the end of this mode, the primary current reaches to its maximum value ($+I_{P\text{-}PK}$).

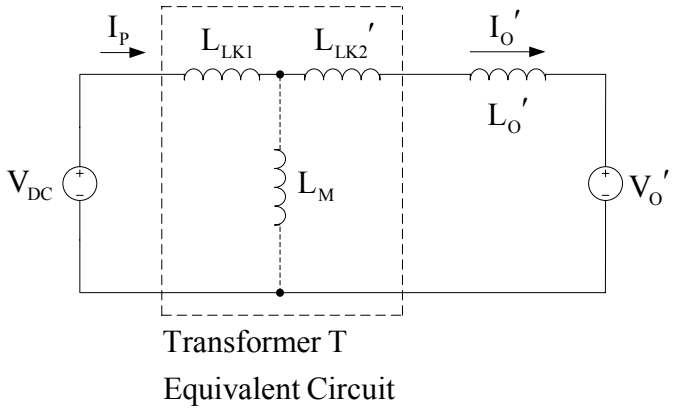


Figure 3.5 The equivalent circuit diagram of the FB-PS-ZVS DC/DC converter for mode 0.

3.4.2 Mode 1

This mode starts with the turn-off of the switch T_1 and the primary current starts to flow through the capacitors, C_1 and C_4 as shown in Figure 3.6. The primary current charges C_1 while discharging C_4. At the end of this mode, the voltage across C_1 clamps to V_{DC} and the voltage across C_4 decreases to zero. Since this mode consists

of only charge and discharge operations, it lasts a short time interval (from t_1^- to t_1^+). In this interval the load current flows through the transformer secondary winding. Therefore, on the primary voltage waveform this mode is demonstrated with the fall of the voltage from $+V_{DC}$ to zero and also in Figure 3.6 this falling edge is given in detail. The equivalent circuit diagram of the FB-PS-ZVS DC/DC converter for this mode is given in Figure 3.7.

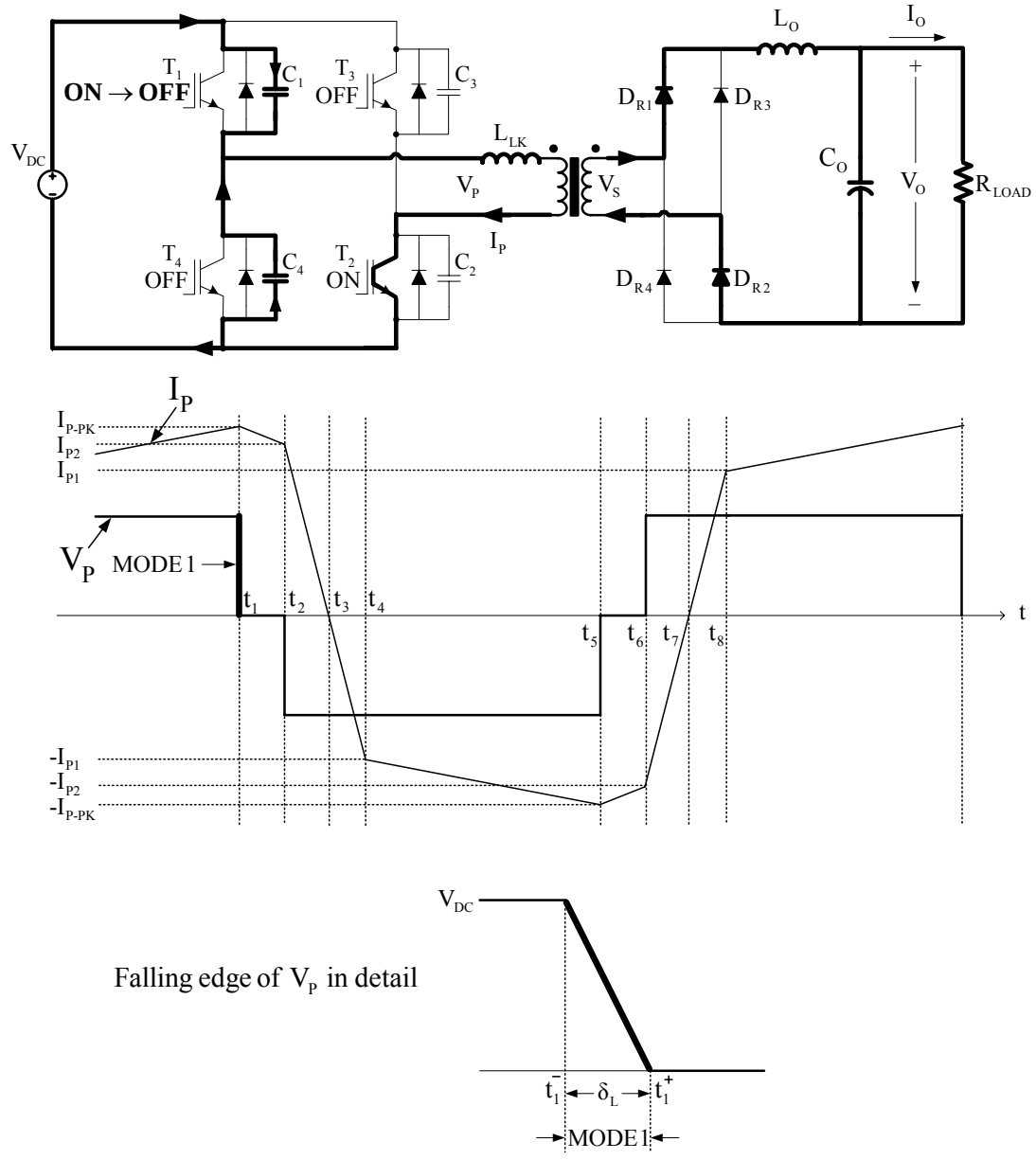


Figure 3.6 The circuit diagram and primary voltage and primary current waveforms of the FB-PS-ZVS DC/DC converter in mode 1.

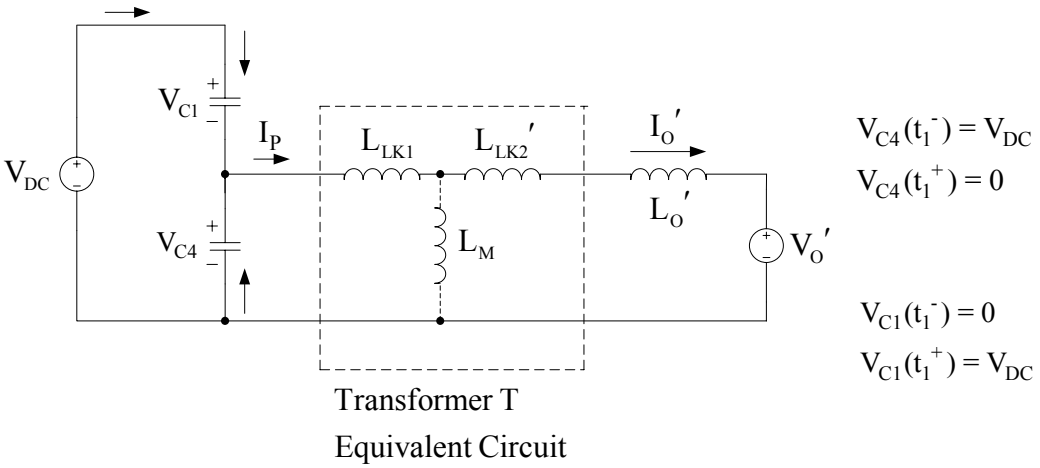


Figure 3.7 The equivalent circuit diagram of the FB-PS-ZVS DC/DC converter for mode 1.

In mode 1, the total required energy to charge C_1 and discharge C_4 is provided not only from the stored energy of leakage inductance, but also from the stored energy of the output filter inductor. At the beginning of mode 1, the primary current is at its maximum value ($+I_{P\text{-}PK}$). Since at rated load current the stored energy in the output filter inductor is significantly larger than the required energy to charge C_1 and discharge C_4, these capacitors are assumed to be charged or discharged linearly with constant current ($I_{P\text{-}PK}/2$). Because in this mode, the two capacitors are effectively in parallel and equally share the primary current.

The voltage waveforms across the switches T_1 and T_4 (V_{C1} and V_{C4}) in this mode are shown in Figure 3.8. In this figure, V_{C4} decreases to zero in the time interval of δ_L. Beyond this point, T_4 can be turned on with zero voltage on it. Hence, to satisfy ZVS condition the dead-time between T_1 and T_4 switch gate PWM signals must be at least as much as δ_L which is given in (3.2).

$$\delta_L = \frac{(C_1 + C_4) \cdot V_{DC}}{I_{P\text{-}PK}} \tag{3.2}$$

The dead-time between the switches T_1 and T_4 is calculated for the minimum peak primary current at which the ZVS condition is satisfied. If the load current reduced further, the ZVS condition is lost which results in the switching power loss on the switches T_1 and T_4.

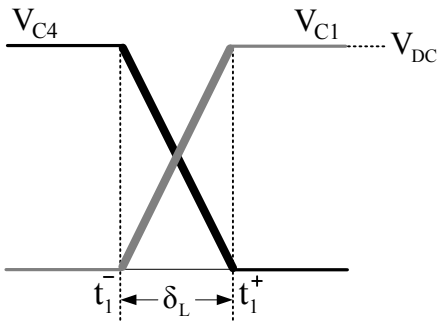


Figure 3.8 The voltage waveforms across the switches T_1 and T_4 in mode 1.

3.4.3 Mode 2

At the end of mode 1 the capacitor C_4 is discharged, and in this mode the freewheeling diode of the switch T_4 (D_4) is forward-biased and starts to conduct the primary current as shown in Figure 3.9. Beyond this point, T_4 can be turned on with zero voltage on it and ZVS condition is satisfied.

In this mode the primary current freewheels through the switch T_2 and the diode D_4. The fall of the transformer primary current from $I_{P\text{-}PK}$ can be investigated from the equivalent circuit diagram of the FB-PS-ZVS DC/DC converter for mode 2 which is given in Figure 3.10. At the end of this mode, the primary current reduces to the magnitude of I_{P2} with the slope $-V_O'/L_O'$.

In this mode the voltage at the primary winding is zero and negligibly small at the secondary winding.

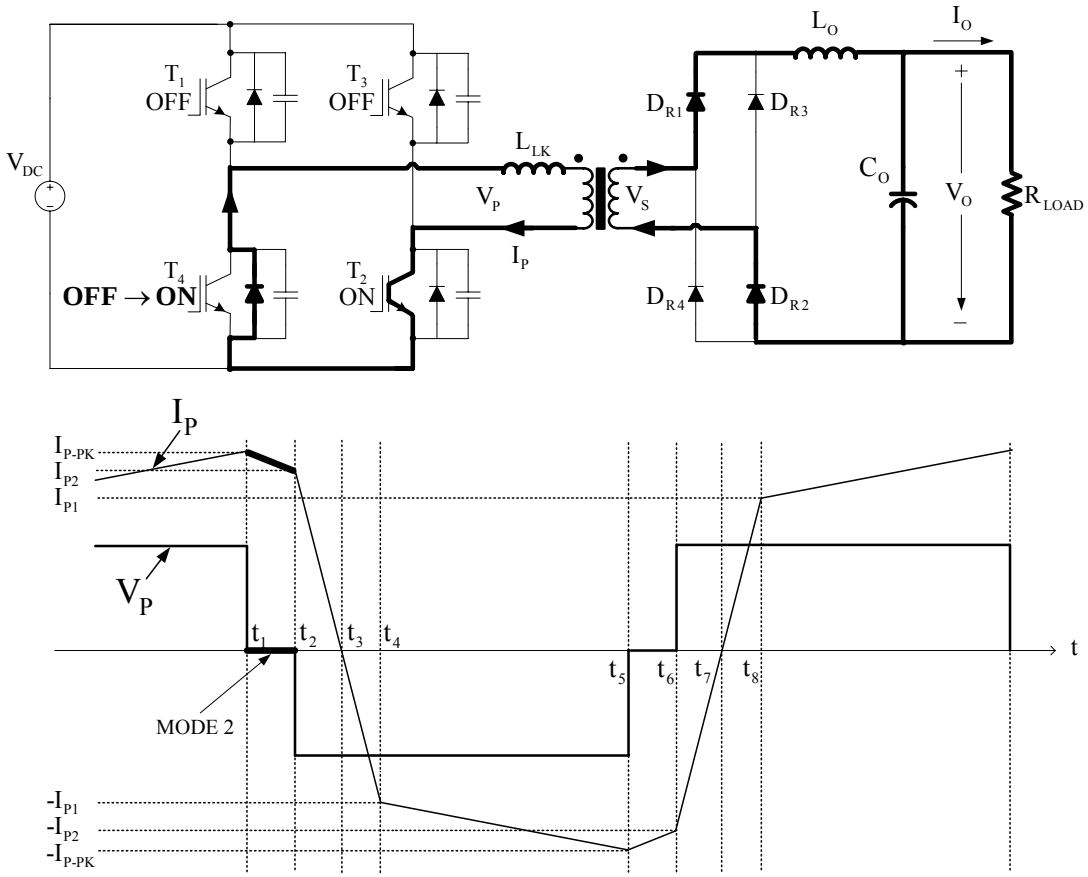
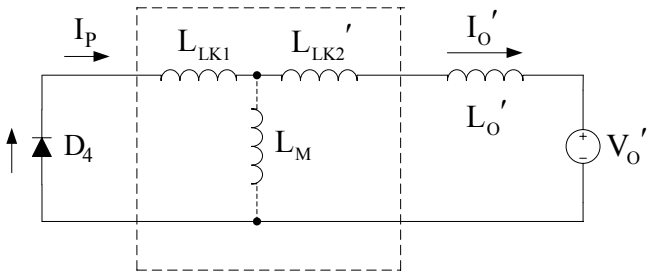


Figure 3.9 The circuit diagram and primary voltage and primary current waveforms of the FB-PS-ZVS DC/DC converter in mode 2.



Transformer T
Equivalent Circuit

Figure 3.10 The equivalent circuit diagram of the FB-PS-ZVS DC/DC converter for mode 2.

3.4.4 Mode 3

This mode starts with the turn-off of the switch T_2 and the primary current starts to flow through the capacitors C_2 and C_3 as shown in Figure 3.11. The primary current charges C_2 while discharging C_3. At the end of this mode, the voltage across C_2 clamps to V_{DC} and the voltage across C_3 decreases to zero. Since this mode consists of only charge and discharge operations, it lasts a short time interval (from t_2^- to t_2^+). Therefore, on the primary voltage waveform this mode is demonstrated with the fall of the voltage from zero to $-V_{DC}$ and also in Figure 3.11 this falling edge is given in detail for three possible operating conditions.

The equivalent circuit diagrams of the FB-PS-ZVS DC/DC converter for this mode are given in Figure 3.12. At the beginning of this mode the equivalent circuit of the converter is shown in Figure 3.12.a. The capacitor C_2 begins to get charged by the primary current and when the voltage across C_2 becomes higher than the total voltage drop value on the leakage inductance of the transformer and the full-bridge rectifier diodes D_{R3} and D_{R4}, these diodes turn on and start conducting. Since all the diodes in the full-bridge rectifier are now conducting, the secondary winding of the transformer is short-circuited. Therefore, while the primary voltage of the transformer is developing from 0 to $-V_{DC}$ in this mode, the secondary voltage remains zero as shown in Figure 3.11. The equivalent circuit diagram indicating this condition is given Figure 3.12.b.

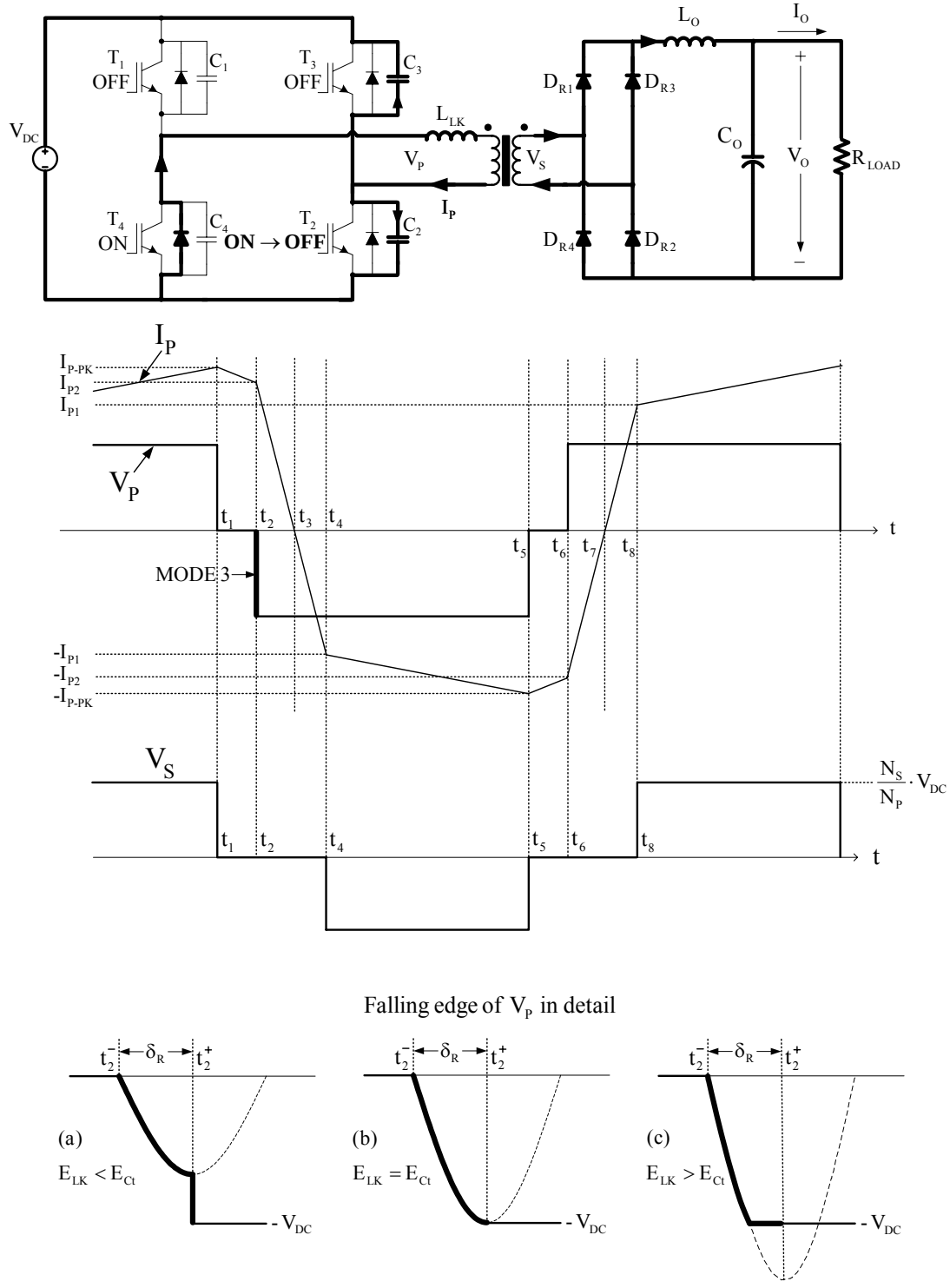


Figure 3.11 The circuit diagram, primary voltage, primary current, secondary voltage, and the zoomed primary voltage waveforms of the FB-PS-ZVS DC/DC converter in mode 3.

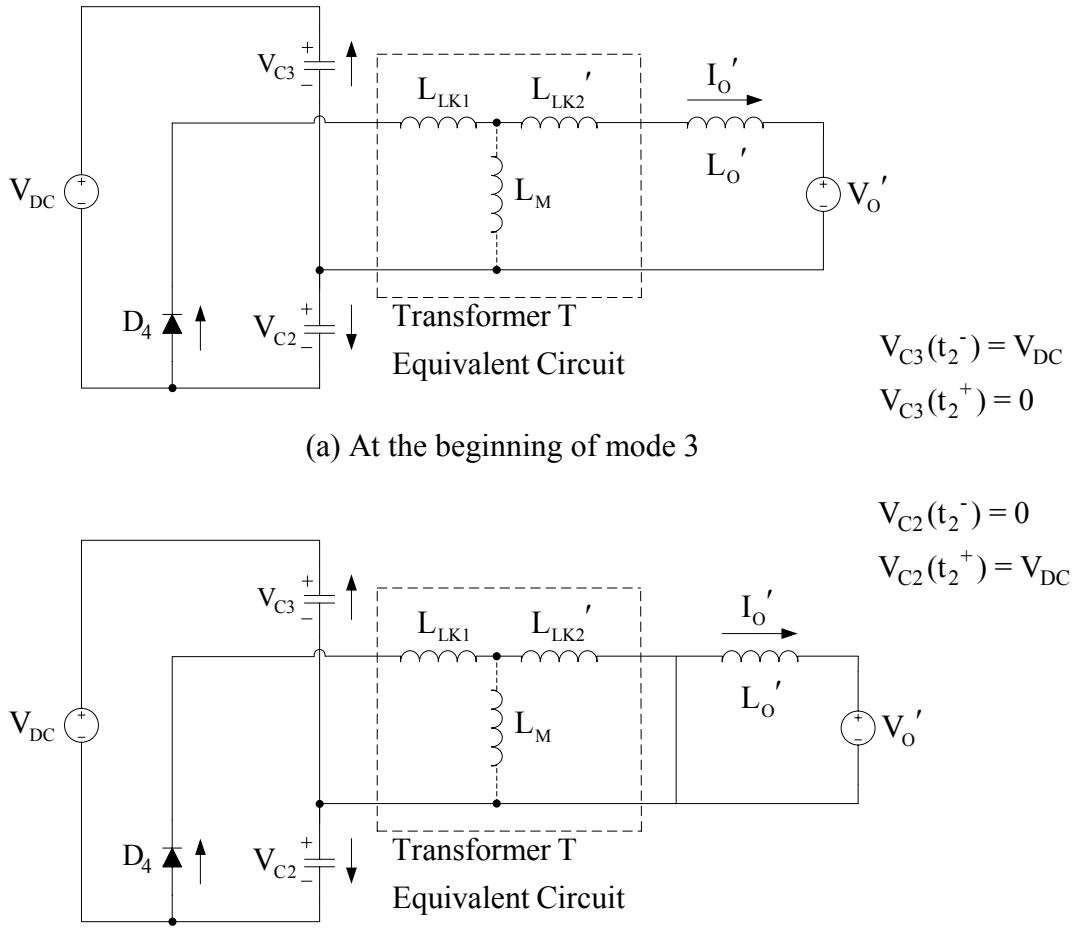


Figure 3.12 The equivalent circuit diagrams of the FB-PS-ZVS DC/DC converter for mode 3.

In this mode, the total required energy to charge C_2 and discharge C_3 (E_{Ct}) is supplied from the stored energy in the leakage inductance of the transformer (E_{LK}). Resulting from three different load current values, the falling edge of the primary voltage waveform is shown in detail for the corresponding three operating conditions in Figure 3.11, such as $E_{LK} < E_{Ct}$, $E_{LK} = E_{Ct}$, and $E_{LK} > E_{Ct}$. These primary voltage waveforms are given with the assumption that the switch T_3 is turned on at t_2^+. If T_3 is turned on when E_{LK} is lower than E_{Ct}, T_3 could not turn on with zero voltage on it since C_3 could not be completely discharged and ZVS could not be achieved. To satisfy the ZVS condition, E_{LK} must be higher than E_{Ct} as given in (3.3).

$$\frac{1}{2}\cdot L_{LK}\cdot {I_{P2}}^2 \geq \frac{1}{2}\cdot C_t\cdot {V_{DC}}^2 \tag{3.3}$$

In (3.3) I_{P2} is the primary current value at the beginning of mode 3. C_t is the total equivalent resonant capacitor value for this mode as given in (3.4).

$$C_t = C_2 + C_3 \tag{3.4}$$

The capacitors C_2 and C_3 are charged and discharged with resonant operation between these capacitors and the transformer leakage inductance. Due to this resonance, a sinusoidal voltage appears across C_2 and C_3. The voltage across C_2 rises from zero to its peak value at one fourth of the resonant period (δ_R) as shown for three operating conditions in Figure 3.13. If T_2 voltage is $+V_{DC}$ at the end of this mode ($t = t_2^+$), this means that T_3 voltage is zero and it can be turned on with zero voltage on it. For the other case ($E_{LK} < E_{Ct}$) ZVS could not be achieved. In order to achieve ZVS, the dead-time between T_2 and T_3 switch gate PWM signals must be at least as much as δ_R which is given in (3.5).

$$\delta_R = \frac{T_R}{4} = \frac{\pi}{2}\sqrt{L_{LK}\cdot C_t} \tag{3.5}$$

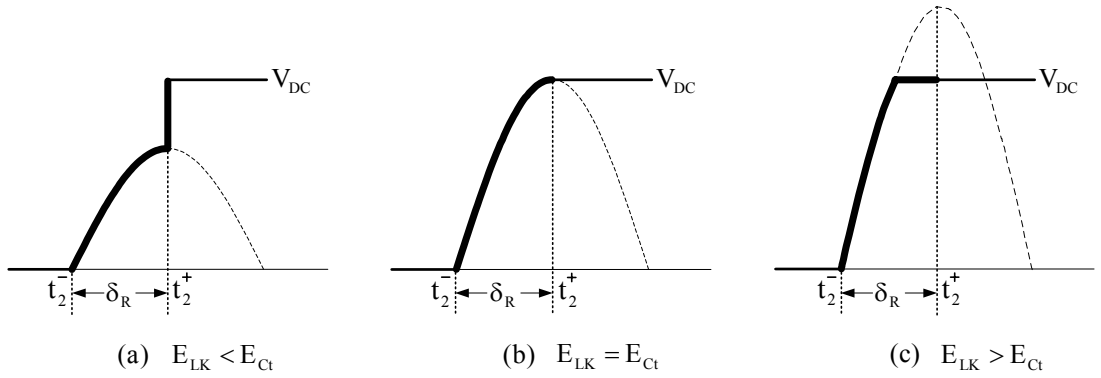


Figure 3.13 The voltage waveforms across the switch T_2 for three different primary current values in mode 3.

In the above given theoretical analysis for mode 3, it is assumed that T_3 is turned on after a time delay of δ_R following the turn off of T_2. The voltage waveforms in Figure 3.13 are obtained by taking this assumption into account. Due to the hardware implementation constraints, practically the dead-time between the switches (T_2 and T_3) may be required to be higher than the time interval δ_R, which is calculated by utilizing only the switch parasitic capacitance. Hence, T_3 could not turn on with zero voltage on it even though the ZVS condition is satisfied ($E_{LK} > E_{Ct}$). Therefore, some measures must be taken to compensate the effect of the initially specified dead-time. The design process involving this issue is included in Chapter 4.

3.4.5 Mode 4

At the end of mode 3 the capacitor C_3 is discharged completely, and in this mode the freewheeling diode of the switch T_3 (D_3) is forward-biased and starts to conduct the primary current as shown in Figure 3.14. Therefore, T_3 can be now turned on with zero voltage on it and the ZVS condition is satisfied.

The primary current starts to decrease rapidly with the slope $-V_{DC}/L_{LK}$, while the diodes D_3 and D_4 are conducting during the time interval from t_2^+ to t_3. In the time interval from t_3 to t_4, the primary current increases rapidly with the same slope while the switches T_3 and T_4 are conducting. The equivalent circuit diagrams for both cases in this mode are given in Figure 3.15. At the end of this mode, the primary current reaches to a magnitude of $-I_{P1}$, where the primary referred value of the load current is the same ($-I_{P1}$) at $t = t_4$.

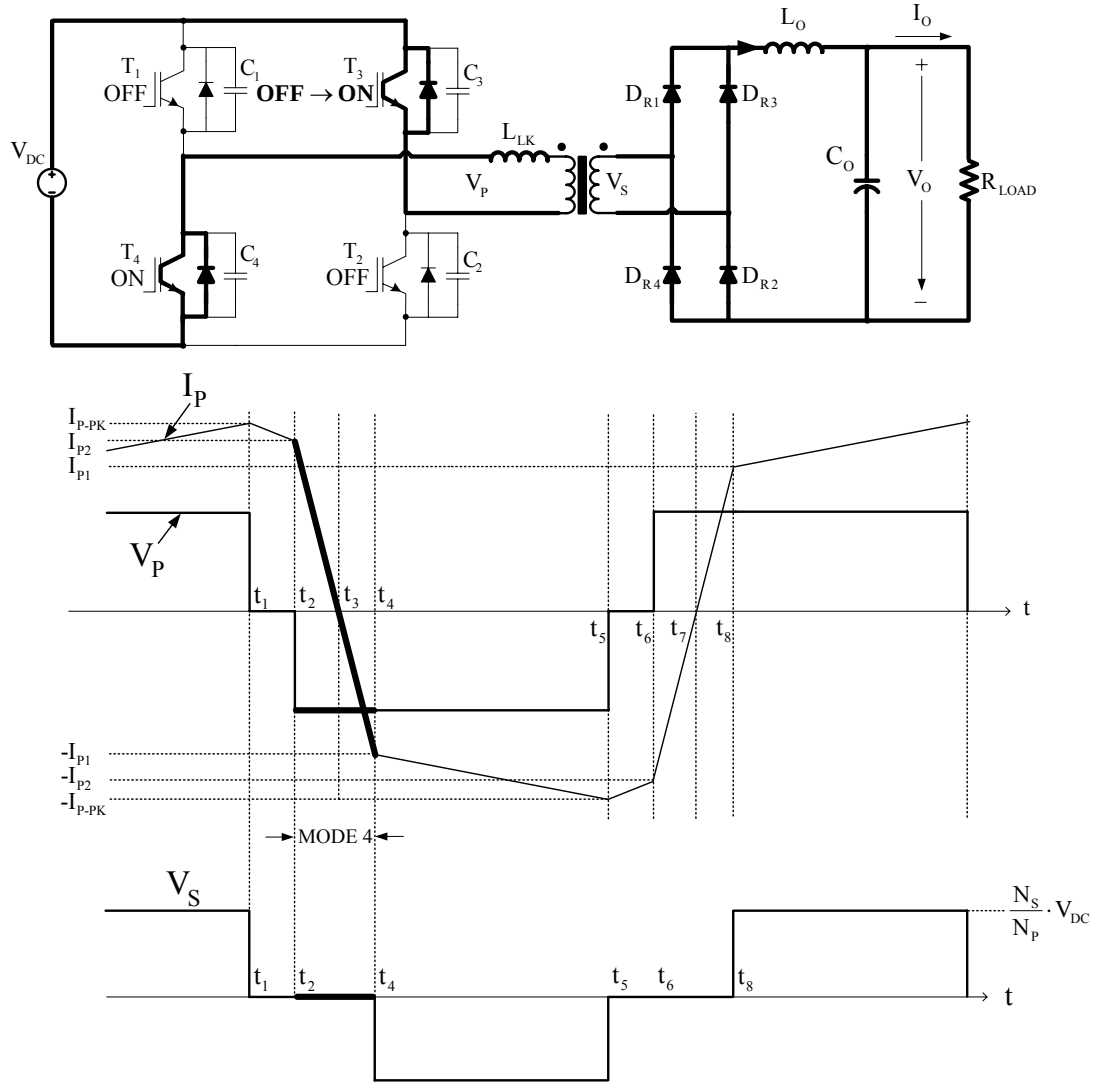
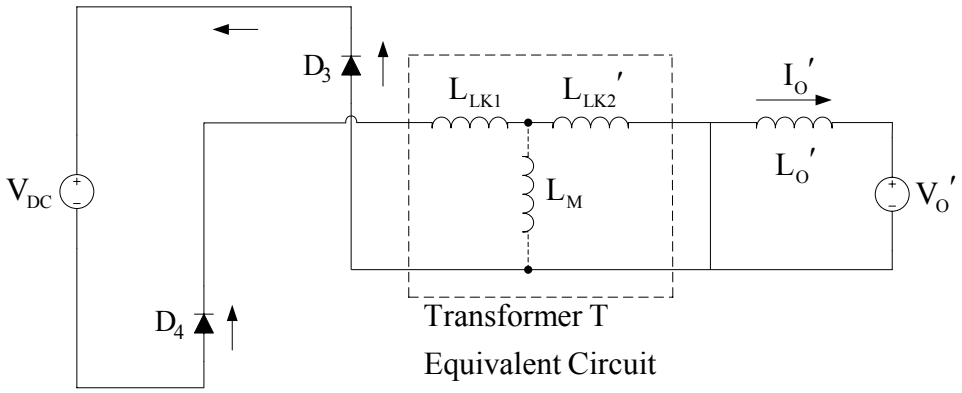
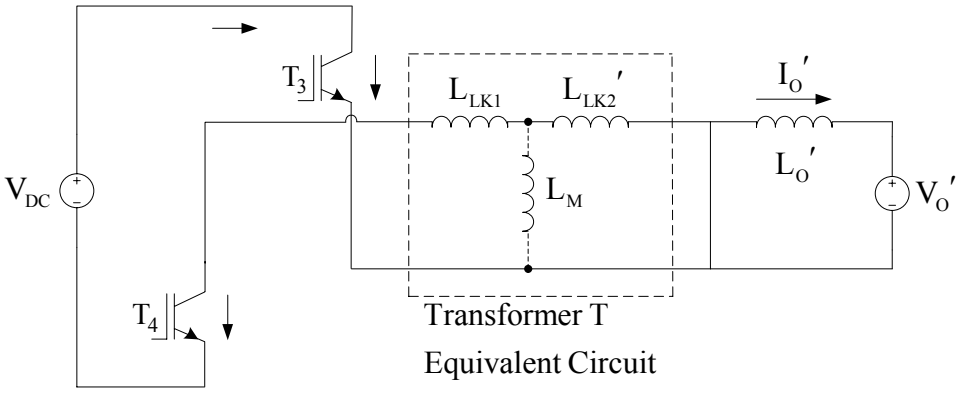


Figure 3.14 The circuit diagram and primary voltage, primary current, and secondary voltage waveforms of the FB-PS-ZVS DC/DC converter in mode 4.

In this mode, since all rectifier diodes are conducting, the secondary winding of the transformer is still short-circuited. Therefore, as shown in Figure 3.14 the voltage across the transformer secondary winding also remains zero in this mode.



(a) For $t_2^+ < t < t_3$



(b) For $t_3 < t < t_4$

Figure 3.15 The equivalent circuit diagrams of the FB-PS-ZVS DC/DC converter for mode 4.

3.4.6 Mode 5

At the end of mode 4 the current flowing through the rectifier diodes D_{R1} and D_{R2} is decreased to zero, and in this mode the load current flows only through the diodes D_{R3} and D_{R4} as shown in Figure 3.16.

In this mode, the voltage at the secondary winding develops again and the output filter inductor starts to store energy. Hence, the power transfer from the input to the output is started again. The equivalent circuit diagram of the converter for this mode is shown in Figure 3.17. At the end of this mode the primary current reaches its negative peak value ($-I_{P\text{-}PK}$).

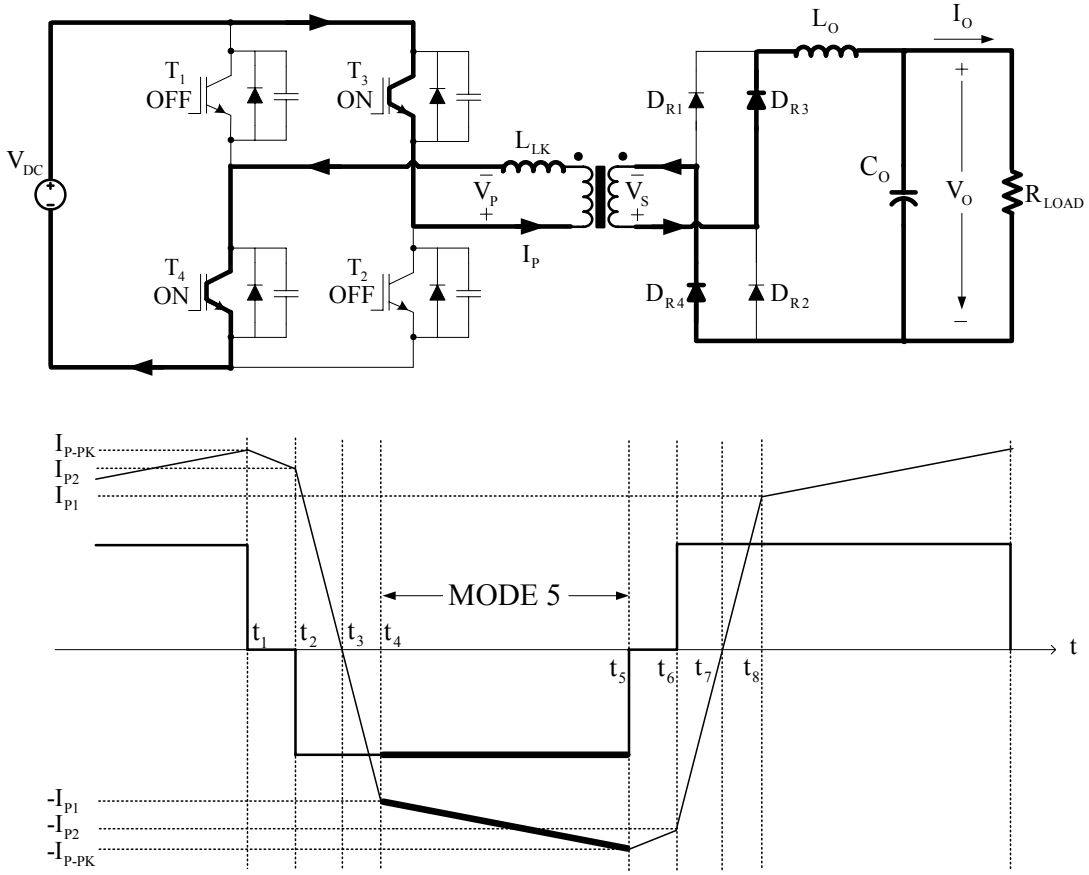


Figure 3.16 The circuit diagram and primary voltage and current waveforms of the FB-PS-ZVS DC/DC converter in mode 5.

In summary, all switching devices in the full-bridge inverter of the FB-PS-ZVS DC/DC converter turn on and off with ZVS condition. However, ZVS is achieved in the both inverter legs by different mechanisms.

The lagging leg switches T_2 and T_3 turn on with ZVS when the stored energy in the leakage inductance of the transformer is adequate to charge and discharge the capacitors C_2 and C_3. However, the leading leg switches T_1 and T_4 turn on under ZVS condition for lower load current values since the stored energy in the output filter inductor is utilized additionally in this switching transition.

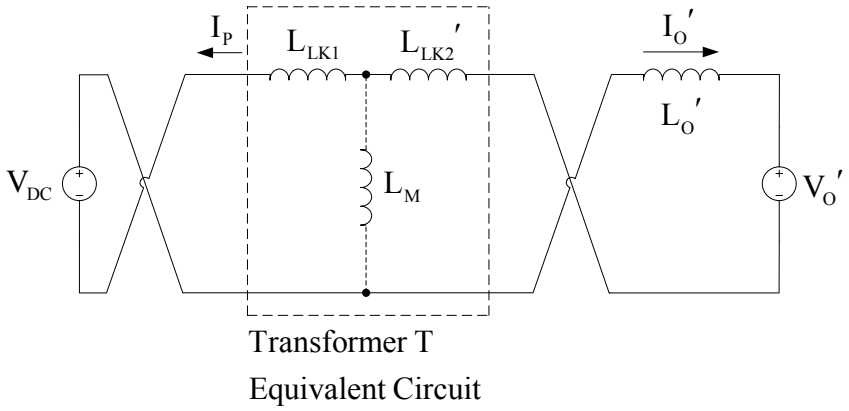


Figure 3.17 The equivalent circuit diagram of the FB-PS-ZVS DC/DC converter for mode 5.

3.5 Analysis of The FB-PS-ZVS DC/DC Converter

3.5.1 Zero Voltage Switching Condition

With the strong influence of the stored energy in the output filter inductor, ZVS is achieved by the switches T_1 and T_4 (leading leg switches) for wider range of the load current than the switches T_2 and T_3 (lagging leg switches). I_{P2}, the magnitude of the primary current at the beginning of mode 3 must be at least equal to the critical current to satisfy the ZVS condition for the switches T_2 and T_3. The magnitude of the critical current (I_{P2Cr}), which is derived from the ZVS condition in (3.3), is given in (3.6).

$$I_{P2Cr} = \sqrt{\frac{C_t}{L_{LK}}} \cdot V_{DC} \tag{3.6}$$

It should be kept in mind that the critical current expression given in (3.6) is valid when the dead-time between the lagging leg switches is one fourth of the resonant period (δ_R) as given in (3.5). However, especially for the high voltage switching devices such as IGBTs (where the required dead-time is large), it is not favorable to determine the dead-time by utilizing the calculated value from (3.5), which employs

only the switch parasitic capacitance. By utilizing the additional resonant components, the derivation of the critical current for an initially specified dead-time is discussed in Chapter 4.

Since power is not transferred from the input voltage source to the load in mode 2, the primary current at the beginning of mode 3 (I_{P2}) is the referred value of the output filter inductor current to the primary. As can be observed from the load current waveform in Figure 3.18, the load current value at $t = t_2^-$ (at the beginning of mode 3) is given in (3.7).

$$I_{S2} = I_{S\text{-}PK} - \frac{V_O}{L_O} \cdot \left(1 - d_{O,ZVS}\right) \cdot \frac{T_S}{2} \tag{3.7}$$

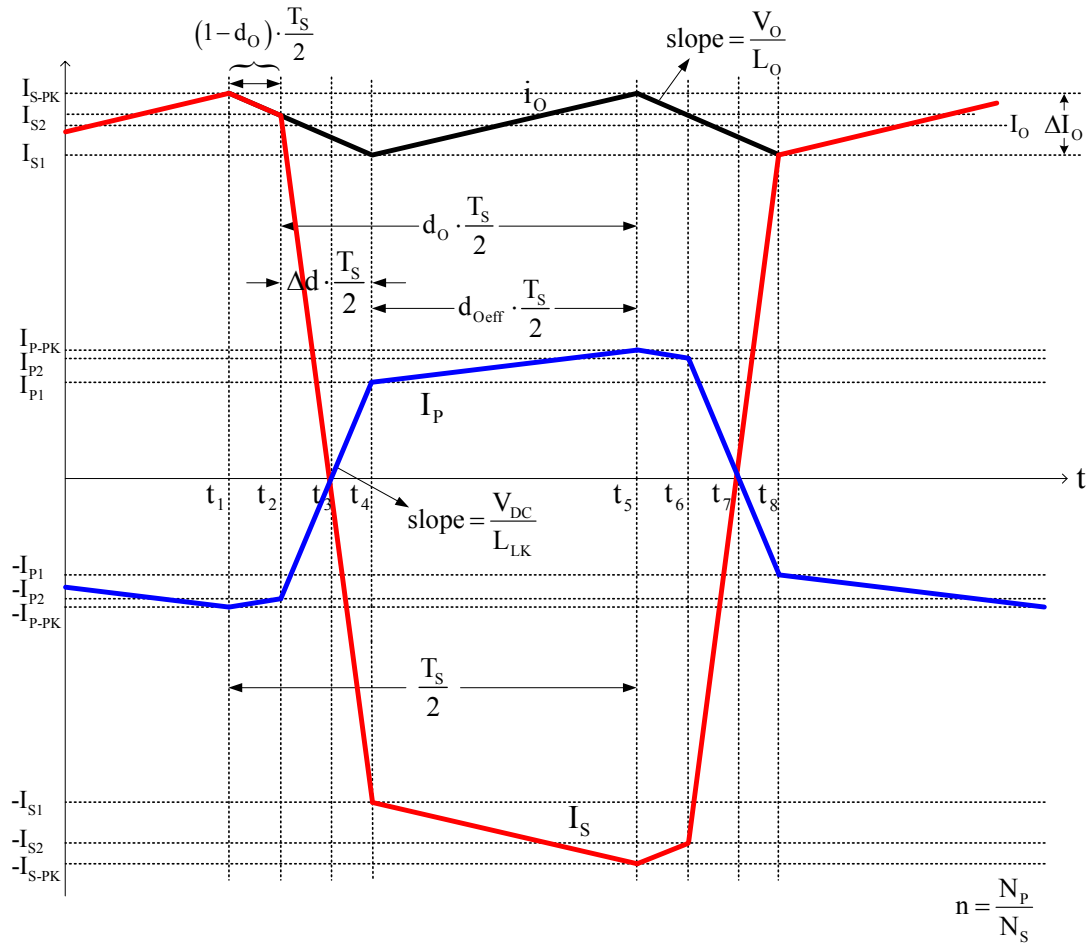


Figure 3.18 The primary, secondary, and load current waveforms.

From (3.7) the value of I_{P2} is obtained as in (3.8) by replacing $I_{S\text{-}PK}$ with the sum of the average load current (I_O) and the half of the peak to peak value of the load ripple current ($\Delta I_O/2$), where $I_{S\text{-}PK}$ is the peak value of the transformer secondary winding current and $d_{O,ZVS}$ is the d_O value at the ZVS boundary.

$$I_{P2} = \frac{N_S}{N_P} \cdot \left(I_O + \frac{\Delta I_O}{2} - \frac{V_O}{L_O} \cdot \left(1 - d_{O,ZVS}\right) \cdot \frac{T_S}{2} \right) \tag{3.8}$$

Inserting the critical current expression (given in (3.6)) for I_{P2}, (3.8) can be arranged to provide the load current that satisfies the ZVS condition as in (3.9).

$$I_O \geq \frac{N_P}{N_S} \cdot \sqrt{\frac{C_T}{L_{LK}}} \cdot V_{DC} - \frac{\Delta I_O}{2} + \frac{V_O}{L_O} \cdot \left(1 - d_{O,ZVS}\right) \cdot \frac{T_S}{2} \tag{3.9}$$

3.5.2 Input to Output DC Voltage Relation

If the transformer is designed to have large leakage inductance, the DC/DC converter can be operated under ZVS condition for wider range of the load current. However, in such a case the duration of mode 4 increases due to the reduction in the slope of the primary current (V_{DC}/L_{LK}). Therefore d_{Oeff}, shown on the transformer secondary voltage waveform in Figure 3.3, will decrease since in this mode the voltage across the secondary winding is zero. The effective duty cycle, d_{Oeff} is the ratio of the total duration of voltage ($+V_{DC}/n$ or $-V_{DC}/n$) appearing at the transformer secondary winding in a switching cycle, to the switching period. The reduction in d_{Oeff} decreases the DC voltage conversion ratio of the converter. The FB-PS-ZVS DC/DC converter is a step-down derived and isolated DC/DC converter; hence its DC voltage conversion ratio is given in (3.10). The DC voltage conversion ratio is the same as that of the full-bridge DC/DC converter, which was derived in Chapter 2.

$$\frac{V_O}{V_{DC}} = \frac{N_S}{N_P} \cdot d_{Oeff} \tag{3.10}$$

As shown on the transformer primary and secondary voltage waveforms in Figure 3.3, d_O is greater than d_{Oeff} as much as duty cycle loss (Δd) as expressed in (3.11).

$$d_{Oeff} = d_O - \Delta d \tag{3.11}$$

Δd can be obtained as in (3.12) by utilizing the primary current waveform section belonging to mode 4, in Figure 3.18.

$$\Delta d = \frac{I_{P1} + I_{P2}}{\frac{V_{DC}}{L_{LK}} \cdot \frac{T_S}{2}} \tag{3.12}$$

The primary current value at the end of mode 4 (I_{P1}) can be obtained from the load current waveform in Figure 3.18 and it is expressed in (3.13).

$$I_{P1} = \frac{N_S}{N_P} \cdot \left(I_O - \frac{\Delta I_O}{2} \right) \tag{3.13}$$

Δd can be expressed as in (3.14) by inserting the expressions for I_{P1} (given in (3.13)) and I_{P2} (given in (3.8)), into (3.12).

$$\Delta d = \frac{\frac{N_S}{N_P}}{\frac{V_{DC}}{L_{LK}} \cdot \frac{T_S}{2}} \cdot \left(2 \cdot I_O - \frac{V_O}{L_O} \cdot (1 - d_O) \cdot \frac{T_S}{2} \right) \tag{3.14}$$

d_O can be obtained as in (3.15) by inserting d_{Oeff} (given in (3.10)) and Δd (given in (3.14)) expressions in (3.11).

$$d_O = \frac{n \cdot V_O + \frac{4 \cdot L_{LK} \cdot I_O}{n \cdot T_S} - \frac{L_{LK} \cdot V_O}{n \cdot L_O}}{V_{DC} - \frac{L_{LK} \cdot V_O}{n \cdot L_O}} \tag{3.15}$$

As expressed in (3.15), d_O depends on the leakage inductance of the transformer, the transformer turns ratio, the output filter inductor, the switching period, the input DC voltage, the load current, and the output voltage.

To observe the relationship between d_{Oeff} and d_O, (3.10) is inserted into (3.15) and the resulting expression for d_{Oeff} is given in (3.16). In this expression I_O/V_O is simplified as $1/R_O$.

$$d_{Oeff} = \frac{d_O}{1 + \frac{4 \cdot L_{LK}}{n^2 \cdot R_O \cdot T_S} - \frac{L_{LK}}{n^2 \cdot L_O} + d_O \cdot \frac{L_{LK}}{n^2 \cdot L_O}} \tag{3.16}$$

In (3.16) the term $L_{LK}/(n^2 \cdot L_O)$ can be neglected since it is small compared to the other terms and (3.17) can be obtained.

$$d_{Oeff} = \frac{d_O}{1 + \frac{4 \cdot L_{LK}}{n^2 \cdot R_O \cdot T_S}} \tag{3.17}$$

As can be observed from (3.17) if the leakage inductance is increased, d_{Oeff} will decrease for the same d_O. Although the leakage inductance influences the ZVS condition advantageously, it has an adverse effect on the DC voltage conversion ratio of the converter. Also d_{Oeff} depends on the transformer turns ratio, the switching frequency period, the load current, and the output voltage.

With the basic converter analysis being completed, the next chapter attempts the analytical design of a 5 kW FB-PS-ZVS DC/DC converter.

CHAPTER 4

DESIGN OF THE FULL-BRIDGE PHASE-SHIFTED ZERO VOLTAGE SWITCHING DC/DC CONVERTER

4.1 Introduction

The analytical design of the FB-PS-ZVS DC/DC converter system is a complex procedure due to the large number of parameters involved and the interdependence of the circuit parameters. The leakage inductance of the transformer, the parasitic output capacitance of the semiconductor switches, and the transformer turns ratio are the parameters that determine the performance of the converter at the ZVS boundary and rated output current. If additional inductor and capacitors are included in the converter system, they also affect the converter performance. These parameters are the main design parameters. Optimization of the design parameters involves a method of performance calculation, evaluation, and a method of convergence (experimental, computational, iterative, etc. methods) towards the best parameter set that meet the defined design and performance constraints.

In this chapter, the conventional iterative design procedure, which includes iterations of the transformer turns ratio and leakage inductance by computational evaluation of the performance, is given with the assistance of flowcharts. It is shown that this design procedure is not favorable for power converters employing semiconductor switches which have a significant dead-time constraint. Following the conventional design method, the exhaustive search method based design procedure, which is a detailed converter design approach, is proposed. Considering the dead-time constraint, this procedure first analytically defines a range for the optimum parameters, and then carries out an exhaustive search of the design parameters. The

convenient design parameter sets, which satisfy the basic design criterion, are analytically evaluated considering efficiency and performance (such as the critical output current) at the ZVS boundary and rated load. Then, among the convenient sets, the most favorable design parameter set is selected by taking the analytical performance evaluation results into account. For the selected design parameter set, the design of the high frequency isolation transformer, which is a key component for the converter, is carried out. The transformer is first designed on-paper by employing the conventional single pass transformer design approach. The on-paper design is verified by means of an advanced software employing the Finite Element Analysis (FEA) approach. Utilizing the transformer open-circuit and short-circuit test results, the equivalent circuit parameters of the transformer are extracted. With all the main passive circuit component parameters of the 5 kW FB-PS-ZVS DC/DC converter defined, the parameters are listed at the end of this chapter.

4.2 Design Considerations of The FB-PS-ZVS DC/DC Converter

For welding applications the FB-PS-ZVS DC/DC converter can be operated at high frequencies since the switching losses are practically reduced to zero in this converter topology. In this manner the size and cost of the converter can be substantially reduced. However, for the same ZVS range, higher frequencies result in smaller d_{Oeff} as can be concluded from (3.17). Therefore, for the limited ZVS range, a corresponding maximum switching frequency boundary exists. Considering the components of a high power (several kilowatts and above) FB-PS-ZVS DC/DC converter such as the semiconductor switches, the gate driver modules, and the transformer, a switching frequency from 20 kHz to 100 kHz can be selected for a practically safe and efficient implementation.

A practical FB-PS-ZVS DC/DC converter can not satisfy the ZVS condition for the whole load range. If the ZVS condition can not be satisfied, during switching a high dv/dt will appear on the switches and this will result in significant switching losses and electromagnetic interference (EMI). The thermal stress will decrease the reliability of the converter and will force a large heatsink design. The noise generated

by the switches will couple with the other parts in the converter and other equipment in the environment via conducted or radiated paths. Therefore, a practical ZVS range must be determined initially. Satisfying the ZVS condition for a value above approximately 30% to 40% of the output current is a practically reasonable specification. Under this load range, since the switching losses of the lagging leg are relatively low due to the reduction in the load current and the leading leg operates at ZVS regardless the loading condition (the finite magnetization current at no-load is sufficient to provide ZVS in this leg), the total efficiency does not significantly degrade and the thermal stress becomes tolerable.

The transformer primary winding current at the beginning of mode 3 (I_{P2}) must be equal to or larger than the critical current (given in (3.6)) to achieve ZVS. The ZVS range can be further expanded by utilizing a high frequency transformer having larger leakage inductance or inserting an additional inductor in series with the transformer primary winding. However, the larger series inductance decreases the DC voltage conversion ratio of the DC/DC converter. The ZVS range can be calculated after specifying the leakage inductance of the transformer (if an additional series inductor exists, the total inductance of both is utilized as the equivalent resonant inductor) and the total output capacitance across each semiconductor switch in the full-bridge inverter.

Another point that must be considered in the design process is the transformer turns ratio. The ZVS range can further be increased by decreasing the transformer turns ratio, however in this case the primary current will increase and so the conduction losses of the switches in the full-bridge inverter. Also, the transformer turns ratio can not be increased significantly, since the open-circuit output voltage must be typically about 80 V to start the ignition of the arc in an arc welding machine. If the open-circuit output voltage is lower, the arc starting process becomes difficult.

The design parameters discussed in this section must satisfy several design constraints for a proper converter operation. First, the maximum value of d_{Oeff} must provide the output voltage at the rated output current. Then, the output current value

at the ZVS boundary must satisfy the initially specified ZVS range and the peak primary current at the rated output current must be below the initially specified maximum value. The design parameter sets satisfying these constraints are obtained by utilizing an analytical approach for search boundaries and an exhaustive search, and the convenient sets are evaluated considering the efficiency of the DC/DC converter for each set.

4.3 The Conventional Iterative Design of The FB-PS-ZVS DC/DC Converter

Based on the design considerations given in the previous section and the derived equations through the analysis of the FB-PS-ZVS DC/DC converter in Chapter 3, the conventional iterative design procedure is presented in this section [9]. The interdependence of the converter circuit parameters results in an iterative design procedure.

The specifications V_{DC}, rated values of V_O and I_O, and ΔI_O are required initially for the design process. Additionally the total resonant capacitance value (C_t), which is the total switch parasitic capacitance value in one inverter leg, is required. The design procedure is given in the following steps.

Step 1. Initially the maximum value of d_O ($d_{O\text{-}max}$) is determined. This value must be as large as possible to maximize the transformer turns ratio (N_P/N_S). The large N_P/N_S value reduces the primary current and thus the conduction losses of the semiconductor switches.

Step 2. The peak value of the transformer secondary voltage ($V_{S\text{-}PK}$) is specified in this step. It must be as low as possible to maximize N_P/N_S due to the reason given in step 1 and to reduce the voltage stress on the rectifier diodes at the secondary side. However, reducing $V_{S\text{-}PK}$ (increasing N_P/N_S), reduces the primary current and so does the ZVS range. Based on these considerations, an approximate value is assigned to $V_{S\text{-}PK}$ initially and its final value is determined after several iterations in steps 2-5.

Utilizing the inequality given in (4.1) and the application requirement at the output (high or low output voltage), an approximate value can be specified and assigned to $V_{S\text{-}PK}$ initially. The resulting transformer turns ratio is given in (4.2).

$$V_{S\text{-}PK} \geq \frac{V_O}{d_{O\text{-}max}} \tag{4.1}$$

$$n = \frac{N_P}{N_S} = \frac{V_{DC}}{V_{S\text{-}PK}} \tag{4.2}$$

Substituting n in (3.10) d_{Oeff} can be calculated.

Step 3. The minimum load current that satisfies the ZVS condition, which is also called the critical load current (I_{OCr}), is determined in this step. As expressed in the analysis section of Chapter 3, the ZVS range of the converter is calculated by utilizing the primary current at the beginning of mode 3. This critical current (I_{P2Cr}) can not be calculated initially, since in the equation (3.8) the output filter inductance and switching frequency values are not determined yet. Several iterations of steps 3-5 are required to determine the final value of I_{OCr}.

The iteration is started by setting I_{P2Cr} equal to I_{OCr}' (primary referred value of I_{OCr}) and after steps 4 and 5 are carried out, I_{P2Cr} is calculated. The iterations of steps 3-5 are repeated until changes in I_{P2Cr} are negligible.

Step 4. From equation (4.3), the leakage inductance of the transformer is calculated by using I_{P2Cr}, which is specified in the previous step. Equation (4.3) is obtained by utilizing the ZVS condition given in (3.3).

$$L_{LK} = \frac{C_t \cdot V_{DC}^{\,2}}{I_{P2Cr}^{\,2}} \tag{4.3}$$

Step 5. The operating switching frequency is calculated by using equation (4.4), which is obtained from (3.17).

$$f_S = \frac{n^2 \cdot R_O}{4 \cdot L_{LK}} \cdot \left(\frac{d_{O\text{-}max}}{d_{Oeff}} - 1 \right) \tag{4.4}$$

From equation (4.5) the output filter inductor value is calculated. This equation is obtained from the output load current waveform in the time interval between t_4 and t_5 (in mode 5). In mode 5 (or in mode 0) the voltage at the output filter inductor is $V_{DC}/n - V_O$ and the change of the current that is flowing through the inductor is ΔI_O.

$$L_O = \frac{V_{DC}/n - V_O}{\Delta I_O} \cdot \frac{d_{Oeff}}{2 \cdot f_S} \tag{4.5}$$

The value of d_O at ZVS boundary ($d_{O\text{-}ZVS}$) is calculated by using equation (3.17). In this equation R_O is calculated by utilizing I_{OCr}.

In (4.6) the calculated value of I_{P2} at the ZVS boundary (I_{P2Cr}) is given. This equation is obtained from (3.8).

$$I_{P2Cr} = \frac{N_S}{N_P} \cdot \left(I_{OCr} + \frac{\Delta I_O}{2} - \frac{V_O}{L_O} \cdot \left(1 - d_{O\text{-}ZVS}\right) \cdot \frac{1}{2 \cdot f_S} \right) \tag{4.6}$$

The first iteration is completed after implementing steps 3 to 5 again, by using the calculated value of I_{P2Cr}.

The initial design is completed after covering the design procedure given above. The flowchart illustrating the explained design procedure of the converter is given in Figure 4.1. By utilizing the obtained leakage inductance and switching frequency, further iterations may be carried out to assign the feasible design parameters.

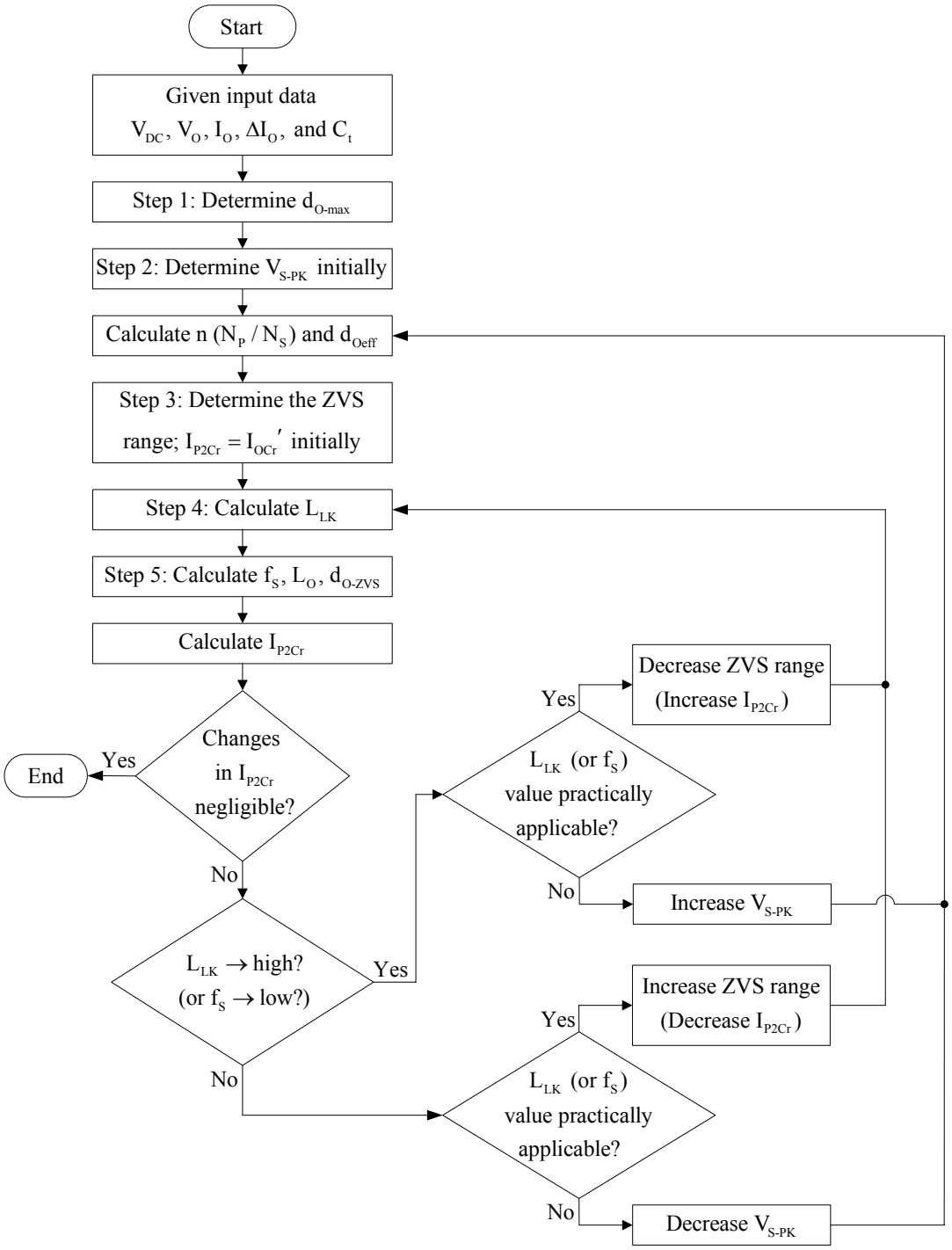


Figure 4.1 The conventional iterative design procedure flowchart of the FB-PS-ZVS DC/DC converter.

If the leakage inductance, which is calculated in step 4 after the first iteration, is high (low) there are two alternative iteration paths. One path is to decrease (increase) the

transformer turns ratio by increasing (decreasing) the peak secondary voltage magnitude (return to step 2) if the leakage inductance value is far from the practically applicable values. The other path is to reduce (increase) the ZVS range by increasing (decreasing) the value of I_{P2Cr} (return to step 3) if the leakage inductance value is close to the practically applicable values. If the switching frequency, which is calculated in step 5 after the first iteration, is low (high) there are two alternative iteration paths. These paths are similar to the procedure followed for the leakage inductance when its value is high (low).

These iterations are repeated until calculated I_{P2Cr} in step 5 approaches to the same value used in step 4.

4.4 The Exhaustive Search Method Based Design of The FB-PS-ZVS DC/DC Converter Considering The Dead-time Constraint

In the conventional iterative design procedure of the FB-PS-ZVS DC/DC converter, I_{P2Cr}, the minimum current that satisfies the ZVS condition, (also the current flowing through the transformer primary winding at the beginning of mode 3) is obtained with the assumption that the dead-time between the lagging leg switches is one-fourth of the resonant period ($T_R/4$). Due to safety reasons, for the high current switching semiconductor devices, it is not favorable to determine the dead-time by utilizing the expression given in (3.5), which is calculated by utilizing only the transformer leakage inductance and the total output parasitic capacitance of the lagging leg switches. While the dead-time requirement for MOSFETs is short (typically significantly smaller than a microsecond), IGBTs require larger dead-time due to the tail current (typically larger than 2-3 microseconds). Hence, the dead-time requirement of the circuit must be determined based on the switching device characteristics. When the dead-time introduced between the switches is larger than one-fourth of the resonant period, which is calculated by utilizing only the circuit parasitic resonant components, the switch may not turn on with zero voltage although the energy stored in the leakage inductance at the beginning of mode 3 by the primary current (I_{P2}) is higher than the total energy stored in the total capacitance

across the lagging leg switches. Thus, due to dead-time constraint in this design procedure, the dead-time is utilized as an input specification.

The transformer primary current (I_P) in mode 3 charges the capacitor across T_2, and discharges the capacitor across T_3. If T_3 is not turned on (since the dead-time interval, t_d is not expired yet) when the voltage across this switch is decreased to zero as illustrated in Figure 4.2, T_3 may turn on with a significant magnitude of voltage on it based on the transformer primary current magnitude at the beginning of mode 3 (I_{P2}). By the resonance operation, while I_{P2} is larger than the critical current (I_{P2Cr}) that is given in (3.6), the voltage across T_3 decreases to zero. During the time interval t_{M3a}, first resonance operation occurs as shown in Figure 4.2. Then, the switch voltage value remains at zero and the switch turns on with zero voltage. However, if I_{P2} is not large enough, the switch voltage value remains at zero for a short span of time interval (t_{M3b}) while the primary current decreases linearly with a slope of V_{DC}/L_{LK}. Then, the switch voltage rises again by the second resonance operation in this mode during the time interval t_{M3c}, since I_{P2} is decreased to zero and started to increase in the reverse direction. When the dead-time interval is completed and the switch T3 is turned on under hard switching condition, the voltage across T3 decreases to zero (the energy in the capacitor is dissipated in the transistor). Thus, the ZVS condition for T_3 is not satisfied although I_{P2} is larger than I_{P2Cr}.

To compensate for the effect of the initially specified dead-time for the above given case (as illustrated in Figure 4.2), additional capacitors are connected across the lagging leg switches. In [10] the FB-PS-ZVS DC/DC converter performance is investigated with the additional capacitors across the lagging leg switches as in this design method, however an analytical design method is not included. The utilized additional capacitors decrease the slope of the rising and falling edge of the switch voltage. Thus, the switch voltage decreases from V_{DC} to 0 in a larger time interval. However, in this case, due to the additional capacitors the ZVS range will be narrower. To increase the ZVS range again, an additional inductor should be connected in series with the transformer primary winding. This additional inductance value must be selected considering the fact that d_{Oeff} decreases with the increasing

total resonant inductance. Therefore, while specifying the ZVS range, the maximum obtained output voltage must be checked to find out whether it satisfies the desired output voltage level or not.

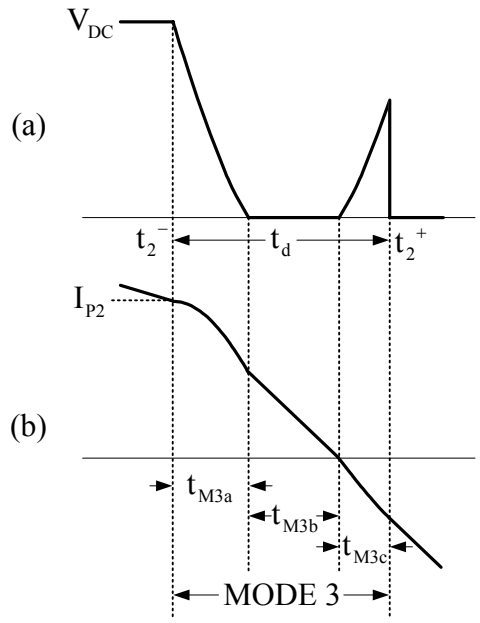


Figure 4.2 The waveforms in mode 3 when I_{P2} is slightly larger than I_{P2Cr} and t_d is larger than $T_R/4$: (a) voltage across the switch T_3, (b) transformer primary current.

The exhaustive search method based design procedure, which is explained in the following steps, outputs the design parameter sets including the total resonant inductance (L_t), total resonant capacitance (C_t), and transformer turns ratio (n) values. These parameter sets are selected based on the design constraints, which include the maximum output critical current ($I_{OCr\text{-}max}$) and the maximum transformer primary peak current ($I_{P\text{-}PK\text{-}max}$). If the calculated I_{OCr} and $I_{P\text{-}PK}$ values satisfy these conditions and the calculated output voltage is above the desired output voltage value, a design parameter set is stored. Otherwise the parameter set is discarded and the parameters are incremented and a new set is calculated and so on. For the design process, the input specifications V_{DC}, V_O, I_O, f_S, t_d, $I_{OCr\text{-}max}$, and $I_{P\text{-}PK\text{-}max}$ are required. This design procedure first calculates the search range boundary values through the steps 1 to 6, and then performs an exhaustive search of the convenient design parameter sets in the calculated search range through the steps 7 to 10.

Step 1. As an initial step, $d_{O\text{-}max}$, which indicates the maximum on time of the primary voltage that the full-bridge inverter outputs, is specified. Including the effect of the dead-time, the maximum d_O is calculated by using (4.7).

$$d_{O\text{-}max} = 1 - 2 \cdot t_d \cdot f_S \tag{4.7}$$

Step 2. Assuming the maximum d_{Oeff} is the same as the $d_{O\text{-}max}$, the maximum turns ratio is obtained by using the DC voltage conversion ratio of the converter. The maximum turns ratio, n_{max}, which is utilized in the design procedure as a search boundary, is calculated by utilizing (4.8).

$$n_{max} = d_{O\text{-}max} \cdot \frac{V_{DC}}{V_O} \tag{4.8}$$

Step 3. To specify the minimum turns ratio for the search boundary, a lower limit for d_{Oeff} is assumed where the power transfer occurs only within 25% of the switching period. Thus, determining a minimum d_{Oeff} of 0.25, n_{min} is calculated by utilizing (4.9).

$$n_{min} = 0.25 \cdot \frac{V_{DC}}{V_O} \tag{4.9}$$

Step 4. Through the exhaustive search method based design procedure, all critical current values are calculated for the C_t values in the range of its specified maximum ($C_{t\text{-}max}$) and minimum ($C_{t\text{-}min}$) values. To determine $C_{t\text{-}min}$, $L_{t\text{-}max}$ is specified initially, in this step. $L_{t\text{-}max}$ can be determined by using the same assumption in the previous step since the minimum d_{oeff} is obtained at the maximum L_t value. $L_{t\text{-}max}$ is specified from the primary current waveform in mode 4 where the primary current slope in this mode is V_{DC}/L_t. Assuming the total change in the primary current magnitude is $2\cdot(I_O/n)$ in this mode, $L_{t\text{-}max}$ can be determined using the maximum value of the transformer turns ratio. The duration of this mode can be specified by utilizing the

assumption in the previous step which assumes a minimum d_{Oeff} value of 0.25 at the maximum d_O value. Utilizing these considerations $L_{t\text{-}max}$ is given as in (4.10).

$$L_{t\text{-}max} = \frac{V_{DC}}{2 \cdot \left(I_O / n_{max} \right)} \cdot \left(\frac{3}{8 \cdot f_S} - t_d \right) \tag{4.10}$$

Step 5. Utilizing the obtained maximum value of L_t in the previous step, the minimum value of C_t, which is employed in the design procedure as a search boundary, is obtained as in (4.11). Since the minimum critical current is obtained when the dead-time between the lagging leg switches is one-fourth of the resonant period, $C_{t\text{-}min}$ is specified by equating the dead-time to the one-fourth of the resonant period.

$$C_{t\text{-}min} = \frac{1}{L_{t\text{-}max}} \cdot \left(\frac{2 \cdot t_d}{\pi} \right)^2 \tag{4.11}$$

Step 6. The maximum C_t can be obtained by utilizing only the transformer leakage inductance, which is the minimum possible L_t value ($L_{t\text{-}min}$). Utilizing $L_{t\text{-}min}$, $C_{t\text{-}max}$ can be calculated similarly as in the previous step. With the resulting expression for $C_{t\text{-}max}$ as given in (4.12), the total resonant capacitor range is obtained for the exhaustive search process.

$$C_{t\text{-}max} = \frac{1}{L_{t\text{-}min}} \cdot \left(\frac{2 \cdot t_d}{\pi} \right)^2 \tag{4.12}$$

As an initial assumption, the minimum value of the transformer leakage inductance can be assumed as low as 3 μH, which is about the minimum possible leakage inductance value of a 5 kW high frequency transformer.

Step 7. In this step, L_t is specified with the consideration that the minimum critical current is obtained when the dead-time between the lagging leg switches is

one-fourth of the resonant period. Thus, using (4.13) a corresponding L_t value is calculated for each C_t value.

$$L_t = \frac{1}{C_t} \cdot \left(\frac{2 \cdot t_d}{\pi} \right)^2 \tag{4.13}$$

Step 8. The critical current, which satisfies the ZVS condition, is calculated for the corresponding L_t and C_t as given in (4.14).

$$I_{P2Cr} = \sqrt{\frac{C_t}{L_t}} \cdot V_{DC} \tag{4.14}$$

Step 9. In this step, the maximum d_{Oeff} is calculated as given in (4.15), which is obtained by using (3.17). To calculate the maximum d_{Oeff}, $d_{O\text{-}max}$ is utilized as in the following equation.

$$d_{Oeff\text{-}max} = \frac{d_{O\text{-}max}}{\left(1 + \frac{4 \cdot L_t \cdot I_O \cdot f_S}{n^2 \cdot V_O} \right)} \tag{4.15}$$

Step 10. In this step, the calculated I_{P2Cr} and $d_{Oeff\text{-}max}$, and the primary current values are checked whether they satisfy the desired conditions for the proper operation of the converter or not. If $d_{Oeff\text{-}max}$ satisfies the desired output voltage as in (4.16), the primary current is below the desired maximum primary peak current value as in (4.17), and I_{P2Cr} is below the primary referred value of the desired maximum output critical current value as in (4.18), this data set includes the convenient design parameters and it is stored.

$$d_{Oeff\text{-}max} \geq \frac{n \cdot V_O}{V_{DC}} \tag{4.16}$$

$$\frac{I_O}{n} \leq I_{P\text{-}PK\text{-}max} \tag{4.17}$$

$$I_{P2Cr} \leq \frac{I_{OCr\text{-}max}}{n} \tag{4.18}$$

In addition to scanning the total resonant capacitance value in the specified range, there exists another scanning process utilizing the transformer turns ratio, which is carried out for each C_t value. Thus, for a C_t and L_t data set, the above three constraints are validated for the possible transformer turns ratio range (between n_{min} and n_{max}) and the adequate design parameter sets including the parameters L_t, C_t, and n are stored.

The exhaustive search method based design procedure is carried out by scanning the design parameters L_t, C_t, and n between the minimum and maximum search boundaries for these parameters. Since there exists an L_t value for each C_t value as given in (4.13), only C_t and n values are scanned in the design procedure. In the performed exhaustive search, a step value for C_t is taken as 0.5% of C_t range ($0.005*(C_{t\text{-}max}+C_{t\text{-}min})/2$) and for n a step value is taken as 1% of n range ($0.01*(n_{max}+n_{min})/2$). All possible design parameter sets are obtained in the defined range and if the obtained set satisfies the design criterion given in Step 10, this design parameter set is stored. Otherwise, the set is discarded and the search continues until the search boundaries are reached. The exhaustive search method based design procedure is illustrated in the flowchart given in Figure 4.3.

With the above exhaustive search algorithm, suitable design parameter sets are obtained for the desired ZVS range. Among these possible parameter sets, the choice of the most feasible parameter set is determined through the analytical performance analysis of the FB-PS-ZVS DC/DC converter to be conducted consequentially.

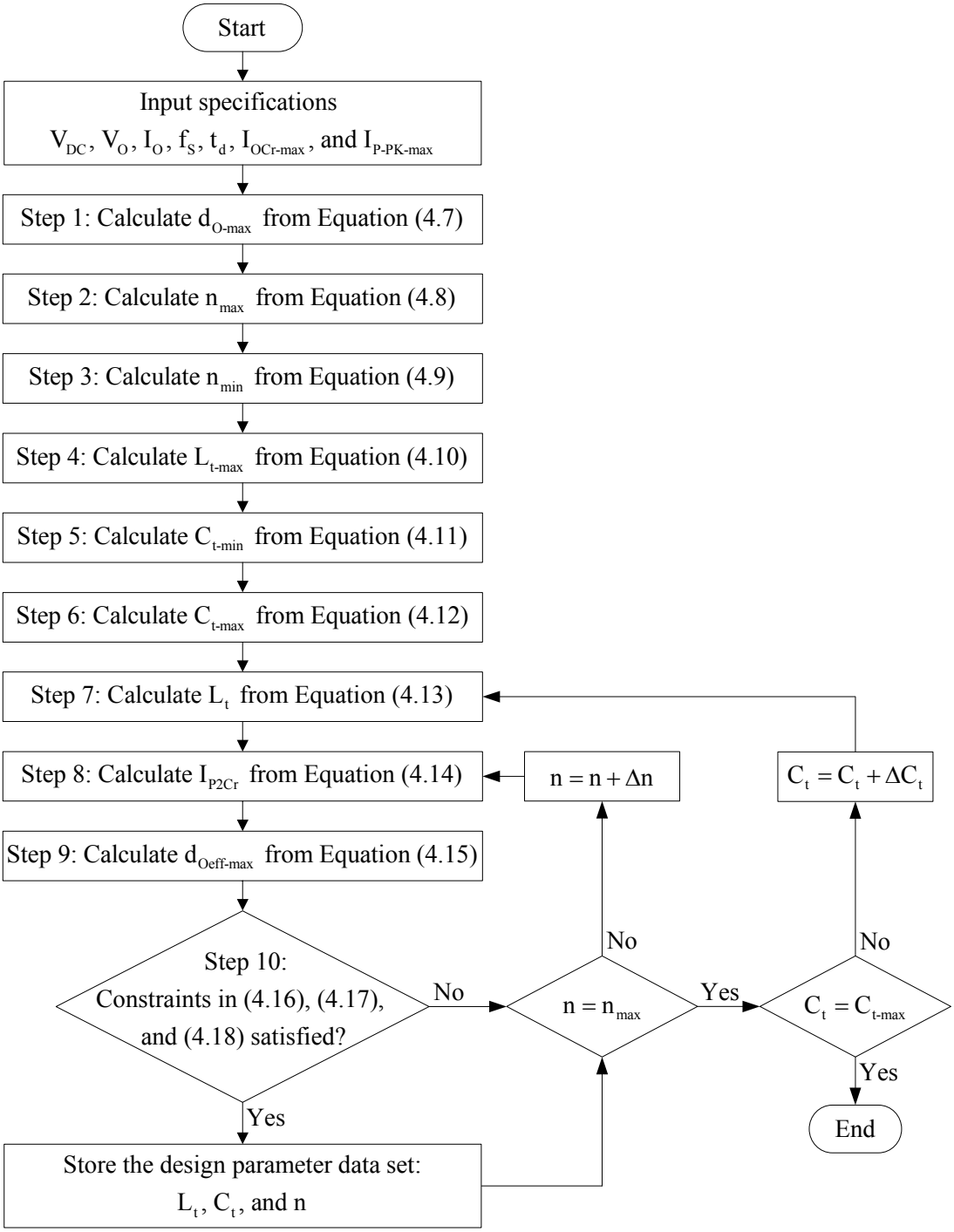


Figure 4.3 The flowchart of the exhaustive search method based design procedure of the FB-PS-ZVS DC/DC converter considering the dead-time constraint.

4.5 Determination of The 5 kW FB-PS-ZVS DC/DC Converter Design Parameters by Utilizing The Exhaustive Search Method

In this section, the design parameter sets obtained by means of the exhaustive search method based design procedure are evaluated and the most feasible design parameter set is determined through an analytical performance estimation process. With the transformer turns ratio specified in the selected parameter set, the design of the high frequency transformer is carried out in section 4.6. Then, utilizing the leakage inductance of the designed transformer, the required additional inductor value is obtained and all the design parameters of the converter system are determined.

The analytical performance evaluation of the FB-PS-ZVS DC/DC converter is carried out for each design parameter set, which are calculated by utilizing the input specifications listed in Table 4.1. Resulting from the specifications given in Table 4.1, 81 design parameter sets are obtained from the utilized design procedure which is implemented via MATLAB, a numerical computing program [11]. The related MATLAB code is given in Appendix A. Since most of the design parameter sets involve numerical values close to each other, 29 of them, that are significantly different from each other, are listed in Table 4.2 after eliminating the similar sets. Given the parameter sets, the approximate values of the maximum output critical current and maximum primary peak output current are obtained from the secondary referred value of the calculated I_{P2Cr} in equation (4.14) and the primary referred value of I_O, respectively. In Table 4.2, the values of these currents are listed for each corresponding design parameter set. Also the equations required to calculate the accurate values of these currents are derived and the corresponding results are listed in the following sections. The additional columns in Table 4.2 show the degree of closeness of the resulting $I_{OCr\text{-}max}$ and $I_{P\text{-}PK\text{-}max}$ values compared to the chosen critical values of 35 A and 28 A, respectively.

Table 4.1 The input specifications of the FB-PS-ZVS DC/DC converter

Input voltage (V_{DC})	400 V
Output voltage (V_O)	55 V
Output current (I_O)	100 A
Switching frequency (f_S)	50 kHz
Dead-time (t_d)	0.9 μsec
Maximum output critical current ($I_{OCr\text{-}max}$)	35 A
Maximum primary peak current ($I_{P\text{-}PK\text{-}max}$)	28 A

The listed design parameter sets in Table 4.2 are further evaluated by considering the analytical performance results at the ZVS boundary and rated load. Also the total power loss and the resulting efficiency of the DC/DC converter are calculated for each data set. Finally, the most favorable data set is selected as a final design parameter set due to its superior overall performance.

Table 4.2 The design parameter sets obtained from the exhaustive search method based design procedure and their maximum output critical and primary peak current values

	Design parameters				
	L_t (μH)	**C_t (nF)**	**n (turns)**	**$I_{OCr\text{-}max}$ (A)**	**$I_{P\text{-}PK\text{-}max}$ (A)**
1	29.43	11.16	3.59	27.99	27.82
2	29.43	11.16	3.79	29.49	26.41
3	28.75	11.42	3.59	28.65	27.82
4	28.75	11.42	3.79	30.18	26.41
5	**28.75**	**11.42**	**3.98**	**31.71**	**25.14**
6	28.10	11.68	3.59	29.32	27.82
7	28.10	11.68	3.79	30.88	26.41
8	28.10	11.68	3.98	32.45	25.14
9	28.10	11.68	4.12	33.62	24.26
10	27.48	11.95	3.59	29.98	27.82
11	27.48	11.95	3.79	31.58	26.41
12	27.48	11.95	3.98	33.18	25.14
13	27.48	11.95	4.17	34.78	23.98
14	26.88	12.21	3.59	30.64	27.82
15	26.88	12.21	3.79	32.28	26.41
16	26.88	12.21	3.98	33.91	25.14
17	26.88	12.21	4.07	34.73	24.55
18	26.31	12.48	3.59	31.30	27.82
19	26.31	12.48	3.79	32.98	26.41
20	26.31	12.48	3.98	34.65	25.14
21	25.77	12.74	3.59	31.97	27.82
22	25.77	12.74	3.74	33.25	26.75
23	25.77	12.74	3.93	34.96	25.44
24	25.25	13.00	3.59	32.63	27.82
25	25.25	13.00	3.83	34.81	26.08
26	24.74	13.27	3.59	33.29	27.82
27	24.74	13.27	3.74	34.63	26.75
28	24.26	13.53	3.64	34.41	27.46
29	23.80	13.80	3.59	34.62	27.82

4.5.1 The DC/DC Converter Performance Results at The ZVS Boundary

In this part, the obtained design parameter sets from the exhaustive search based design procedure, are evaluated by utilizing the analytical performance evaluation results at the ZVS boundary. Utilizing the obtained I_{P2Cr} value, the expressions for I_O, d_O, and d_{Oeff} at the ZVS boundary are derived and their calculated values are listed.

First, the average output current at the ZVS boundary (I_{OCr}) is calculated by utilizing the corresponding I_{P2Cr} value for each design parameter set. However, to calculate I_{OCr}, the output inductor value must be defined initially. Determining a desired peak to peak output current ripple value (ΔI_O) at the rated load current, L_O can be calculated by using (4.19) where $d_{Oeff\text{-}max}$ is obtained from (4.15). Equation (4.19) is derived from the output current waveform (given in Figure 3.18) in mode 0 (or mode 5).

$$L_O = \frac{V_{DC}/n - V_O}{\Delta I_O} \cdot d_{Oeff\text{-}max} \cdot \frac{T_S}{2} \tag{4.19}$$

After determining L_O, the output current ripple at the ZVS boundary ($\Delta I_{O\text{-}ZVS}$) is calculated similarly as in (4.19) and given in (4.20). In this equation, V_{OCr} is the average output voltage at the ZVS boundary, and $d_{Oeff\text{-}ZVS}$ is the d_{Oeff} value at the ZVS boundary.

$$\Delta I_{O\text{-}ZVS} = \frac{V_{DC}/n - V_{OCr}}{L_O} \cdot d_{Oeff\text{-}ZVS} \cdot \frac{T_S}{2} \tag{4.20}$$

I_{OCr} is obtained as in (4.21) by utilizing (3.9), where $d_{O\text{-}ZVS}$ is the d_O value at the ZVS boundary.

$$I_{OCr} = n \cdot I_{P2Cr} - \frac{\Delta I_{O\text{-}ZVS}}{2} + \frac{V_{OCr}}{L_O} \cdot \left(1 - d_{O\text{-}ZVS}\right) \cdot \frac{T_S}{2} \tag{4.21}$$

A second order equation for I_{OCr} is obtained with the assistance of the following three equations, which are defined at the ZVS boundary. Equations (4.22) and (4.23) are obtained from (3.17) and (3.10), respectively.

$$d_{O\text{-}ZVS} = d_{Oeff\text{-}ZVS} \cdot \left(1 + \frac{4 \cdot L_t}{n^2 \cdot R_O \cdot T_S} \right) \tag{4.22}$$

$$d_{Oeff\text{-}ZVS} = \frac{V_{OCr}}{V_{DC}} \cdot n \tag{4.23}$$

$$V_{OCr} = R_O \cdot I_{OCr} \tag{4.24}$$

After solving the resulting equation given in (4.25) and selecting the valid I_{OCr} value from the obtained two solutions, $d_{Oeff\text{-}ZVS}$ and $d_{O\text{-}ZVS}$ values are also calculated and these results at the ZVS boundary are listed in Table 4.3.

$$I_{OCr}{}^2 + \frac{n \cdot V_{DC} \cdot \left(4 \cdot L_O - R_O \cdot T_S\right)}{R_O \cdot \left(n^2 \cdot R_O \cdot T_S + 8 \cdot L_t\right)} \cdot I_{OCr} - \frac{4 \cdot n^2 \cdot V_{DC} \cdot L_O \cdot I_{P2Cr}}{R_O \cdot \left(n^2 \cdot R_O \cdot T_S + 8 \cdot L_t\right)} = 0 \tag{4.25}$$

4.5.2 The DC/DC Converter Performance Results at The Rated Load Current

In this part, the design parameter sets are evaluated by utilizing their analytical performance results at the rated load current. Selecting d_O the same as $d_{O\text{-}max}$, d_{Oeff} is calculated by using (4.15). Then, ΔI_O at the rated load current is calculated similarly as in (4.20) by utilizing the rated values of V_O and d_{Oeff}. Using ΔI_O value, the maximum primary peak current ($I_{P\text{-}PK\text{-}max}$) is calculated as given in (4.26). The obtained results and the transformer secondary peak voltage ($V_{S\text{-}PK}$) at the rated load current are listed in Table 4.4.

Table 4.3 The converter performance result sets at the ZVS boundary

	I_{P2Cr} (A)	I_{OCr} (A)	$d_{Oeff\text{-}ZVS}$	$d_{O\text{-}ZVS}$
1	7.79	28.32	0.14	0.26
2	7.79	29.84	0.16	0.27
3	7.97	29.00	0.14	0.26
4	7.97	30.55	0.16	0.27
5	**7.97**	**32.09**	**0.18**	**0.29**
6	8.16	29.67	0.15	0.26
7	8.16	31.25	0.16	0.28
8	8.16	32.84	0.18	0.30
9	8.16	34.02	0.19	0.31
10	8.34	30.34	0.15	0.27
11	8.34	31.96	0.17	0.28
12	8.34	33.58	0.18	0.30
13	8.34	35.20	0.20	0.32
14	8.53	31.01	0.15	0.27
15	8.53	32.67	0.17	0.29
16	8.53	34.32	0.19	0.30
17	8.53	35.15	0.20	0.31
18	8.71	31.68	0.16	0.27
19	8.71	33.37	0.17	0.29
20	8.71	35.06	0.19	0.31
21	8.89	32.35	0.16	0.28
22	8.89	33.65	0.17	0.29
23	8.89	35.37	0.19	0.31
24	9.08	33.02	0.16	0.28
25	9.08	35.23	0.19	0.30
26	9.26	33.70	0.17	0.28
27	9.26	35.04	0.18	0.30
28	9.45	34.82	0.17	0.29
29	9.63	35.04	0.17	0.29

$$I_{P\text{-}PK\text{-}max} = \frac{1}{n} \cdot \left(I_O + \frac{\Delta I_O}{2} \right) \tag{4.26}$$

Table 4.4 The converter performance result sets at the rated load current

	d_O	d_{Oeff}	ΔI_O (A)	$I_{P\text{-}PK\text{-}max}$ (A)	$V_{S\text{-}PK}$ (V)
1	0.91	0.50	1.88	28.09	111.29
2	0.91	0.52	1.74	26.64	105.65
3	0.91	0.50	1.90	28.09	111.29
4	0.91	0.53	1.75	26.64	105.65
5	**0.91**	**0.55**	**1.60**	**25.34**	**100.55**
6	0.91	0.51	1.92	28.09	111.29
7	0.91	0.53	1.77	26.65	105.65
8	0.91	0.55	1.62	25.34	100.55
9	0.91	0.57	1.50	24.44	97.04
10	0.91	0.51	1.94	28.09	111.29
11	0.91	0.54	1.79	26.65	105.65
12	0.91	0.56	1.63	25.34	100.55
13	0.91	0.58	1.48	24.16	95.92
14	0.91	0.52	1.96	28.10	111.29
15	0.91	0.54	1.80	26.65	105.65
16	0.91	0.56	1.64	25.34	100.55
17	0.91	0.57	1.57	24.74	98.18
18	0.91	0.52	1.98	28.10	111.29
19	0.91	0.55	1.82	26.65	105.65
20	0.91	0.57	1.66	25.35	100.55
21	0.91	0.53	2.00	28.10	111.29
22	0.91	0.54	1.87	27.00	107.00
23	0.91	0.57	1.71	25.66	101.78
24	0.91	0.53	2.01	28.10	111.29
25	0.91	0.56	1.81	26.32	104.32
26	0.91	0.54	2.03	28.11	111.29
27	0.91	0.55	1.90	27.01	107.00
28	0.91	0.55	2.00	27.73	109.82
29	0.91	0.54	2.06	28.11	111.29

4.5.3 The DC/DC Converter Efficiency Performance Results

In addition to the above analytical performance evaluation at the ZVS boundary and rated load current, the power loss and efficiency calculation of the converter system is utilized for the overall performance evaluation while comparing the design parameter sets obtained from the exhaustive search method based design procedure.

While calculating the power losses in the full-bridge inverter, since the leading leg switches satisfy the ZVS condition even with small primary current values, their switching loss is assumed to be zero for the whole load current range. However, the lagging leg switches satisfy the ZVS condition only when the primary current is above a significant value, which is defined as the critical current (I_{P2Cr}). Therefore, when the primary current value is above the critical current, zero switching loss is assumed in the full-bridge inverter. As a result, under soft switching operating conditions, the power loss in the full-bridge inverter consists of only the conduction losses of the switches. However, when the primary current is below I_{P2Cr} value, the lagging leg switches turn on with a significant voltage (V_{Tf}) on them. As shown in Figure 4.4, the switch voltage decrease from V_{DC} is ΔV_T, which is proportional to I_{P2} (the primary current at the beginning of mode 3). ΔV_T and the resulting V_{Tf} expressions are given in (4.27) and (4.28), respectively.

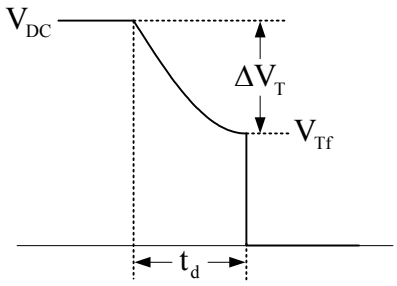


Figure 4.4 The switch voltage waveform during hard-switching.

$$\Delta V_T = \sqrt{\frac{L_t}{C_t}} \cdot I_{P2} \tag{4.27}$$

$$V_{Tf} = V_{DC} - \Delta V_T \tag{4.28}$$

The power loss due to hard-switching operation is obtained from the remaining energy stored in the total resonant capacitance after the the primary current decreases to zero while I_{P2} is smaller than I_{P2Cr}. The power loss due to hard-switching of the lagging leg switches (P_{Lhs}), which results from the discharging of C_t across the switch from V_{Tf} to 0 after the turn-on of the switch, is given in (4.29).

$$P_{Lhs} = f_S \cdot C_t \cdot V_{Tf}^{\ 2} \tag{4.29}$$

P_{Lhs} for each design parameter set is calculated and listed in Table 4.5 for four different values of I_{P2}. These I_{P2} values, which are 20%, 40%, 60%, and 80% of I_{P2Cr}, result in the V_{Tf} values of 320 V, 240 V, 160 V, and 80 V, respectively.

The efficiency of the DC/DC converter can be obtained after calculating the power loss in the main DC/DC converter blocks, which are the full-bridge inverter, the transformer, and the full-bridge rectifier. Since zero switching loss is assumed in the full-bridge inverter, only the conduction losses of the switches and their freewheeling diodes are taken into account while calculating the power loss in the inverter ideally. The conduction loss expressions for the switches and freewheeling diodes are given in (4.30) and (4.31), respectively. In (4.30) P_T is the conduction power loss of the utilized switch (IGBT), V_{CEsat} is the on-state voltage drop of the IGBT, and I_C is the current flowing through the IGBT. In (4.31) P_{FWD} is the conduction power loss of a freewheeling diode of an IGBT, V_{FWD} is the on-state voltage drop of the each freewheeling diode, and I_D is the current flowing through this diode.

$$P_T = V_{CEsat} \cdot f_S \cdot \int I_C(t)dt \tag{4.30}$$

$$P_{FWD} = V_{FWD} \cdot f_S \cdot \int I_D(t)dt \tag{4.31}$$

Table 4.5 The converter performance result sets considering the switching loss (P_{Lhs}) in the full-bridge inverter under the hard-switching condition

	P_{Lhs} (W)			
	I_{P2} = 20% I_{P2Cr}	**I_{P2} = 40% I_{P2Cr}**	**I_{P2} = 60% I_{P2Cr}**	**I_{P2} = 80% I_{P2Cr}**
1	57.11	32.13	14.28	3.57
2	57.11	32.13	14.28	3.57
3	57.11	32.13	14.28	3.57
4	58.46	32.89	14.62	3.65
5	**58.46**	**32.89**	**14.62**	**3.65**
6	59.82	33.65	14.95	3.74
7	59.82	33.65	14.95	3.74
8	59.82	33.65	14.95	3.74
9	59.82	33.65	14.95	3.74
10	61.17	34.41	15.29	3.82
11	61.17	34.41	15.29	3.82
12	61.17	34.41	15.29	3.82
13	61.17	34.41	15.29	3.82
14	62.52	35.17	15.63	3.91
15	62.52	35.17	15.63	3.91
16	62.52	35.17	15.63	3.91
17	62.52	35.17	15.63	3.91
18	63.87	35.93	15.97	3.99
19	63.87	35.93	15.97	3.99
20	63.87	35.93	15.97	3.99
21	65.23	36.69	16.31	4.08
22	65.23	36.69	16.31	4.08
23	65.23	36.69	16.31	4.08
24	66.58	37.45	16.65	4.16
25	66.58	37.45	16.65	4.16
26	67.93	38.21	16.98	4.25
27	67.93	38.21	16.98	4.25
28	69.28	38.97	17.32	4.33
29	70.64	39.73	17.66	4.41

Since the current flowing through the leading and lagging leg switches and their freewheeling diodes are not similar as shown in Figure 4.5, P_T and P_{FWD} expressions for the leading and the lagging leg devices will be different. The switch power loss equations for T_1 (or T_4) and T_2 (or T_3) are given in (4.32) and (4.33), respectively. For the freewheeling diodes, the power loss equations are given in (4.34) and (4.35) for D_1 (or D_4) and D_2 (or D_3), respectively. The resulting total power loss in the full-bridge inverter is given in (4.36).

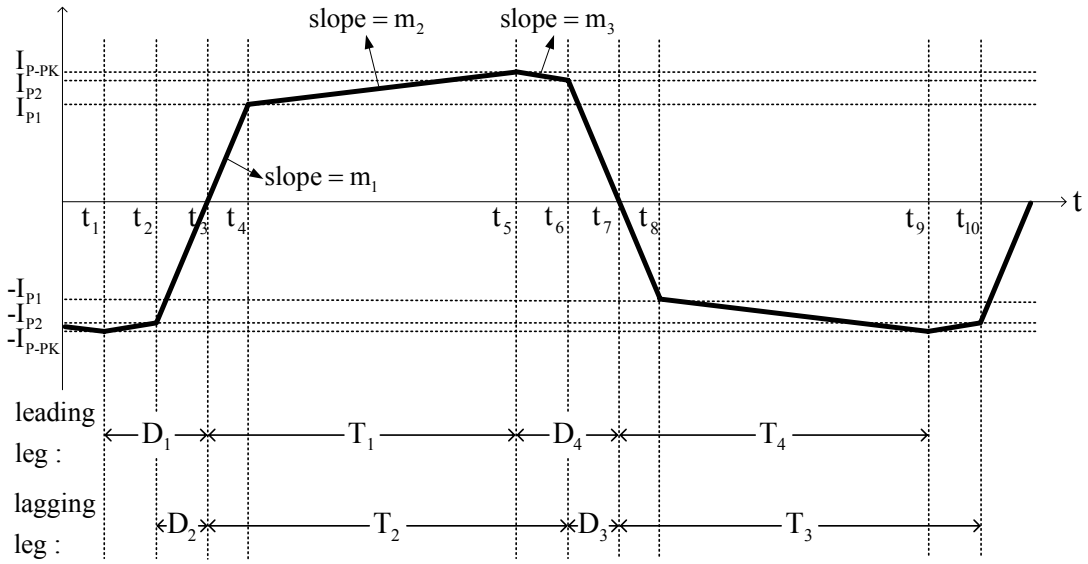


Figure 4.5 The primary current waveform indicating the conducting switches and freewheeling diodes in the corresponding time intervals.

$$P_{T1,4} = V_{CEsat} \cdot \left[\frac{m_1 \cdot f_S}{2} \cdot \left(\frac{I_{P1} + I_{P2}}{2 \cdot m_1} - \frac{d_O - d_{Oeff}}{4 \cdot f_S} \right)^2 + \frac{I_{P1} \cdot d_{Oeff}}{2} + \frac{m_2 \cdot {d_{Oeff}}^2}{8 \cdot f_S} \right] \tag{4.32}$$

$$P_{T2,3} = V_{CEsat} \cdot \left[\frac{m_1 \cdot f_S}{2} \cdot \left(\frac{I_{P1} + I_{P2}}{2 \cdot m_1} - \frac{d_O - d_{Oeff}}{4 \cdot f_S} \right)^2 + \frac{I_{P1} \cdot d_{Oeff}}{2} + \frac{m_2 \cdot {d_{Oeff}}^2}{8 \cdot f_S} + \frac{I_{P2} \cdot (1 - d_O)}{2} + \frac{m_3 \cdot (1 - d_O)^2}{8 \cdot f_S} \right] \tag{4.33}$$

$$P_{D1,4} = V_{FWD} \cdot \left[\frac{I_{P2} \cdot (1 - d_O)}{2} + \frac{m_3 \cdot (1 - d_O)^2}{8 \cdot f_S} + \frac{m_1 \cdot f_S}{2} \cdot \left(\frac{I_{P1} + I_{P2}}{2 \cdot m_1} + \frac{d_O - d_{Oeff}}{4 \cdot f_S} \right)^2 \right] \quad (4.34)$$

$$P_{D2,3} = V_{FWD} \cdot \left[\frac{m_1 \cdot f_S}{2} \cdot \left(\frac{I_{P1} + I_{P2}}{2 \cdot m_1} + \frac{d_O - d_{Oeff}}{4 \cdot f_S} \right)^2 \right] \quad (4.35)$$

$$P_{inv} = 2 \cdot \left(P_{T1,4} + P_{T2,3} + P_{D1,4} + P_{D2,3} \right) \quad (4.36)$$

In the above equations the slopes of the sections of the primary current waveform are presented in three parts which can be observed in Figure 4.5. These slopes are m_1 between t_2 and t_4, m_2 between t_4 and t_5, and m_3 between t_5 and t_6. In the equations (4.37), (4.38), and (4.39) the slopes m_1, m_2, and m_3 are given respectively.

$$m_1 = \frac{V_{DC}}{L_t} \quad (4.37)$$

$$m_2 = \frac{V_{DC} - V_O'}{L_O'} \quad (4.38)$$

$$m_3 = \frac{V_O'}{L_O'} \quad (4.39)$$

The total power loss in the transformer consists of the core loss and mainly the winding loss. The core loss (P_C) can be obtained from the magnetic core manufacturer's material datasheet after specifying the maximum operating flux density (B_m) at the operating frequency (f_S). The winding loss can be given simply as in (4.40) where I_{Prms} is the rms value of the primary current and $R_1 + R_2'$ is the primary referred equivalent winding resistance.

$$P_W = \left(R_1 + R_2' \right) \cdot {I_{Prms}}^2 \quad (4.40)$$

From the primary current waveform shown in Figure 4.5, I_{Prms} is obtained by utilizing the slope expressions, and the resulting P_W is given in (4.41). Finally, the total power loss in the transformer is given in (4.42).

$$P_W = \left(R_1 + R_2'\right)\cdot\left[\frac{m_1^{\,2}\cdot(d_O - d_{Oeff})^3}{12\cdot f_S^{\,2}} - \frac{m_1\cdot I_{P2}\cdot(d_O - d_{Oeff})^2}{2\cdot f_S} + I_{P2}^{\,2}\cdot(d_O - d_{Oeff})\right.$$
$$+\frac{m_2^{\,2}\cdot d_{Oeff}^{\,3}}{12\cdot f_S^{\,2}} + \frac{m_2\cdot I_{P1}\cdot d_{Oeff}^{\,2}}{2\cdot f_S} + I_{P1}^{\,2}\cdot d_{Oeff} + \frac{m_3^{\,2}\cdot(1-d_O)^3}{12\cdot f_S^{\,2}} \qquad (4.41)$$
$$\left.+\frac{m_3\cdot I_{P2}\cdot(1-d_O)^2}{2\cdot f_S} + I_{P2}^{\,2}\cdot(1-d_O)\right]$$

$$P_{xfmr} = P_C + P_W \qquad (4.42)$$

Finally, the total conduction power loss in the full-bridge rectifier is given in (4.43) where V_{RD} is the forward voltage drop of each rectifier diode. As can be observed in Figure 4.6, the average current of each diode in the rectifier is $I_O/2$.

$$P_{rect} = 4\cdot\left(V_{RD}\cdot\frac{I_O}{2}\right) \qquad (4.43)$$

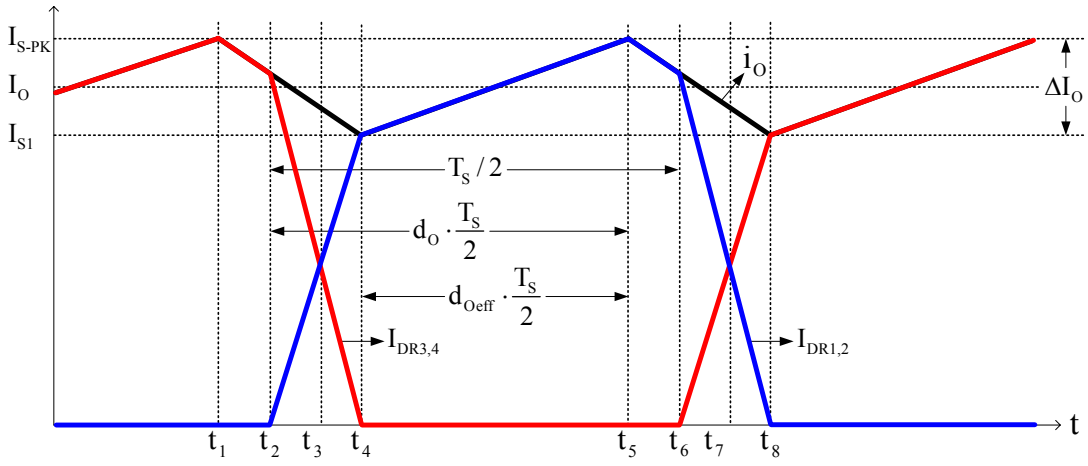


Figure 4.6 The rectifier diode and load current waveforms.

Thus, the power loss equations for the main blocks of the DC/DC converter are obtained. The total power loss of the converter and the resulting percentage efficiency of the converter (η_c) are given in (4.44) and (4.45), respectively. Utilizing the obtained design parameters, and the given specifications of the converter circuit components in Table 4.6, the power losses and efficiency of each solution set are listed in Table 4.7.

$$P_{total} = P_{inv} + P_{xfmr} + P_{rect} \tag{4.44}$$

$$\eta_c = \frac{V_O \cdot I_O}{V_O \cdot I_O + P_{total}} \cdot 100 \tag{4.45}$$

Table 4.6 The specifications of the converter circuit components utilized in the efficiency calculation

Inverter		**Transformer**		**Rectifier**	
V_{CEsat}	3.3 V	B_m	0.15 T	V_{RD}	0.85 V
V_{FWD}	2 V	P_C	15 W		
		$R_1 + R_2'$	0.2 Ω		

With all the detailed performance calculations completed, in order to finalize the design, a convenient design parameter set must be selected among these 29 possible sets. At this point, the efficiency and practical implementation issues of the converter components are the determining factors in selecting the convenient set. In this thesis, the design parameter set in the fifth row of Table 4.2 is selected as the final design parameter set, since its efficiency is high, its switching loss at the hard switching case is low, and its C_t value is satisfied with a 4.7 nF capacitor for each lagging leg switch, which is an available capacitor value in the market.

Having determined the transformer turns ratio as four, the design and implementation of the high frequency transformer is given in the next section.

Table 4.7 The converter efficiency performance result sets

	P_{inv} (W)	P_{xfmr} (W)	P_{rect} (W)	P_{total} (W)	η_c (%)
1	150.70	128.02	170.00	448.73	92.46
2	144.67	118.79	170.00	433.46	92.69
3	151.10	129.03	170.00	450.14	92.43
4	145.04	119.64	170.00	434.68	92.68
5	**139.47**	**111.33**	**170.00**	**420.80**	**92.89**
6	151.49	130.03	170.00	451.52	92.41
7	145.40	120.47	170.00	435.88	92.66
8	139.81	112.03	170.00	421.83	92.88
9	135.89	106.33	170.00	412.22	93.03
10	151.88	131.00	170.00	452.88	92.39
11	145.76	121.29	170.00	437.05	92.64
12	140.13	112.71	170.00	422.85	92.86
13	134.94	105.12	170.00	410.06	93.06
14	152.26	131.96	170.00	454.22	92.37
15	146.11	122.08	170.00	438.20	92.62
16	140.46	113.38	170.00	423.84	92.85
17	137.79	109.42	170.00	417.21	92.95
18	152.64	132.89	170.00	455.53	92.35
19	146.46	122.86	170.00	439.32	92.60
20	140.77	114.03	170.00	424.81	92.83
21	153.01	133.81	170.00	456.82	92.33
22	148.30	126.05	170.00	444.35	92.52
23	142.47	116.80	170.00	429.27	92.76
24	153.38	134.70	170.00	458.08	92.31
25	145.65	121.98	170.00	437.64	92.63
26	153.74	135.58	170.00	459.32	92.29
27	148.98	127.58	170.00	446.57	92.49
28	152.47	133.64	170.00	456.11	92.34
29	154.45	137.28	170.00	461.72	92.26

4.6 Design of The High Frequency Transformer Utilized in The FB-PS-ZVS DC/DC Converter

4.6.1 High Frequency Transformer Design Considerations

The high frequency isolation transformer utilized in the DC/DC converter is designed by using the electrical specifications given in Table 4.8.

Table 4.8 Electrical specifications of the high frequency isolation transformer

Output power (P_O)	5.5 kW
Primary peak voltage ($V_{1\text{-}PK}$)	400 V
Secondary rms current (I_2)	100 A
Primary to secondary winding turns ratio (n)	4
Operating frequency (f)	50 kHz

The preferred magnetic core material type for the high frequency isolation transformer is ferrite due to its superior performance over other type of magnetic materials at the operating frequency given in Table 4.8.

The transformer core size is determined by utilizing the area product formula, which is also related to the power handling capacity of the transformer [12]. This formula is formed by the product of the core cross section area (A_C) and the core window area (A_{CW}). The area product formula derivation starts with Faraday's Law, which is given in (4.46) for squarewave voltage waveform.

$$V_{1\text{-}PK} = 4 \cdot B_m \cdot A_C \cdot N_1 \cdot f \cdot 10^{-4} \tag{4.46}$$

In (4.46) $V_{1\text{-}PK}$ is the primary peak voltage, B_m (in Tesla) is the maximum induced flux density in the core and N_1 is the primary winding turns number. A_C in equation (4.46) is given in cm^2. The utilization factor of the core window area (K_U) is given in (4.47).

$$K_U = \frac{N_1 \cdot A_w}{A_{CW}} \tag{4.47}$$

A_w is the cross section area of the conductor (may be wire or foil), which is utilized in the primary winding of N_1 turns. From (4.46) and (4.47) the area product expression is obtained as given in (4.48).

$$A_C \cdot A_{CW} = \frac{V_{1\text{-}PK} \cdot A_w \cdot 10^4}{4 \cdot B_m \cdot f \cdot K_U} \tag{4.48}$$

If the conductor cross section area is expressed as the ratio of the flowing current in the conductor to the current density (J) of the conductor, and the input power is expressed as the ratio of the output power to the transformer efficiency (η_t), the area product expression is obtained as given in (4.49).

$$A_C \cdot A_{CW} = \frac{P_O \cdot 10^4}{4 \cdot \eta_t \cdot J \cdot B_m \cdot f \cdot K_U} \tag{4.49}$$

Utilizing P_O and f values given in Table 4.8 and choosing B_m as 0.15 T, J as 250 A/cm^2, η_t as 0.97 and K_U as 0.3, the area product is calculated as 25.2 cm^4 from (4.49). Although one stack of E-65 core transformer meets the desired power handling demand (since it has an area product of 28 cm^4), a double stack transformer that consists of 4 pieces of E-65 core is employed in the implemented transformer since the total windings and winding losses are halved and in this case the placing of the windings in the core window is carried out easily. The dimensional properties of this core type are given in Table 4.9 [13].

Table 4.9 Dimensional properties of the E-65 core

Effective magnetic path length (l_e)	14.7 cm
Effective core cross sectional area (A_C)	5.3 cm^2
Effective volume (V_e)	79 cm^3
Area product ($A_C.A_{CW}$)	28 cm^4

After considering the core type, material and size; the windings of the transformer can be designed. First, the number of turns of the transformer primary is calculated by using (4.50), which origins from the Faraday's Law.

$$N_1 = \frac{V_{1\text{-PK}} \cdot d_{O\text{-max}} \cdot 10^4}{4 \cdot B_m \cdot A_C \cdot f} \tag{4.50}$$

In (4.50) $d_{O\text{-max}}$ is the maximum on time ratio of the voltage applied to the transformer primary. Selecting $d_{O\text{-max}}$ as 0.91 and B_m as 0.15 T, the transformer primary winding turns number is calculated as 12.

Since the high frequency AC voltage formed at the transformer secondary winding is rectified by utilizing a full-bridge diode rectifier, only one secondary winding is utilized in the transformer. As determined in the previous section, the transformer primary to secondary turns ratio is obtained as 4, which results in 3 turns of secondary winding.

While considering the conductor types and sizes of the transformer windings, skin effect must be taken into account due to the operation at high frequency [12]. Although the current distribution in the conductor at low frequencies is uniform, the current mostly flows through the surface of the same conductor at high frequencies. The reduction of the current density through the center of the conductor is the result of skin effect. Therefore, the thickness or the diameter of the conductors must be selected by taking into account this condition. The skin depth in mm, which is defined as the distance from the conductor surface where the current decreases to its 1/e of its value at the conductor surface, is given in (4.51) for copper. Thus, the diameter of wire or the thickness of foil conductors must be smaller than twice the skin depth for better utilization of the conductors and also the transformer core window area.

$$\delta_S = \frac{66.2}{\sqrt{f}} \tag{4.51}$$

At 50 kHz, the skin depth for copper is 0.29 mm and the selected conductor sizes are 0.15 mm thickness foil with 40 mm width for the primary winding, and a 0.5 mm thickness foil with 40 mm width for the secondary winding. The DC resistances of these windings are calculated by using the conventional resistance calculation formula as given in (4.52).

$$R_{dc} = \rho_{Cu} \frac{MLT}{A_w} \tag{4.52}$$

MLT is the mean length turn of the windings and ρ_{Cu} is the resistivity of the copper which is the utilized material type in the conductors. R_{dc} values for the primary and secondary windings are calculated as 8.64 mΩ and 0.65 mΩ, respectively. Due to the skin and proximity effects, the equivalent AC resistance values of the windings increase with the frequency. Due to this reason, they are obtained by utilizing the short-circuit test results and the DC resistance ratio of the windings.

Another point in the transformer design is the magnetizing inductance of the transformer. To lower the magnetizing inductance by inserting a small length of air gap between the E cores of the transformer results in two practical advantages. First, it lowers the ZVS range since the continuously flowing current through the magnetizing inductance will increase and the total current flowing through the primary leakage inductance will also increase for the same load current. The other advantage is the saturation DC current of the ferrite core is increased. Due to this reason, an effective air gap of 0.4 mm is introduced in the transformer, from which the magnetizing inductance is calculated as 410 μH.

The windings are placed in the transformer core window in order to reduce the leakage inductance by interleaving the windings as shown in Figure 4.7. In this scheme, 12 turns of primary winding is splitted into two sections of 6 turns and the secondary winding is placed between the primary winding sections. This method also reduces the peak magneto-motive force (mmf) between the primary and secondary winding by half.

The obtained total resonant inductance value from the selected design parameter set (28.75 μH) is large to implement this inductance only utilizing the leakage inductance. Hence, an external inductance is required to obtain the total resonant inductance. To decrease the AC losses due to the proximity effect and increase the coupling between the primary and secondary windings, in the transformer winding design stage the interleaved winding structure is utilized. The interleaved winding structure, however, decreases the available leakage inductance and a larger external inductance becomes necessary for the circuit. There is a compromise between the leakage inductance maximization and maximizing the coupling. In the early development stages the decision was favored towards loss reduction improved coupling and the transformer design was completed. Thereafter, the converter performance optimization studies favored larger external inductance values than those initially presumed. As a result, in the final stage the external inductance was increased to the above value. In a practical converter design, these issues should be carefully considered and in order to reduce the converter size and cost, the transformer should be designed with emphasis on good coupling and sufficiently large leakage inductance. Thus, the interleaving approach may not be required.

So far, the on-paper calculated parameters of the transformer are obtained by utilizing only one dimension that is in radial axis and assuming ideal cases. For more realistic results a magnetic modeler and solver simulation tool, PEmag from ANSOFT is utilized in the transformer design [14]. After the model and the layout of the transformer are formed as shown in Figure 4.7, the equivalent circuit parameters of the transformer are extracted by using PEmag, which is a Finite Element Analysis (FEA) based solver. PEmag generates the model of the transformer by using two dimensional distribution of electric (E) and magnetic (H) fields. These E and H fields consist of two vector components, which are in radial (r) and vertical (z) direction. Maxwell's equations are solved by the FEA solver in these two dimensions. While generating the model all fringing and proximity effects are taken into account.

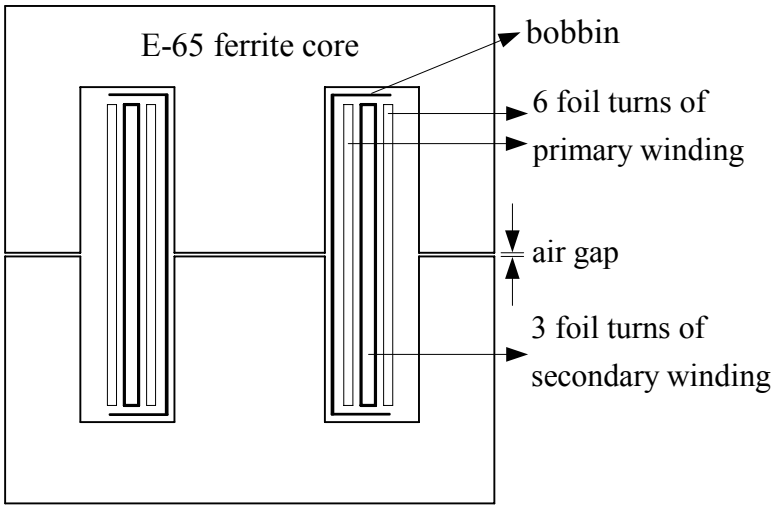


Figure 4.7 The layout of the high frequency transformer.

Based on the illustrated layout of the windings in Figure 4.7, the magnetizing inductance of the high frequency transformer is calculated as 450 μH and the other parameters of the transformer that are calculated by PEmag at DC and the frequency of 50 kHz, are given in Table 4.10. L_{LK}, which is also shown in Figure 4.8, is the total leakage inductance referred to the primary; R_1 and R_2, which are also shown in Figure 4.9 and 4.10, are the primary and the secondary winding resistances.

Table 4.10 FEA model results of the high frequency transformer

	DC	50 kHz
L_{LK}	0.31 μH	0.28 μH
R_1	6.55 mΩ	89.7 mΩ
R_2	0.49 mΩ	4.46 mΩ

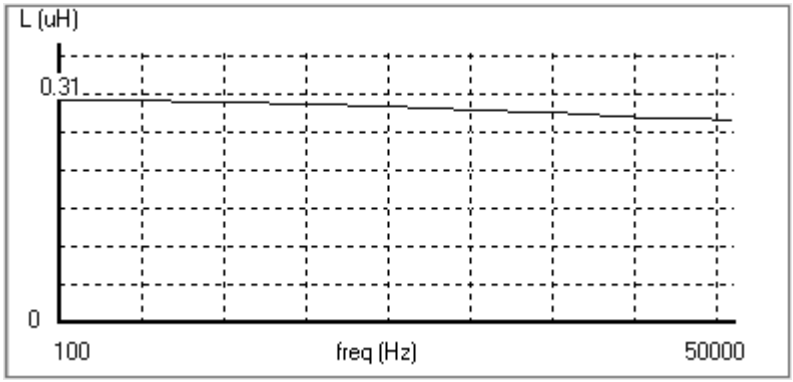


Figure 4.8 The leakage inductance of the transformer obtained by FEA.

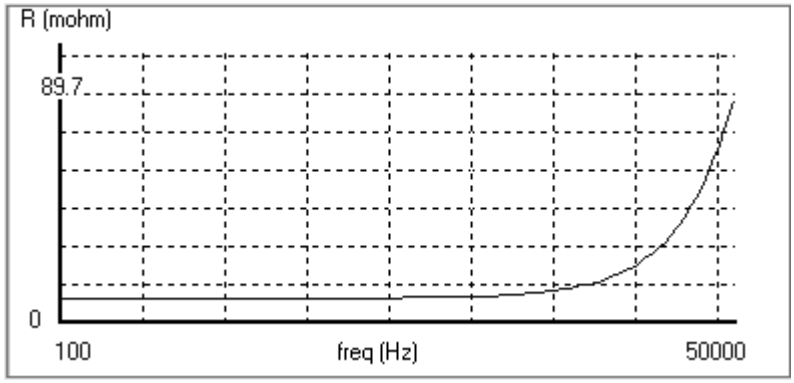


Figure 4.9 The primay winding resistance obtained by FEA.

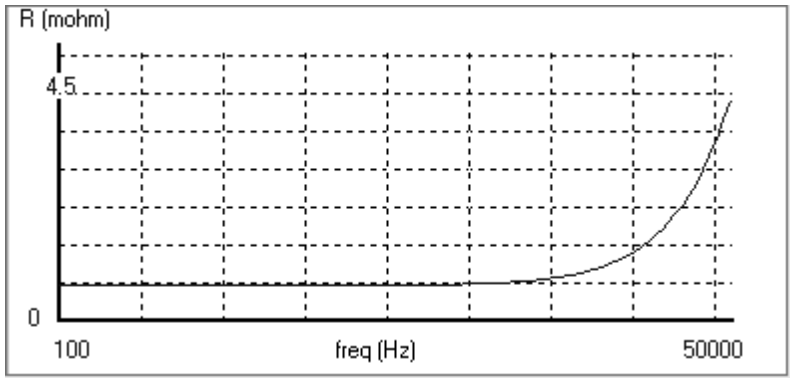


Figure 4.10 The secondary winding resistance obtained by FEA.

4.6.2 Characterization of The Manufactured High Frequency Transformer

The designed high frequency transformer is manufactured by a local magnetic circuit component manufacturer. In Figure 4.11 the photograph of the manufactured high frequency transformer is shown.

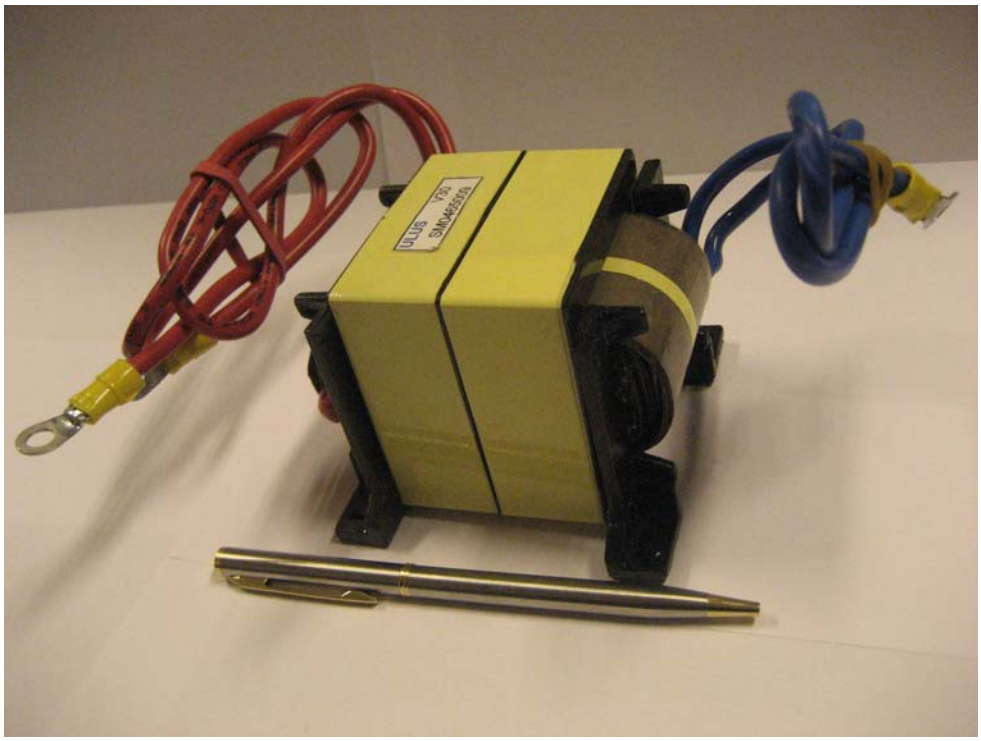


Figure 4.11 Manufactured high frequency transformer.

To obtain the equivalent circuit parameters of the manufactured transformer, short-circuit and open-circuit tests are performed. The transformer T equivalent circuit, which is shown in Figure 4.12, is utilized in order to model the manufactured transformer. In Figure 4.12, L_{LK1} and R_1 represent the leakage inductance and the primary winding resistance, respectively. L_M stands for the magnetizing inductance of the transformer and R_C is utilized for modelling the core losses. L_{LK2}' and R_2' represent the referred values of the leakage inductance and the winding resistance of the secondary winding to the primary side. The primary voltage and current are symbolized as V_1 and I_1, respectively. V_2' and I_2' represent the referred values of the secondary voltage and current to the primary side.

Utilizing short-circuit and open-circuit tests, the equivalent circuit of the high frequency transformer at the operating frequency of 50 kHz is obtained. In both tests a sinusoidal voltage at 50 kHz is applied to the transformer primary by means of a power amplifier, while the secondary side is either short or open circuited.

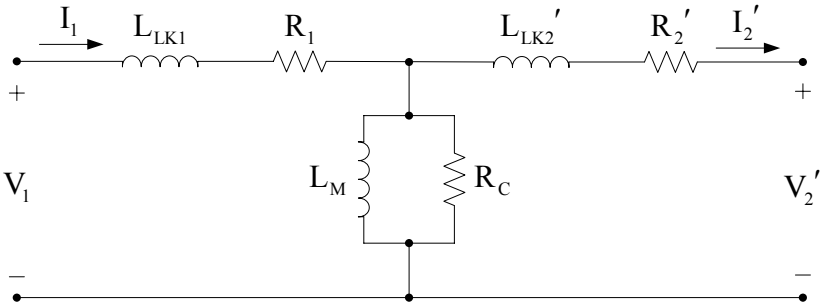


Figure 4.12 Primary referred transformer T equivalent circuit.

4.6.2.1 Short-Circuit Test Results of The High Frequency Transformer

The short-circuit test is carried out by utilizing a signal generator feeding a 50 kHz sinusoidal reference signal to a power amplifier. The power amplifier feeds the transformer primary while the transformer secondary winding is short-circuited. By controlling the magnitude of the signal applied by the signal generator, the transformer primary voltage magnitude is controlled. The results of the short-circuit test including I_1, I_2, and the phase difference between V_1 and I_1 waveforms (ϕ (V_1–I_1)) corresponding to the applied several V_1 values are listed in Table 4.11. For the maximum applied primary voltage, the primary voltage and current, and the secondary current waveforms are shown in Figure 4.13.

Table 4.11 Transformer short-circuit test results for f = 50 kHz

V_1 (V)	**I_1 (A)**	**I_2 (A)**	**ϕ (V_1–I_1)**
2.60	1.36	5.24	84°
5.09	2.62	10.34	84°
6.99	3.62	13.83	84°
9.00	4.66	18.23	84°
10.71	5.47	21.29	84°
11.37	5.96	22.88	84°

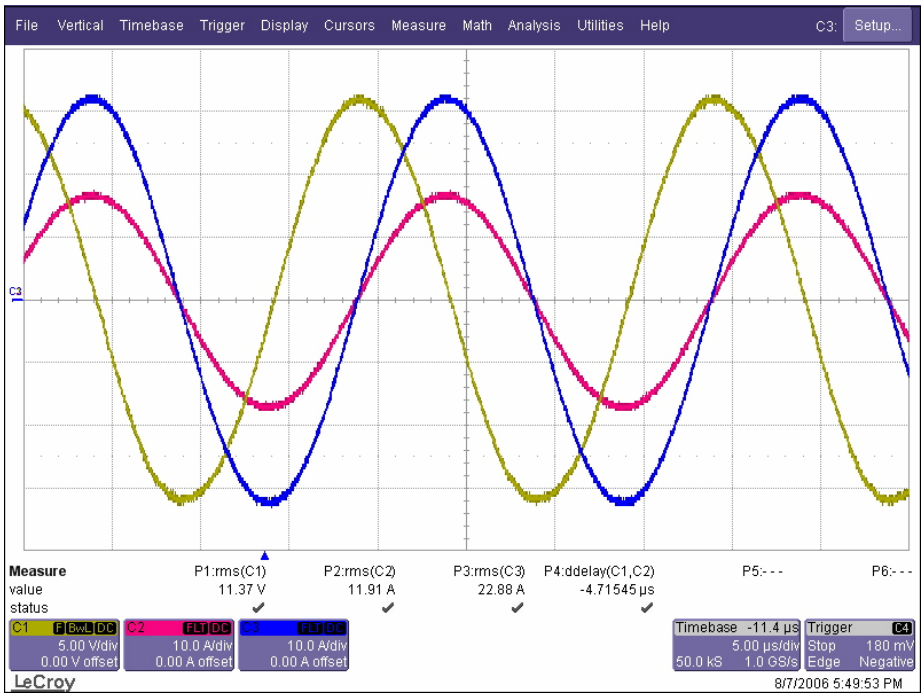


Figure 4.13 The primary voltage (yellow) and current (red), and the secondary current (blue) waveforms obtained from short-circuit test at 50 kHz (scales: 5 V/div, 5 A/div, 10 A/div, 5 µs/div).

The primary and secondary current versus applied primary voltage waveforms are plotted in Figure 4.14. As can be observed in this figure, I_1–V_1 and I_2–V_1 relationships exhibit linear characteristics. The equivalent circuit parameters of L_{LK1}, R_1, L_{LK2}, and R_2 can be calculated by utilizing the obtained results from the short-circuit test. Initially, the short-circuit real power (P_{sc}) is calculated by using (4.53).

$$P_{sc} = V_1 \cdot I_1 \cdot \cos\varphi \tag{4.53}$$

While employing the short-circuit test, the parallel branch including the parameters L_M and R_C in the transformer equivalent circuit can be considered as an open-circuit branch due to its high equivalent impedance. With this assumption, the power dissipated by two resistive circuit components, R_1 and R_2, is given in (4.54).

$$P_{sc} = R_1 \cdot I_1^2 + R_2 \cdot I_2^2 \tag{4.54}$$

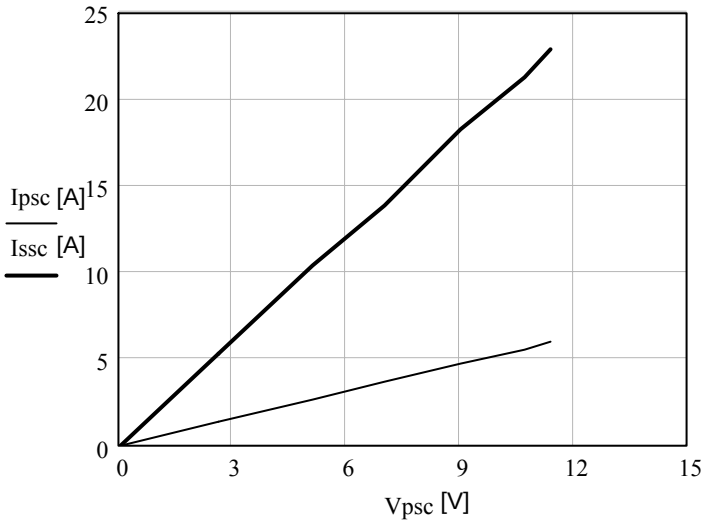


Figure 4.14 The primary current (I_{psc}) and the secondary current (I_{ssc}) versus the primary voltage (V_{psc}) obtained from the short-circuit test.

Finally the values of R_1 and R_2 are specified by using (4.54) and the ratio between them. This ratio can be obtained from the calculated DC resistance values of R_1 and R_2. The calculated DC resistance of R_1 and R_2 are 8.64 mΩ and 0.65 mΩ and the resulting R_1 and R_2 values at 50 kHz are 94.5 mΩ and 7.1 mΩ, respectively.

Similarly, L_{LK1} and L_{LK2} can be calculated by using the short-circuit reactive power (Q_{sc}) expressions given in (4.55) and (4.56).

$$Q_{sc} = V_1 \cdot I_1 \cdot \sin\varphi \tag{4.55}$$

$$Q_{sc} = (\omega \cdot L_{LK1}) \cdot I_1^{\,2} + (\omega \cdot L_{LK2}) \cdot I_2^{\,2} \tag{4.56}$$

Assuming the leakage inductances of the primary and the secondary winding are equal to each other, the resulting primary referred leakage inductance value for the primary and secondary winding is 3.26 μH.

4.6.2.2 Open-Circuit Test Results of The High Frequency Transformer

The open-circuit test is carried out by utilizing the same experimental set-up as in the short-circuit test. However, the secondary of the transformer is left open-circuit in this test. The results of the open-circuit test including I_1, V_2, and $\phi\,(V_1–I_1)$ corresponding to the applied several V_1 values are given in Table 4.12. For the maximum applied primary voltage, the primary voltage and the secondary voltage and current waveforms are shown in Figure 4.15.

Table 4.12 Transformer open-circuit test results for f = 50 kHz

V_1 (V)	I_1 (A)	V_2 (V)	$\phi\,(V_1–I_1)$
12.62	0.098	3.14	89.6°
19.44	0.150	4.79	89.6°
24.14	0.186	6.06	89.6°
29.95	0.226	7.39	89.6°
33.14	0.249	8.17	89.6°
35.84	0.270	8.88	89.6°

The primary current and the secondary voltage versus applied primary voltage waveforms are plotted in Figure 4.16 and 4.17. As can be seen from the figures $I_1–V_1$ and $V_2–V_1$ relationships exhibit linear characteristics.

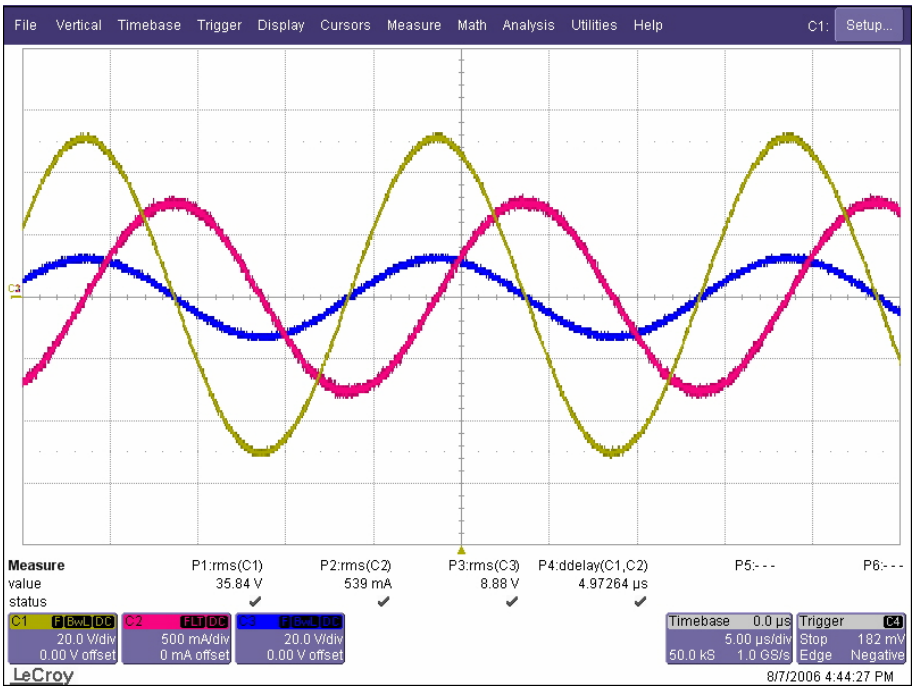


Figure 4.15 The primary voltage (yellow) and current (red), and the secondary voltage (blue) waveforms obtained from open-circuit test at 50 kHz (scales: 20 V/div, 0.25 A/div, 20 V/div, 5 µs/div).

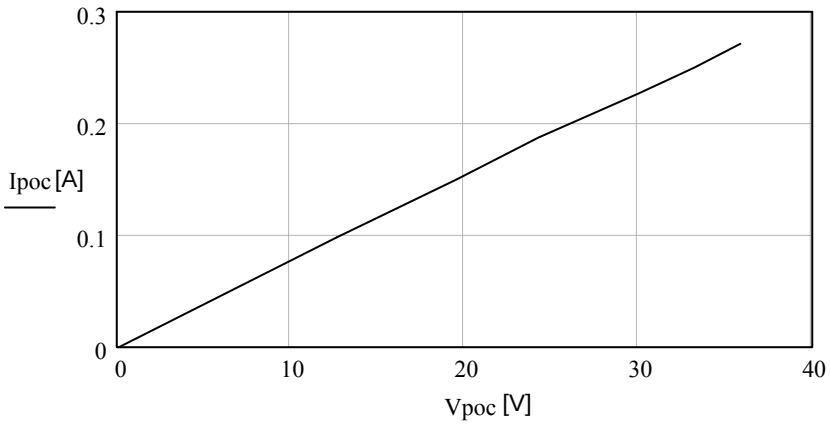


Figure 4.16 The primary current (I_{poc}) versus the primary voltage (V_{poc}) obtained from the open-circuit test.

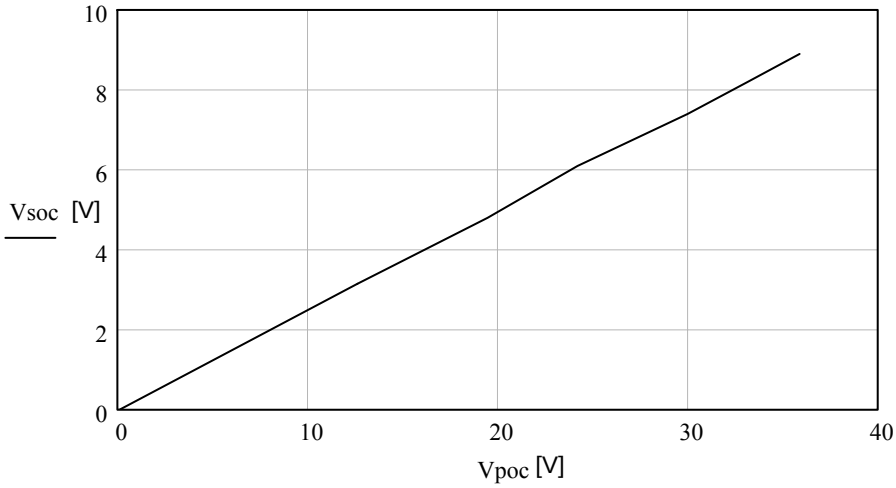


Figure 4.17 The secondary voltage (V_{soc}) versus the primary voltage (V_{poc}) obtained from the open-circuit test.

The transformer open-circuit test aims to specify the values of the circuit components on the parallel branch of the transformer equivalent circuit. Initially the open-circuit impedance (Z_{oc}) is calculated from (4.57).

$$Z_{oc} = \frac{V_1}{I_1 \angle -\varphi} \tag{4.57}$$

Since the transformer secondary side is open circuited, the equivalent circuit parameters of L_{LK1}, R_1, L_M, and R_C are included in Z_{OC}. When the impedance of the series branch of the transformer primary is subtracted from Z_{OC}, only the equivalent impedance of the parallel branch exists in the obtained expression by which L_M and R_C are calculated. Following this procedure, L_M and R_C are calculated as 422.5 μH and 21.2 kΩ at 50 kHz.

By utilizing the calculated equivalent circuit parameters, the transformer equivalent circuit at 50 kHz is shown in Figure 4.18.

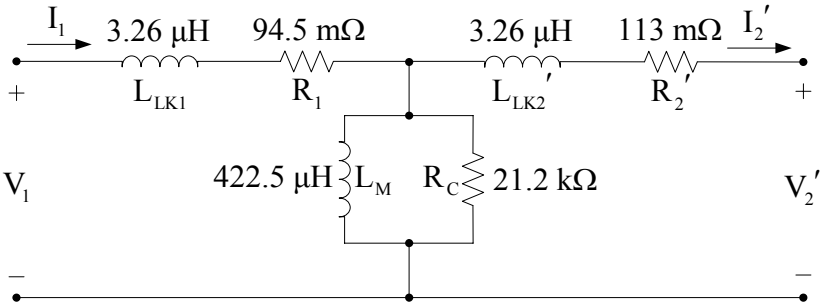


Figure 4.18 Primary referred T equivalent circuit of the transformer at 50 kHz.

4.7 The Final Design Parameters of The 5 kW FB-PS-ZVS DC/DC Converter

This chapter provided a detailed analytical design process through the exhaustive search method based design procedure and the analytical performance evaluation of the obtained convenient design parameter sets. Utilizing the determined favorable design parameter set, the transformer design and manufacture is carried out. Obtaining the equivalent circuit parameters of the manufactured transformer at the targeted operating frequency of 50 kHz, the design of the converter is finalized with the obtained additional passive circuit components of the converter, which are listed in Table 4.13. The additional external inductor (L_{ext}) is inserted in series with the transformer primary winding and the additional external capacitor (C_{ext}) is connected parallel to both of the lagging leg switches. L_{ext} value is obtained from the difference between L_t and L_{LK}, and C_{ext} value is obtained from the half of the difference between C_t and the total output parasitic capacitance of the lagging leg switches.

Table 4.13 The additional components of the 5 kW FB-PS-ZVS DC/DC converter

Additional external inductance (L_{ext})	22.2 µH
Additional external capacitance (C_{ext})	4.7 nF

Utilizing the additional components in Table 4.13 and the manufactured transformer equivalent circuit parameters, the performance of the designed FB-PS-ZVS DC/DC converter system is predicted by means of computer simulations and verified by the experimental results of the implemented system in Chapters 5 and 6, respectively.

CHAPTER 5

PERFORMANCE INVESTIGATION OF THE DESIGNED FB-PS-ZVS DC/DC CONVERTER BY MEANS OF COMPUTER SIMULATIONS

5.1 Introduction

In this chapter, the performance of the FB-PS-ZVS DC/DC converter system, which utilizes the optimum design parameters determined in the previous chapter, is investigated by means of detailed computer simulations. First, the computer simulation model of the power stage of the FB-PS-ZVS DC/DC converter system is constructed. To obtain accurate computer simulation results, device level models of the semiconductor switches are utilized in the full-bridge inverter of the converter system. After an initial study on device level modeling of the switching device, computer simulations are carried out for several load conditions and the resulting steady-state waveforms are presented in addition to the ZVS performance of switches, where the effects of the circuit component parasitics are shown. The computer simulation results also aid in estimating the energy efficiency of the converter with high accuracy. Also the dead-time effect on the converter efficiency is shown by utilizing the simulation results. A detailed numerical investigation reveals some important results regarding the dead-time, circuit parameters, and energy efficiency of the converter. Then, the controller stage of the closed loop current controlled FB-PS-ZVS DC/DC converter system is designed. A reduced order control system dynamic model is obtained with simplifications on the full model, which is formed by modeling each component of the system with an appropriate transfer function block. Then, a compensator is designed by utilizing the simplified system model and the system in closed loop current controller. Finally, the steady-

state and dynamic control performance of the closed loop current controlled system are investigated by means of computer simulations.

5.2 Modeling of The FB-PS-ZVS DC/DC Converter System

Computer simulations, which predict the performance of the designed converter system, are carried out by utilizing the Ansoft-Simplorer computer simulation package program [15]. Ansoft-Simplorer is a graphic window based power electronics circuit simulator, in which the power electronics system is formed by picking and placing the required components on its graphic window. This graphic window is also called the circuit schematic diagram of the program. The simulation results, which are the waveforms of the voltages or currents generally, are displayed on the graphic window. In the day-postprocessor window, the waveforms obtained from the simulation results are evaluated by utilizing the analysis tools such as harmonic calculator, THD calculator, etc.

The computer simulations are carried out by utilizing sufficiently small integration step size in order to increase the computational accuracy since device level models of the semiconductor switching devices are utilized in the FB-PS-ZVS DC/DC converter system. The device level models of the switches exhibit a detailed switching behavior (including the effect of device parasitics), which requires a small integration step size for more accurate simulation results. However, the system level model of the switches does not require a small step size, since it performs only on-state or off-state behavior, where the switching states (rise or fall of the switch voltage and current) occur immediately with no performance degradation. As a result, the minimum integration step size is selected as 2 ns (1/10000 of the switching period), where the switching frequency is 50 kHz (20 μs).

In this section, modeling, simulation, and performance investigation of the FB-PS-ZVS DC/DC power converter system is provided in the following subsections. First, the device level model of the semiconductor switch, which is utilized in the full-bridge inverter, is obtained and its switching characteristics are investigated by a

computer simulation study to verify that they are similar to the switching characteristics of the utilized switch in the manufactured converter system. Then, the power stage of the converter system is modeled by utilizing the determined switch device level model. Thus, the FB-PS-ZVS DC/DC power converter system is constructed to carry out the computer simulations. Then, the performance investigation studies follow.

5.2.1 Modeling of The Switching Device Utilized in The FB-PS-ZVS DC/DC Converter

As discussed in Chapter 3, the circuit operation of the FB-PS-ZVS DC/DC converter depends primarily on the parasitic components and the switching characteristics of the utilized switch in the full-bridge inverter. In Ansoft-Simplorer, the existing system level model of the switches could not meet the requirements for realistic simulation results since it does not include the detailed model involving the parasitics and device characteristics. Therefore, the device level models of the switches, which have closer switching behavior to the ones utilized in the manufactured converter system, are required for the computer simulations.

The controllable semiconductor device, which is utilized in the full-bridge inverter, is selected as IGBT due to its satisfactory performance in the high voltage and high power applications. Semikron brand fast IGBT module, SKM 100GB125DN will be utilized in the manufactured FB-PS-ZVS DC/DC converter system. This IGBT module includes two IGBTs (the dual module) with a freewheeling diode connected in parallel with each IGBT. The basic specifications of this IGBT module including dynamic characteristic information such as the switching time durations are summarized in Table 5.1.

The Ansoft-Simplorer component library does not include the SKM 100GB125DN module IGBT model. In order to obtain convenient IGBT and diode device level models with similar switching behavior to the SKM 100GB125DN module, the most appropriate IGBT device level model is selected from the Simplorer IGBT device

level model library based on the specifications of the utilized IGBT module given in Table 5.1. To investigate the switching characteristics of the IGBT device level model, a computer simulation of the test circuit, which is shown in Figure 5.1, is carried out. The test circuit system has an inductive load with a time constant (L/R) larger than the switching period interval. For an input DC voltage (V_{DC}) of 600 V and a continuous load current of 75 A, the computer simulation results showing the turn-on and turn-off transitions of the IGBT device level model are given in Figure 5.2 and Figure 5.3, respectively. In the waveforms obtained from the simulation results, the voltage or current waveforms having relatively low magnitude are scaled with a scaling factor, which is given below each corresponding figure. The scaling factor employed for the corresponding waveform is placed preceding the "x" symbol. For example, 10x implies that the original signal is multiplied with 10 and what is seen on the vertical axis is 10 times the original signal. Therefore, the original signal should be found by dividing the value read on the vertical axis by 10. Also in the time scale of the Simplorer simulation program output waveforms, micro (μ) symbol is illustrated as "u."

As can be observed in Figure 5.2, $t_{d(on)}$, which is measured from 10% of the gate-emitter voltage (V_{GE}) to 10% of the collector current (I_C), is 75 ns and t_r, which is measured from 10% of I_C to 90% of I_C, is 40 ns. For the turn-off case given in Figure 5.3, $t_{d(off)}$, which is measured from 90% of V_{GE} to 90% of I_C, is 280 ns and finally t_f, which is measured from 90% of I_C to 10% of I_C, is 15 ns.

Table 5.1 Specifications of the SKM 100GB125DN model IGBT module to be utilized in the manufactured FB-PS-ZVS DC/DC converter system

IGBT of the dual module		
V_{CES}	Collector-emitter blocking voltage rating	1200 V
I_C	Continuous collector current rating (rms) (at 25 ^oC)	100 A
V_{CEsat}	Collector-emitter saturation voltage at 75 A (at 25 ^oC)	3.3 V
$t_{d(on)}$	Turn-on delay time at I_C = 75 A (R_{gate} = 8Ω)	80 ns
t_r	Rise time at I_C = 75 A (R_{gate} = 8Ω)	40 ns
$t_{d(off)}$	Turn-off delay time at I_C = 75 A (R_{gate} = 8Ω)	360 ns
t_f	Fall time at I_C = 75 A (R_{gate} = 8Ω)	20 ns
C_{ies}	Input capacitance (at 25 ^oC)	5 nF
C_{oes}	Output capacitance (at 25 ^oC)	0.72 nF
C_{res}	Reverse transfer capacitance (at 25 ^oC)	0.38 nF
Diode of the dual module		
V_F	Forward voltage drop at I_F = 75 A (at 25 ^oC)	2 V
I_{RRM}	Peak reverse recovery current at I_F = 75 A (at 25 ^oC)	50 A
Q_{rr}	Recovered charge at I_F = 75 A (at 25 ^oC)	11.5 μC

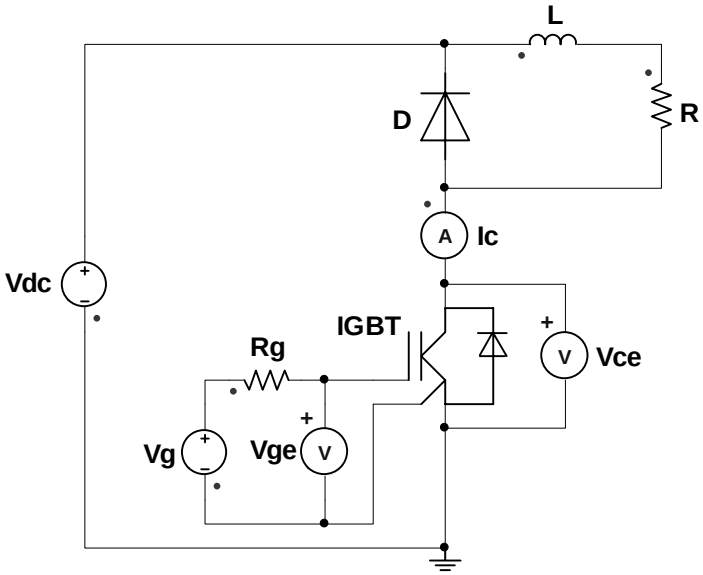


Figure 5.1 The test circuit for the IGBT device level model switching behavior study (Simplorer V7.0 Schematic ssh file).

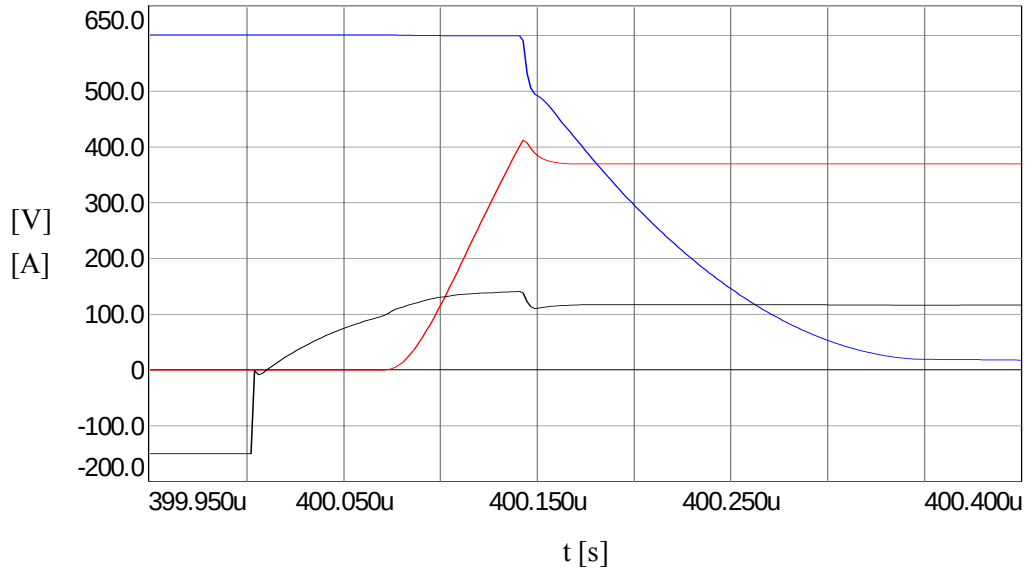


Figure 5.2 Collector-emitter voltage (blue), gate-emitter voltage (black, scale: 10x), and collector current (red, scale: 5x) waveforms during the turn-on transition of the utilized IGBT device level model.

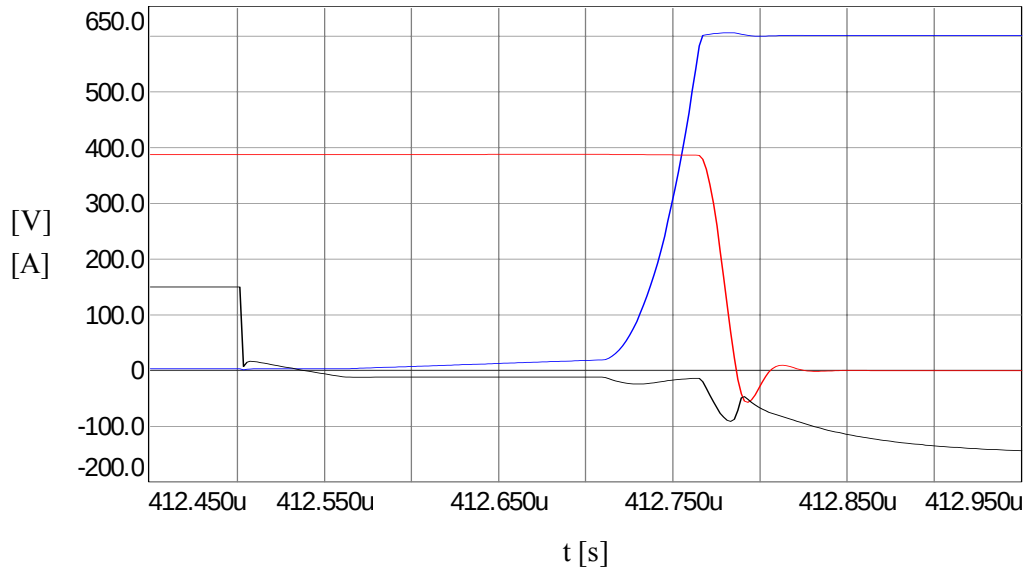


Figure 5.3 Collector-emitter voltage (blue), gate-emitter voltage (black, scale: 10x), and collector current (red, scale: 5x) waveforms during the turn-off transition of the utilized IGBT device level model.

Thus, the IGBT device level model, which has similar switching behavior to the ones for the IGBT module given in Table 5.1, is obtained and this device level model is utilized in the computer simulations of the FB-PS-ZVS DC/DC converter system throughout.

5.2.2 The Power Stage Modeling of The FB-PS-ZVS DC/DC Converter System

The simulation model circuit diagram of the power stage of the FB-PS-ZVS DC/DC converter system is given in Figure 5.4 with its building blocks defined on the same figure. From input to output, these blocks are the adjustable three phase AC voltage source, three-phase full-bridge diode rectifier, DC bus filter capacitor, single-phase full-bridge inverter, high frequency transformer, high frequency full-bridge diode rectifier, voltage clamp snubber, output filter inductor, and resistive load.

The input DC voltage of the FB-PS-ZVS DC/DC converter is supplied by the adjustable AC voltage source (emulating a three-phase variable transformer), diode bridge rectifier, and DC capacitor. The 50 Hz three-phase AC voltage source, which is modeled with the equivalent internal inductance of 100 μH per-phase, is adjusted to 170 V rms per phase in order to supply a DC voltage of 400 V to the input of the FB-PS-ZVS DC/DC converter. This is to emulate a single phase input boost Power Factor Correction (PFC) rectifier that regulates a 400 V DC bus voltage by boosting the rectified single-phase 220 V AC line. The adjusted AC line voltage is rectified by the three-phase full-bridge diode rectifier, where the utilized diodes are system level modeled. The rectified DC voltage is smoothed by the DC capacitor, which has a capacitance value of 1100 μF. Thus, the 400 V input DC voltage becomes available for the FB-PS-ZVS DC/DC converter.

The full-bridge single-phase inverter is constructed by employing the dual-pack IGBT module model discussed in the previous subsection. The gate terminal of the IGBTs are fed from a DC voltage source which applies either +15 V, when the switch gate PWM signal is 1, or -15 V when the switch gate PWM signal is 0. The switch gate PWM signal is supplied from the controller block output signal. The

controlled gate voltage is applied to the IGBT gate terminals via a series gate resistor having a value of 12 Ω.

The additional capacitors (C_{2ext} and C_{3ext}) across the lagging leg IGBTs and the additional inductor (L_{ext}) series with the transformer primary winding are inserted in the simulation model circuit diagram, where their values are listed at the end of the previous chapter (in Table 4.13). The equivalent circuit parameters of the transformer, which are calculated in the the previous chapter (shown in Figure 4.18), are utilized in the transformer simulation model.

To obtain DC voltage from the high frequency AC voltage at the transformer secondary, a high frequency full-bridge diode rectifier is utilized. The voltage at the secondary of the transformer rises from zero to V_{DC}/n (or $-V_{DC}/n$) with a significant overvoltage value at the beginning of mode 0 (or 5) due to the resonance between the the secondary referred transformer leakage inductance and additional external inductance, and the junction capacitance of the diodes, when they transition to the reverse blocking state. To include the resonance effect in the simulation, the device level model of the high frequency rectifier diodes is utilized. A forward voltage drop of 0.85 V and a junction capacitance value of 800 pF are utilized in the device level diode model.

The voltage clamp snubber, which is utilized at the output of the high frequency full-bridge diode rectifier, clamps the rectified secondary voltage to an acceptable level [16]. This voltage clamp snubber clamps the rectified secondary voltage to a constant snubber capacitor voltage. The snubber diode forms a conduction path for the current when the rectified secondary voltage is larger than the snubber capacitor voltage. The resistor connected across the snubber capacitor dissipates the excessive capacitive energy, and the resistor across the snubber diode, which is selected as 10 kΩ, provides further damping on the secondary voltage waveform. The snubber capacitor is selected as 100 nF and the resistor across the snubber capacitor is calculated as 10 kΩ, which results a constant snubber voltage of 150 V. As a result, the rectified secondary voltage is clamped to 150 V.

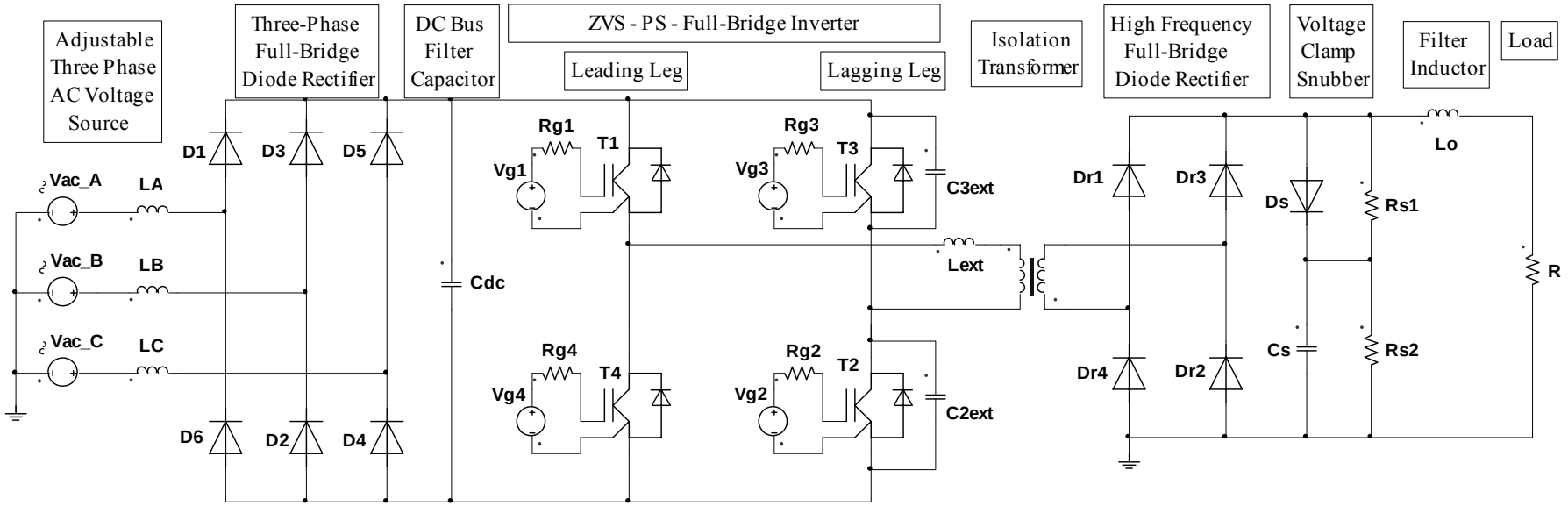


Figure 5.4 Simplorer simulation diagram of the FB-PS-ZVS DC/DC converter system power stage (Simplorer V7.0 Schematic ssh file).

The output filter consists of only an inductor, since the DC/DC converter is targeted to be a current source type power supply for the constant current welding machine. For this purpose, a current control loop exists in the controller block. The output filter inductance value is calculated as 125 μH by using the equation (4.19). The load is selected as a resistor having a rated value of 0.5 Ω.

5.3 Computer Simulation Results of The FB-PS-ZVS DC/DC Power Converter

Utilizing the model developed in the previous section, this section presents the FB-PS-ZVS DC/DC converter computer simulation results for several load current values at steady state, each demonstrating a particular converter operating condition. The simulation results of the converter are shown at the rated load, critical load (ZVS boundary) and under light load (hard-switching) conditions. Each simulation is carried out by applying the appropriate duty cycle value, which results in a determined output current value corresponding to the considered converter operating condition. The waveforms obtained from the simulation results are presented first and then the performance of the simulated systems at different load current values is evaluated by comparison with the calculated efficiency. This section verifies the converter waveforms presented in Chapter 3, which includes the switching transitions also.

5.3.1 The FB-PS-ZVS DC/DC Power Converter Simulations for Various Load Current Levels

5.3.1.1 Simulation Results at The Rated Load Current (100 A)

In this part, the computer simulation results, which show the performance of the designed FB-PS-ZVS DC/DC power converter at the rated load current (100 A), are presented. In Figure 5.5, the inverter output voltage and current, the resulting transformer secondary voltage and current, and the load current waveforms are given for the same time interval in a full PWM cycle. The steady-state waveforms at this operating point are the same as those drawn in the analysis section of Chapter 3.

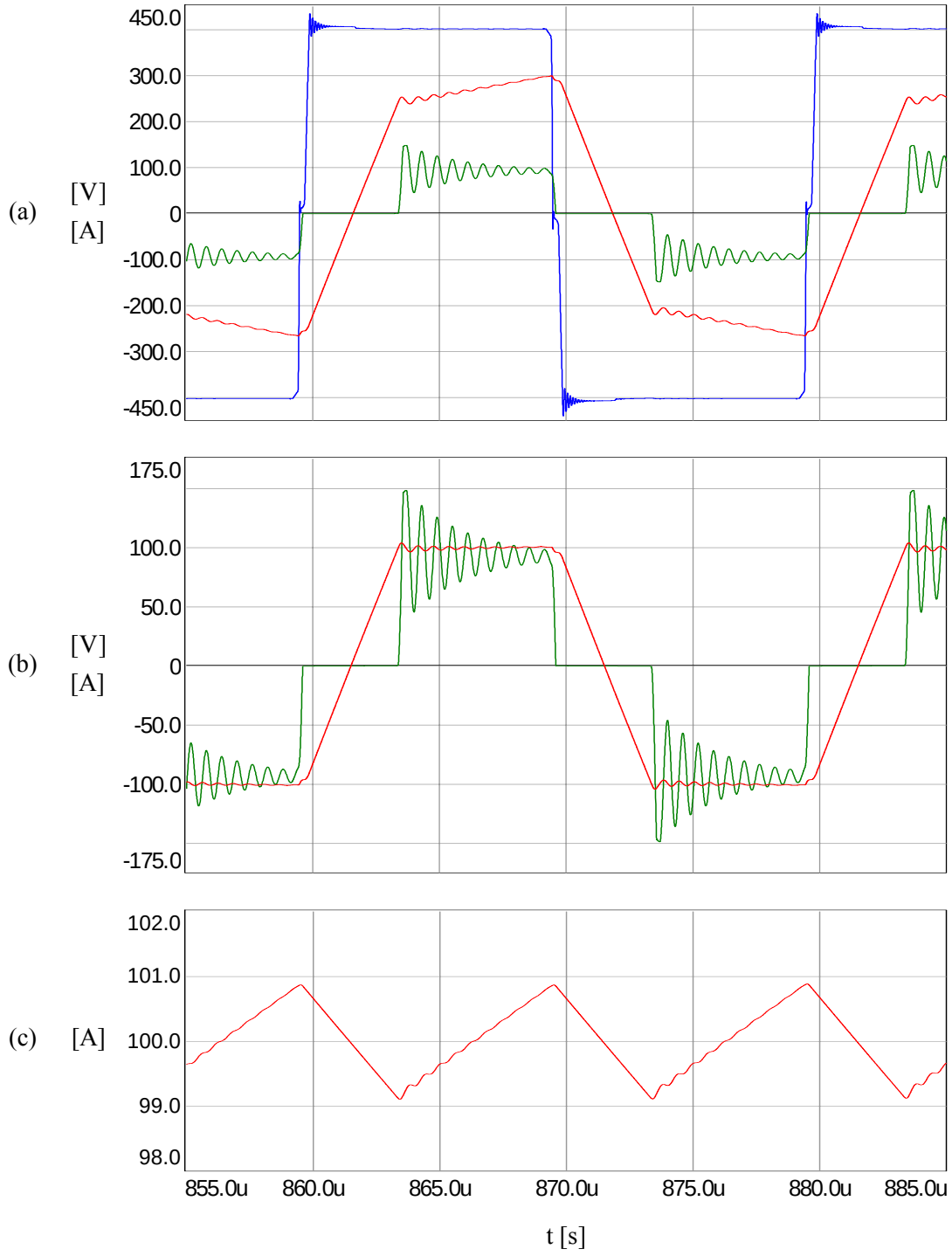


Figure 5.5 FB-PS-ZVS DC/DC power converter waveforms at the rated load current: (a) inverter output voltage (blue), transformer primary current (red, scale: 10x), and transformer secondary voltage (green), (b) transformer secondary voltage (green) and secondary current (red), (c) load current.

From Figure 5.5, it can be observed that the performance results at the rated load current, which are given in the fifth row of the Table 4.4 for the utilized design parameter set, are verified. The calculated d_O and d_{Oeff} values in Chapter 4 are verified by utilizing the inverter output voltage and transformer secondary voltage waveforms, respectively. Also the peak-to-peak ripple load current value is obtained as expected (about 2 A). The parasitic components, which are included in the device level IGBT and diode models, result in the high frequency oscillations that appear on the rising edges of the inverter output voltage and transformer secondary voltage waveforms.

The voltage and current waveforms of the leading and lagging leg IGBT modules (T_4 and T_2 respectively) are shown in Figures 5.6 and 5.7, respectively. Showing the turn-on and turn-off switching transients, these diagrams are presented in different time intervals. The gate-emitter voltage waveform is also given in these diagrams as an indicator for the ZVS turn-on. Under hard-switching operating condition, during turn-on normally a transistor blocks the DC bus voltage until the gate signal is increased from negative or zero to a significantly large positive value. Then the collector-emitter voltage rapidly drops to the on-state value. However, under ZVS operation, in both Figure 5.6 and Figure 5.7, the transistor forward voltage drops from the full blocking value to zero while the gate signal is reverse biased. Only after the collector-emitter voltage reaches the zero value and the anti-parallel diode conducts, the turn-on command is given to the transistor and the gate-emitter voltage is increased from negative to positive. Thus, in this converter, by observing the gate-emitter and collector-emitter voltages simultaneously the ZVS operation can be traced. If the collector-emitter voltage drops to zero before the gate signal becomes positive, ZVS operation occurs. Otherwise the commutation occurs under hard-switching condition. In the following chapter, which involves the experimental results, the gate-emitter voltage waveform will be employed to check whether the switch satisfies the ZVS condition or not. This is necessary because the current flowing through the IGBT module could not be observed due to unavailability of the required current measurement node in the manufactured converter.

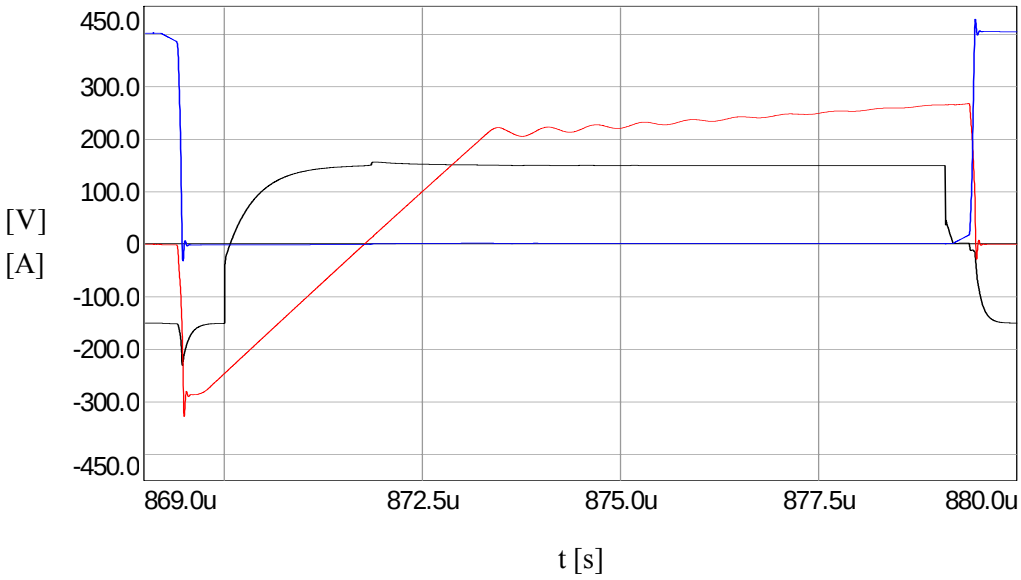


Figure 5.6 Leading leg IGBT module (T_4) waveforms at the rated load current: The voltage across the module (blue), gate-emitter voltage of the IGBT (black, scale: 10x), and current flowing through the module (red, scale: 10x).

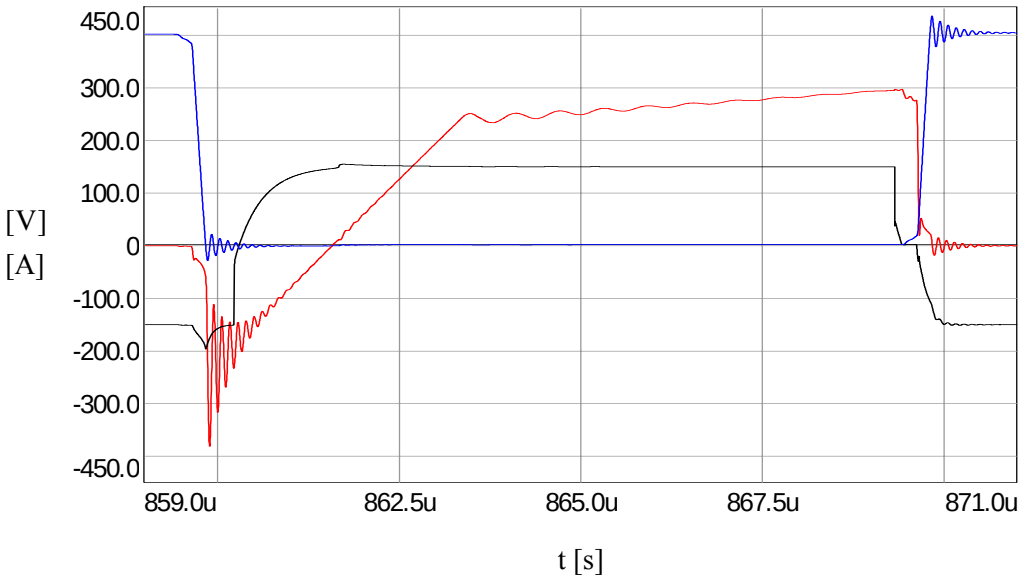


Figure 5.7 Lagging leg IGBT module (T_2) waveforms at the rated load current: The voltage across the module (blue), gate-emitter voltage of the IGBT (black, scale: 10x), and current flowing through the module (red, scale: 10x).

In the simulation results, the current waveforms of the IGBT and freewheeling diode could not be shown separately due to the fact that the device level IGBT module model in the Simplorer program does not provide individual device current measurement access to the components of the IGBT module. As can be observed from the IGBT module current waveforms, the current in positive direction flows through the IGBT and the current in negative direction flows through the freewheeling diode. In Figures 5.6 and 5.7, the inverter current starts to flow through the IGBTs after the voltage across the IGBTs decrease to zero, which means that the ZVS condition is satisfied for all IGBTs.

The turn-off of the IGBTs is completed with negligibly low switching power loss due to the equivalent output capacitance of each IGBT, which slows down the rise of the collector-emitter voltage. Hence, the IGBT is completely turned-off (I_C is decreased to zero) before V_{CE} reaches a significant value. Since an additional capacitor is connected across each lagging leg IGBT, V_{CE} of the lagging leg IGBT decreases slower than V_{CE} of the leading leg IGBT, as can be observed from the Figures 5.6 and 5.7. As a result, it can be assumed that the turn-off for all IGBTs is achieved under ZVS condition as in the turn-on condition for the rated load condition.

5.3.1.2 Simulation Results at The Critical Load Current (35 A)

The computer simulation results, which show the performance of the designed FB-PS-ZVS DC/DC power converter at the critical load current that was found as 35 A, are given in this part. In Figure 5.8, the inverter output voltage and current, the resulting transformer secondary voltage and current, and load current waveforms are shown for the ZVS boundary condition. The performance results at the critical load current given in the fifth row of the Table 4.3 for the utilized design parameter set are verified by utilizing the waveforms given in Figure 5.8, where similar d_O, d_{Oeff}, and I_{OCr} values are obtained. The critical load current is obtained as 35 A, which corresponds to 35% load.

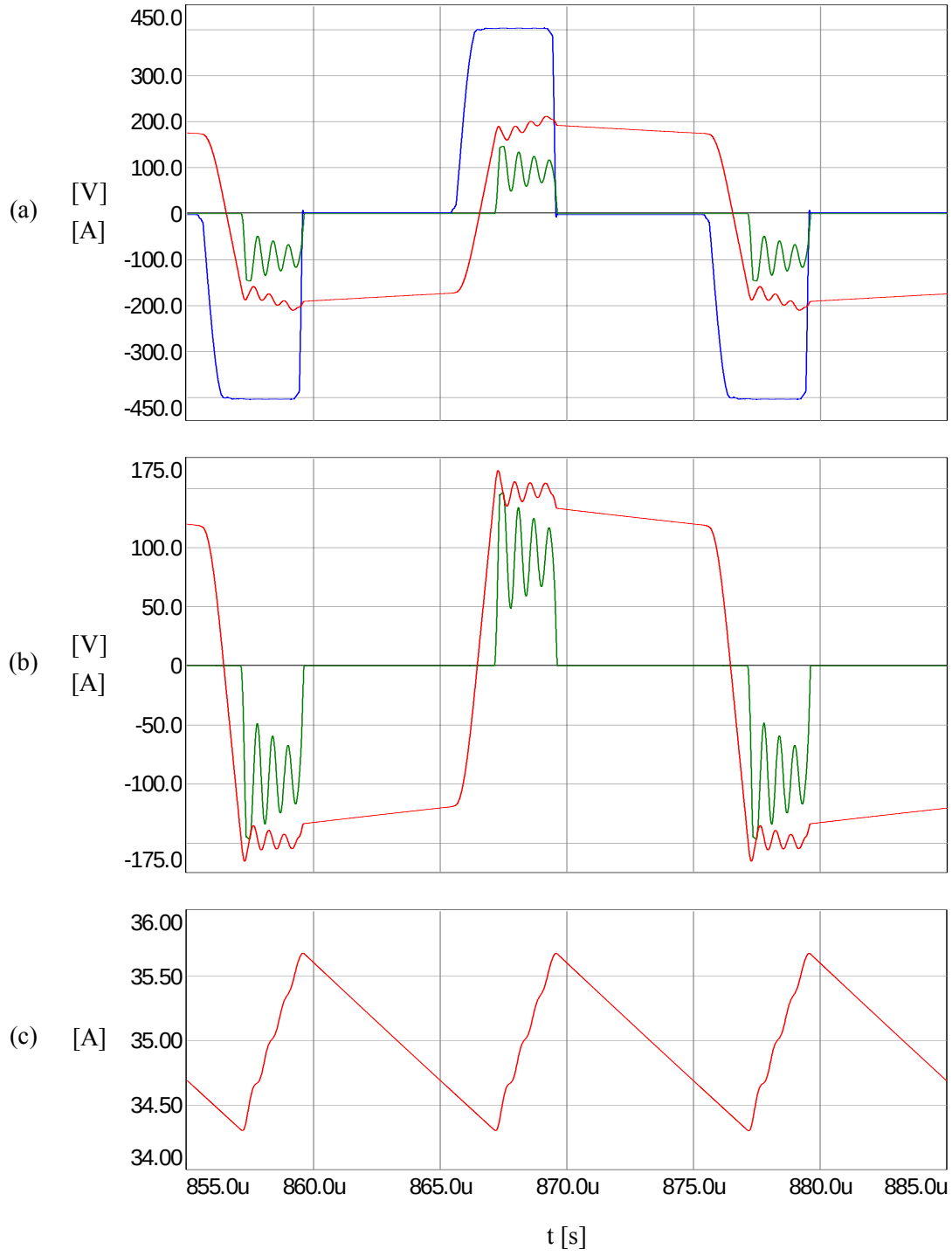


Figure 5.8 FB-PS-ZVS DC/DC power converter waveforms at critical load current: (a) inverter output voltage (blue), transformer primary current (red, scale: 20x), and transformer secondary voltage (green), (b) transformer secondary voltage (green), and secondary current (red, scale: 4x), (c) load current.

While the ZVS condition for the leading leg IGBT (T_4) is satisfied before the turn-on of this IGBT as shown in Figure 5.9, the voltage across the lagging leg IGBT (T_2) has just decreased to zero before this IGBT conducts the inverter current as can be observed in Figure 5.10. If the inverter current is higher than the critical current, the lagging leg IGBTs turn on with zero voltage across them, as in this case. Also in Figure 5.10, it can be observed that the IGBT turns on after the gate-emitter voltage reaches a significant positive voltage, which has a minimum value of the gate-emitter threshold voltage (the required minimum voltage above which a considerable current flows through the IGBT). Figure 5.11 is given to observe the turn-on and turn-off switching transitions of the lagging leg IGBT in detail for this operating condition.

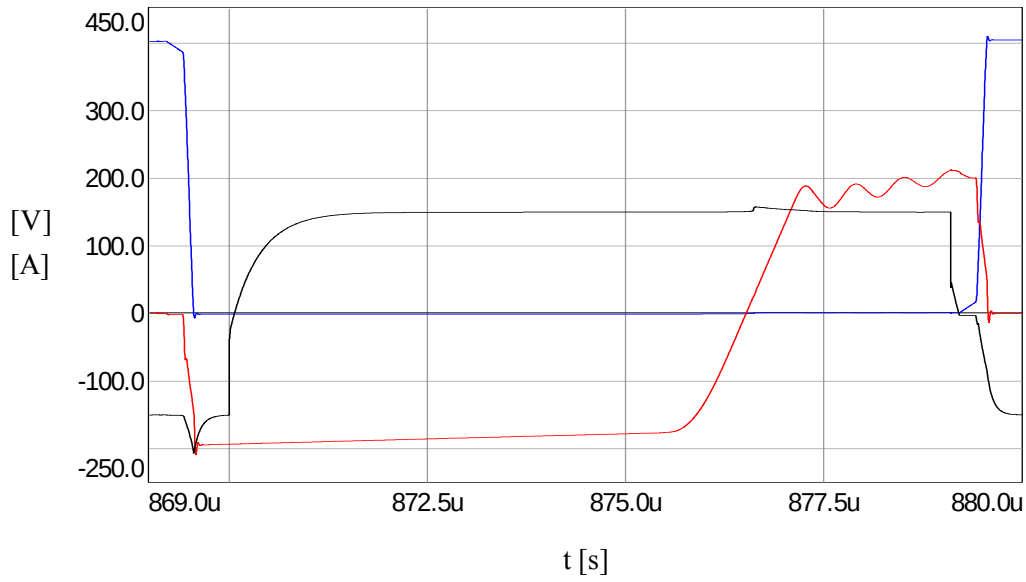


Figure 5.9 Leading leg IGBT module (T_4) waveforms at the critical load current: The voltage across the module (blue), gate-emitter voltage of the IGBT (black, scale: 10x), and current flowing through the module (red, scale: 20x).

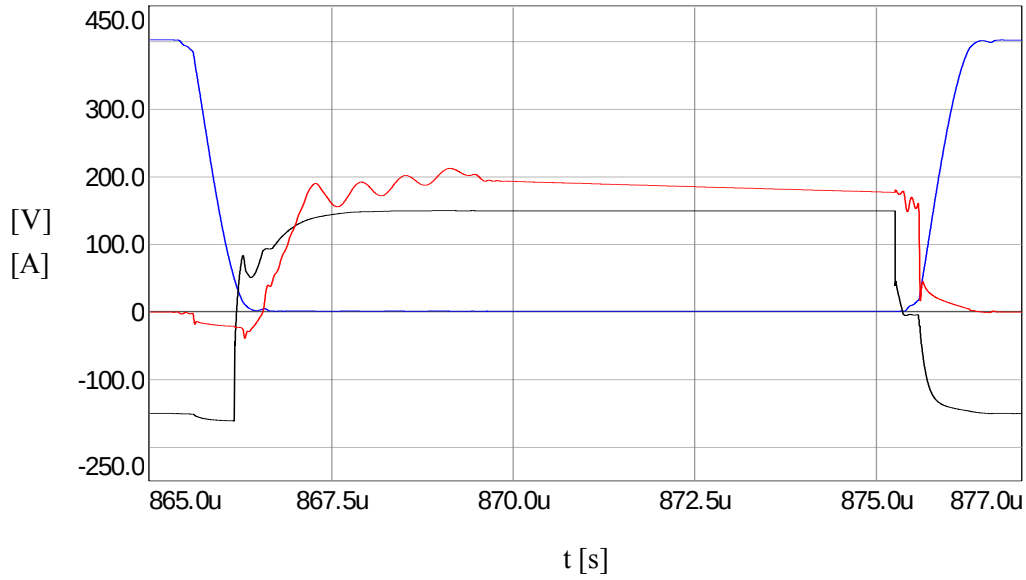


Figure 5.10 Lagging leg IGBT module (T_2) waveforms at the critical load current: The voltage across the module (blue), gate-emitter voltage of the IGBT (black, scale: 10x), and current flowing through the module (red, scale: 20x).

5.3.1.3 Simulation Results at 25% Load

The computer simulation results of the previous two subsections for the two load conditions are given to show the soft-switching behavior of the converter for the two extreme points, which are the maximum (rated) and minimum (critical) load current values satisfying the ZVS condition. In this and following part, the hard-switching behavior is investigated via the computer simulation results for two different light load conditions (25% and 15% load), where a significant degradation in efficiency can be seen.

The power converter waveforms are given in Figure 5.12 at the corresponding load current value, 25 A. Although the ZVS condition for the leading leg IGBT is satisfied as shown in Figure 5.13, the lagging leg IGBT turns on under hard-switching condition as can be observed in Figure 5.14. Figure 5.15, which also shows both switching transitions of the lagging leg IGBT, is given to observe the hard-switching condition in detail.

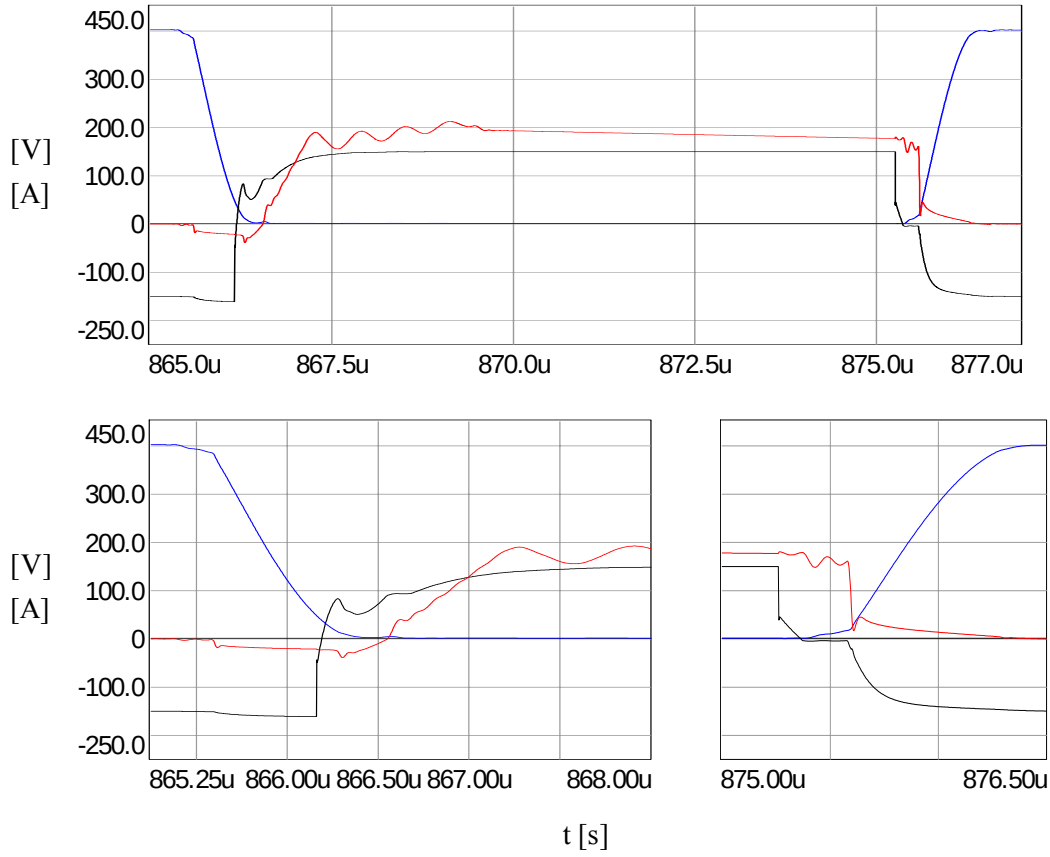


Figure 5.11 Lagging leg IGBT module (T_2) waveforms at the critical load current (top, same as Figure 5.10), and the detailed turn-on and turn-off switching transitions of this module (bottom).

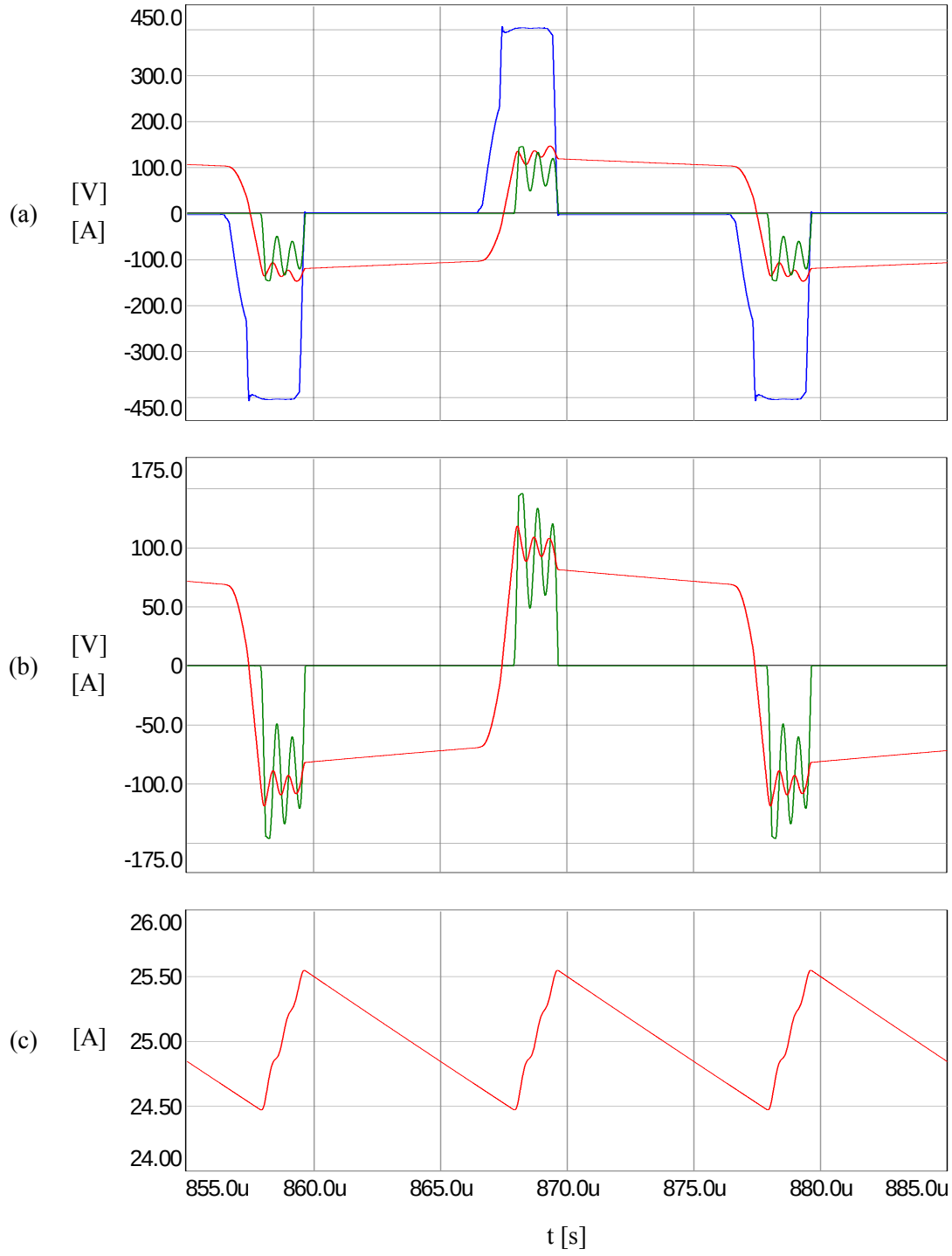


Figure 5.12 FB-PS-ZVS DC/DC power converter waveforms at 25% load: (a) inverter output voltage (blue), transformer primary current (red, scale: 20x), and transformer secondary voltage (green), (b) transformer secondary voltage (green), and secondary current (red, scale: 4x), (c) load current.

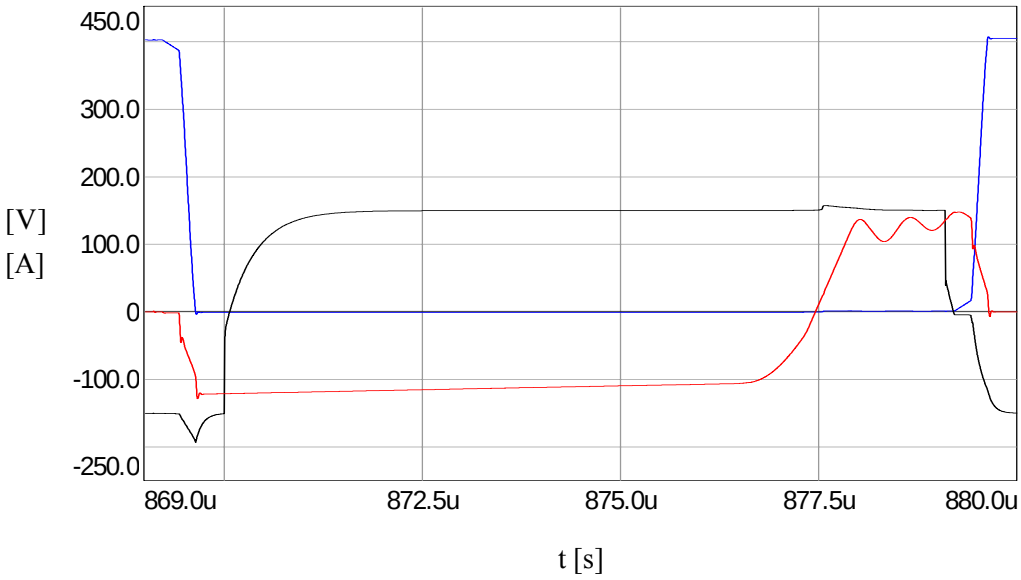


Figure 5.13 Leading leg IGBT module (T_4) waveforms at 25% load: The voltage across the module (blue), gate-emitter voltage of the IGBT (black, scale: 10x), and current flowing through the module (red, scale: 20x).

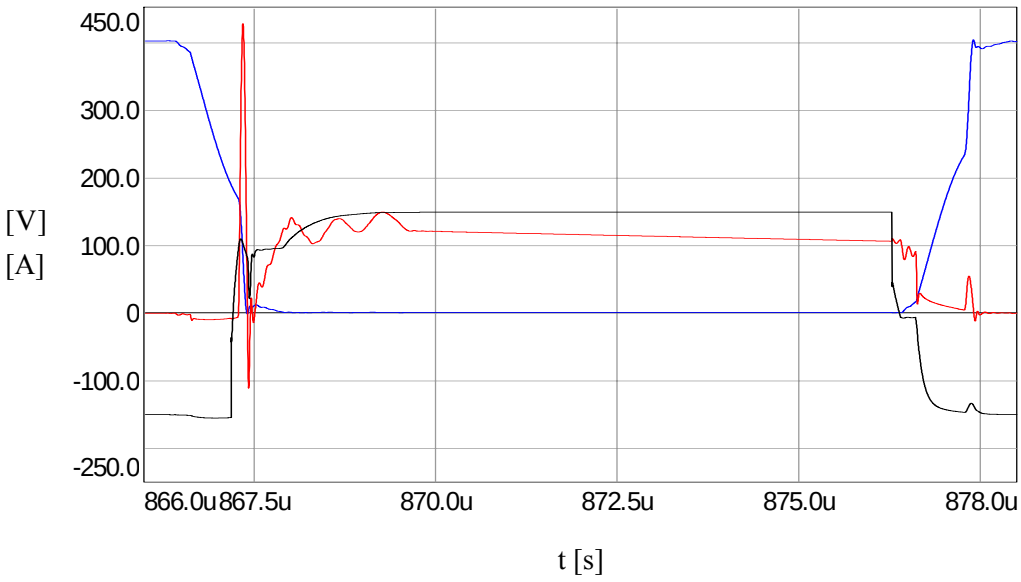


Figure 5.14 Lagging leg IGBT module (T_2) waveforms at 25% load: The voltage across the module (blue), gate-emitter voltage of the IGBT (black, scale: 10x), and current flowing through the module (red, scale: 20x).

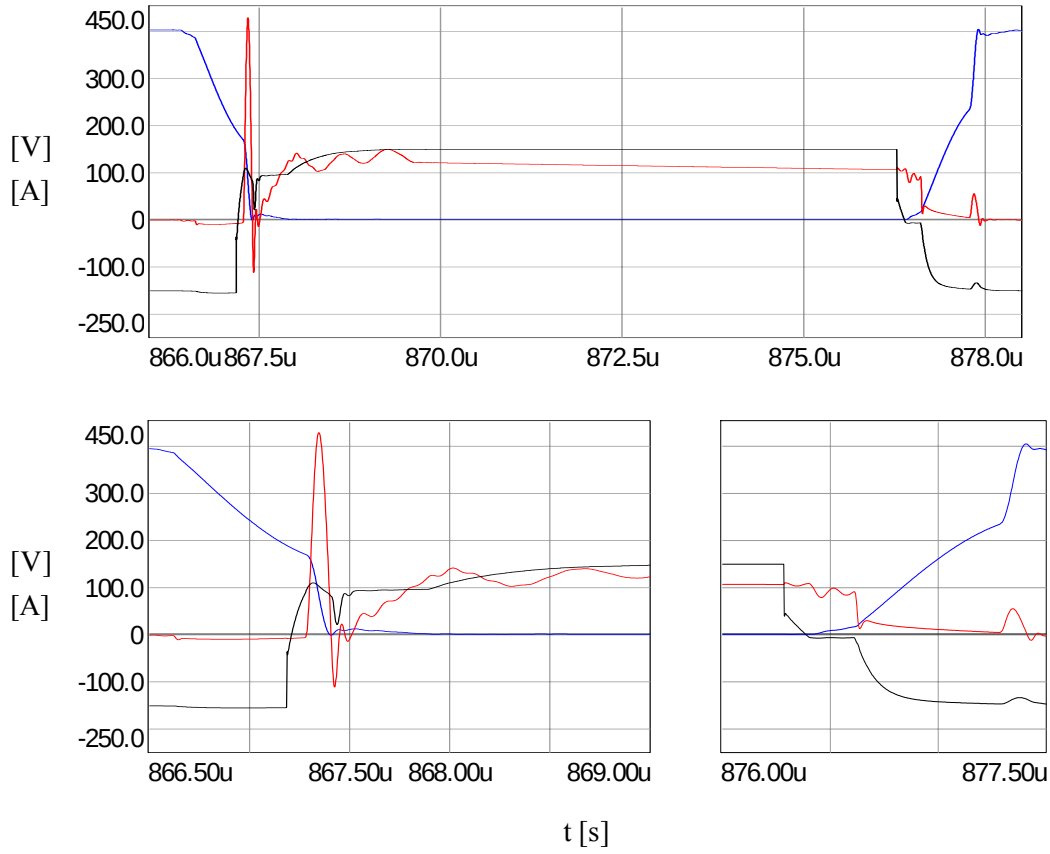


Figure 5.15 Lagging leg IGBT module (T_2) waveforms at 25% load (top, same as Figure 5.14), and the detailed turn-on and turn-off switching transitions of this module (bottom).

As can be observed in Figure 5.15, since the inverter current is below the critical current value at 25% load condition, the total equivalent capacitance across the lagging leg IGBT could not be discharged completely. The resonance operation, which provides the charging/discharging of the total equivalent capacitance across the lagging leg IGBTs, ends when the inverter current decreases to zero. Then, the IGBT current rises immediately while the collector-emitter voltage of the IGBT is decreasing faster than in the resonance operation, which results in the hard-switching condition.

5.3.1.4 Simulation Results at 15% Load

Finally, the computer simulations are carried out at 15% load, and the obtained power converter waveforms from the simulation results are given in Figure 5.16. The soft-switching and hard-switching turn-on operations of the leading and lagging leg IGBTs are shown in Figures 5.17 and 5.18, respectively. Detailed switching time intervals are given in Figure 5.19 for the lagging leg IGBT.

In Figure 5.19, similar hard-switching operation takes place as in Figure 5.15, where the required explanation is given in the previous part. At 25% load condition, the collector-emitter voltage is 125 V when the IGBT current start to rise, as can be observed in Figure 5.15. And for this condition, since the inverter current is lower than the previous case, the collector-emitter voltage is 250 V. After the resonance operation is finished, the remaining energy stored in the total equivalent capacitance of the lagging leg IGBT causes power loss on the IGBT, which was discussed in Chapter 4 as the hard-switching power loss. Since this power loss is proportional to the square of the collector-emitter voltage as given in equation (4.29), the hard-switching loss at 15% load is four times of the power loss at 25% load.

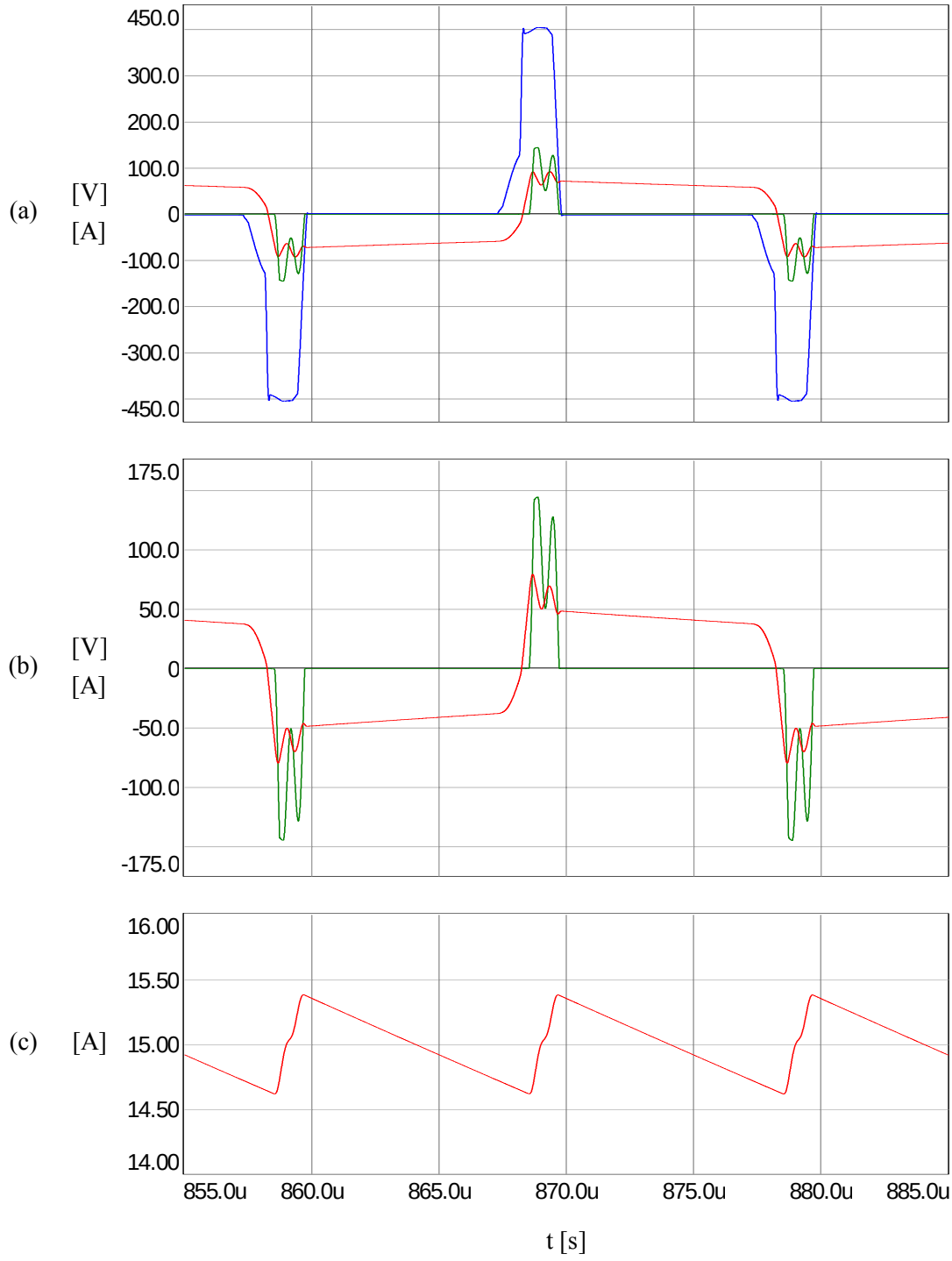


Figure 5.16 FB-PS-ZVS DC/DC power converter waveforms at 15% load: (a) inverter output voltage (blue), transformer primary current (red, scale: 20x), and transformer secondary voltage (green), (b) transformer secondary voltage (green), and secondary current (red, scale: 4x), (c) load current.

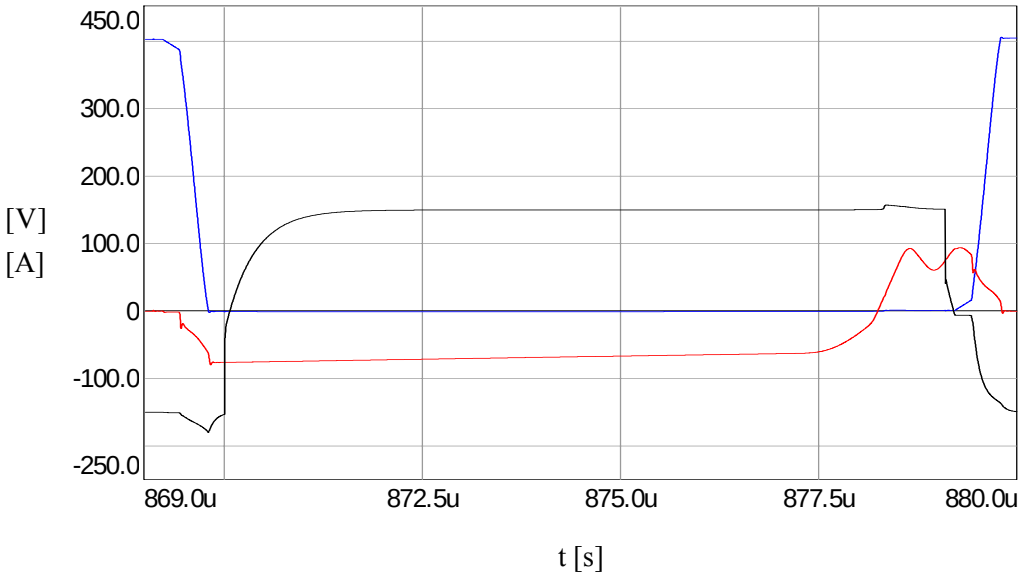


Figure 5.17 Leading leg IGBT module (T_4) waveforms at 15% load: The voltage across the module (blue), gate-emitter voltage of the IGBT (black, scale: 10x), and current flowing through the module (red, scale: 20x).

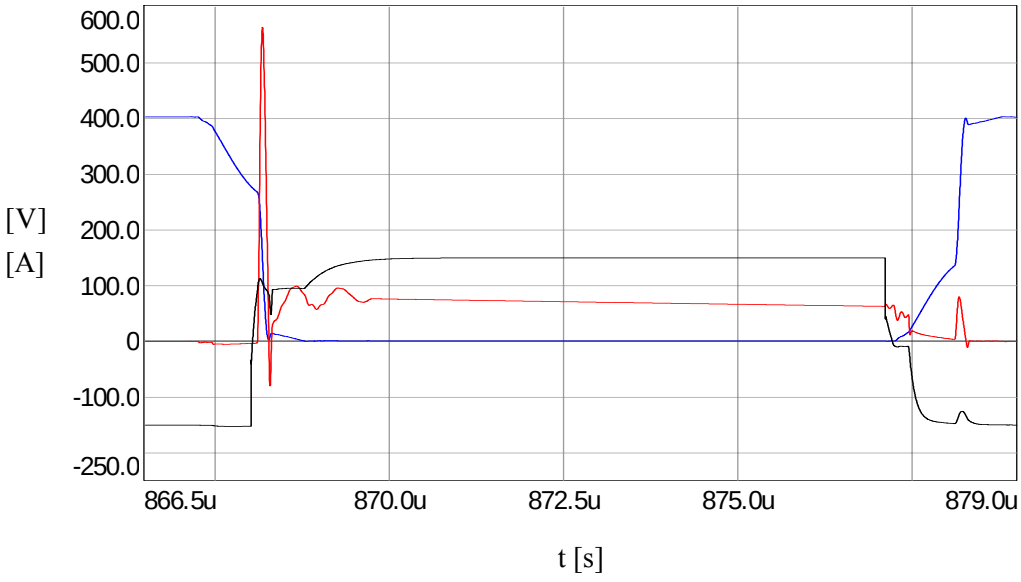


Figure 5.18 Lagging leg IGBT module (T_2) waveforms at 15% load: The voltage across the module (blue), gate-emitter voltage of the IGBT (black, scale: 10x), and current flowing through the module (red, scale: 20x).

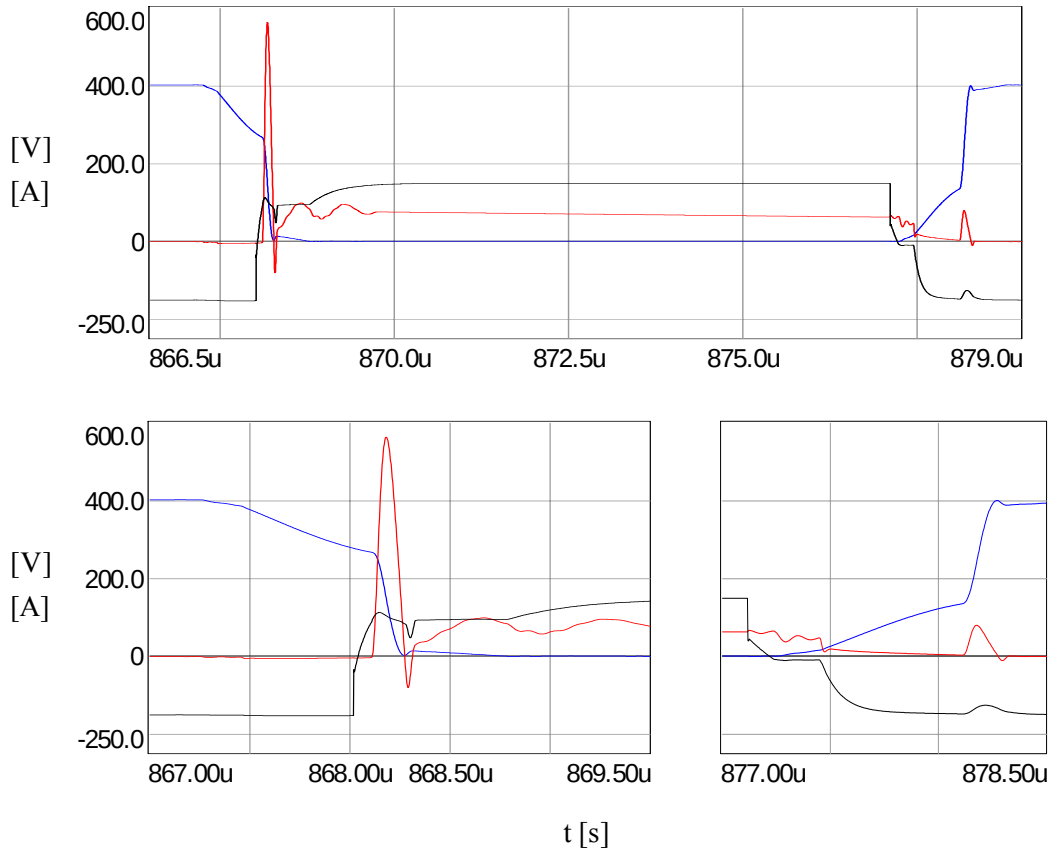


Figure 5.19 Lagging leg IGBT module (T_2) waveforms at 15% load (top, same as Figure 5.18), and the detailed turn-on and turn-off switching transitions of this module (bottom).

5.3.2 Converter Energy Efficiency Estimation By Means of Computer Simulations

Since the computer simulation involves detailed model of the power converter, the simulation results can be utilized to estimate the converter energy efficiency. Here the DC bus terminal to output efficiency is considered and the input diode rectifier efficiency is excluded from the calculations. In the following part, the efficiency performance of the FB-PS ZVS DC/DC converter system, which is obtained from the analytical calculations and computer simulations, is presented. Then, the efficiency performance of the converter system is investigated under several conditions having different dead-time, external capacitance, and external inductance values.

5.3.2.1 Designed Converter Energy Efficiency Performance and Comparison with Analytical Efficiency Estimation Results

In Chapter 4, the required equations are given to analytically calculate the energy efficiency of the converter system. Utilizing these equations, a MATLAB code, which calculates the efficiency for all operating conditions, is implemented and the relationship between the efficiency and the load current is shown in Figure 5.20. The MATLAB code, which is utilized for the analytical efficiency calculation, is given in Appendix B. Also utilizing the day-postprocessor window of Simplorer, the input and output power of the system are obtained for several load conditions. For 15%, 25%, 35% (ZVS boundary), 45%, 65%, 85%, and 100% (rated) load conditions, the efficiency values are obtained from the simulation results and inserted on the efficiency graph in Figure 5.20.

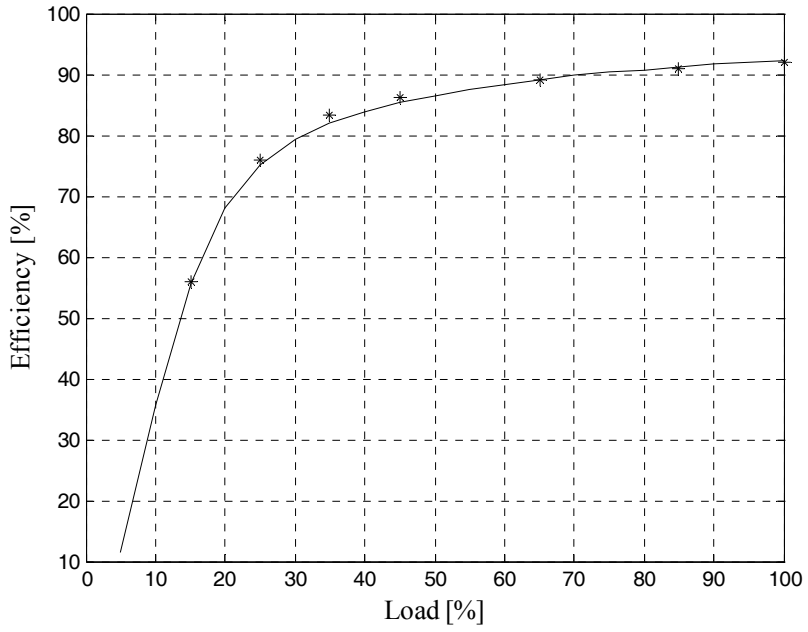


Figure 5.20 Efficiency of the FB-PS-ZVS DC/DC converter system obtained from the analytical calculation (solid line), and the computer simulation results (stars).

The efficiency of the FB-PS-ZVS DC/DC converter system is high when the soft-switching condition is satisfied. The designed and simulated system starts to satisfy

the ZVS condition at 35% load, which corresponds to the critical load current value. It can be observed from Figure 5.20 that the efficiency curve becomes high and almost flat for the load current values higher than the critical load current due to absence of the switching loss mostly. Due to ZVS operation of the switches, the efficiency is better than 80% in the soft-switching range of the converter. Also the calculated efficiencies from the computer simulation results are in strong correlation with the analytical efficiency calculation results.

5.3.2.2 Energy Efficiency Performance Investigation of the FB-PS-ZVS DC/DC Converter Considering the Dead-Time Effect

In the implemented converter system (to be discussed in detail in the next chapter), the dead-time of the converter is specified as 0.9 μs, and therefore, the performance of the designed converter is investigated by utilizing the simulation results with a dead-time of 0.9 μs as in the previous part.

The dead-time is specified based on the utilized semiconductor switching device. Since the turn-on and turn-off transitions in power MOSFETs are completed in a short time interval, the dead-time required for high current carrying MOSFETs is typically less than 1 μs that provides reliable switching operations. However, IGBTs require larger dead-time interval due to tail current during the turn-off switching transition. A reliable switching operation for high current carrying IGBTs requires a dead-time of about 2-3 μs. This dead-time value is a general recommendation stated by the semiconductor device manufacturers. In the implemented converter system, the dead-time inserted between the IGBTs is specified as 0.9 μs since the utilized switch is a fast IGBT module having smaller switching time intervals (listed in Table 5.1) and operated under soft switching operating condition. A smaller dead-time value increases the maximum duty cycle (equation (4.7)) that the inverter can output, while decreasing the reliability. Hence, the dead-time requirement of the semiconductor switch must be determined based on the switching device characteristics.

To investigate the effect of increasing the dead-time on the energy efficiency, two more simulations are carried out in addition to the one performed for 0.9 μs, the result of which is presented in Figure 5.20 (shown in the previous part). In these simulations, dead-time values are selected as 2 μs and 3 μs, while all other design parameters are kept constant. For the three parameter sets that are listed in Table 5.2, the resulting efficiency curves are shown in Figure 5.21. On the efficiency curves "o" characters represent the ZVS boundary current value of the corresponding case. As can be observed from this figure, increasing the dead-time for more reliable switching operation decreases the efficiency. Due to the long dead-time interval, the voltage at the lagging leg switch rises again after it remains at zero for a short span of time. Thus, the corresponding switch turns on with a significant voltage on it, which results in larger ZVS boundary current and lower efficiency. For the case with 3 μs dead-time, the ZVS condition could not be satisfied even at the rated load, which results in much lower efficiency curve than for other two cases.

Table 5.2 Converter design parameters utilized in the performance comparison of converters having different dead-time values

	Parameters for 0.9 μs dead-time (black)	Parameters for 2 μs dead-time (blue)	Parameters for 3 μs dead-time (red)
t_d (μs)	0.9	2	3
L_{ext} (μH)	23	23	23
C_{ext} (nF)	4.7	4.7	4.7
n	4	4	4

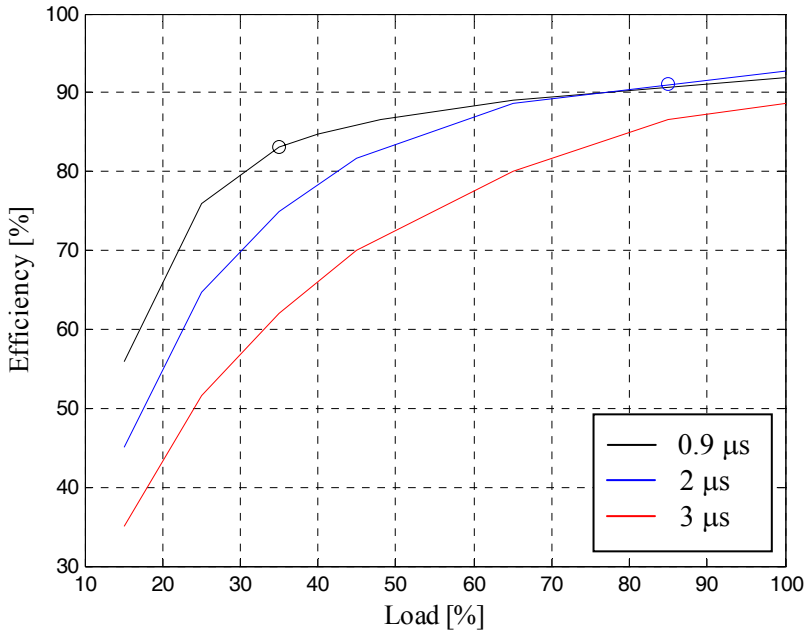


Figure 5.21 Eficiency of the FB-PS-ZVS DC/DC converter system obtained from the computer simulation results for various dead-time values.

This part presents the effect of the external capacitance for the case with a dead-time of 2 µs. The performance evaluated converter parameter sets are given in Table 5.3. To improve the efficiency curve for the case of 2 µs dead-time (also shown in Figure 5.21 for the parameters of Table 5.2), the value of the external capacitance is increased. The efficiency curves for three different external capacitance values are shown in Figure 5.22. As can be observed in Figure 5.22, increasing the external capacitance improves the efficiency curve up to the ZVS boundary current value. This is due to the fact that a larger capacitance value results in slower capacitor voltage rise (for the case as illustrated in Figure 4.2) and less switching losses under hard-switching condition. However, the increase in the capacitance value does not strongly alter the energy efficiency characteristics and only the third digit is influenced.

Table 5.3 Converter design parameters utilized in the performance comparison of converters having different external capacitance values

	Parameters for 4.7 nF external capacitance (blue)	Parameters for 9.1 nF external capacitance (red)	Parameters for 15 nF external capacitance (black)
t_d (μs)	2	2	2
L_{ext} (μH)	23	23	23
C_{ext} (nF)	4.7	9.1	15
n	4	4	4

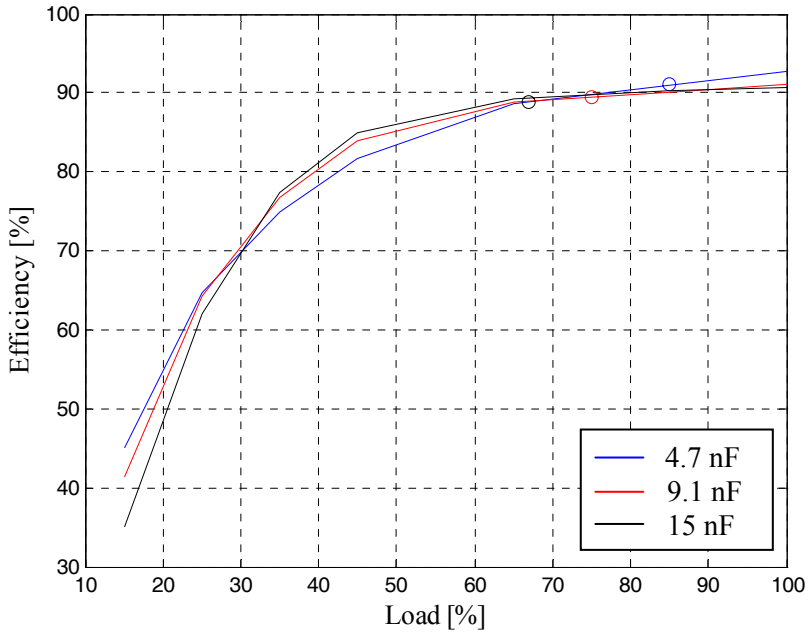


Figure 5.22 Eficiency of the FB-PS-ZVS DC/DC converter system obtained from the computer simulation results for various external capacitance values.

The effect of the external inductance is shown by means of computer simulations in this part. For the three converter parameter sets listed in Table 5.4, the resulting efficiency curves are shown in Figure 5.23. As can be observed in this figure, increasing the external inductance improves the efficiency for whole load range since the ZVS boundary current value and hence the switching loss are decreased. However, there is a maximum limit value for the external inductance which satisfies the rated output voltage. Over the maximum L_{ext} value, d_{Oeff} results in a lower output

voltage than its rated value. The third parameter set in Table 5.4 has a L_{ext} value of 28 µH, which is the maximum limit value for this case.

Table 5.4 Converter design parameters utilized in the performance comparison of converters having different external inductance values

	Parameters for 15 µH external inductance (blue)	Parameters for 23 µH external inductance (red)	Parameters for 28 µH external inductance (black)
t_d (µs)	2	2	2
L_{ext} (µH)	15	23	28
C_{ext} (nF)	9.1	9.1	9.1
n	4	4	4

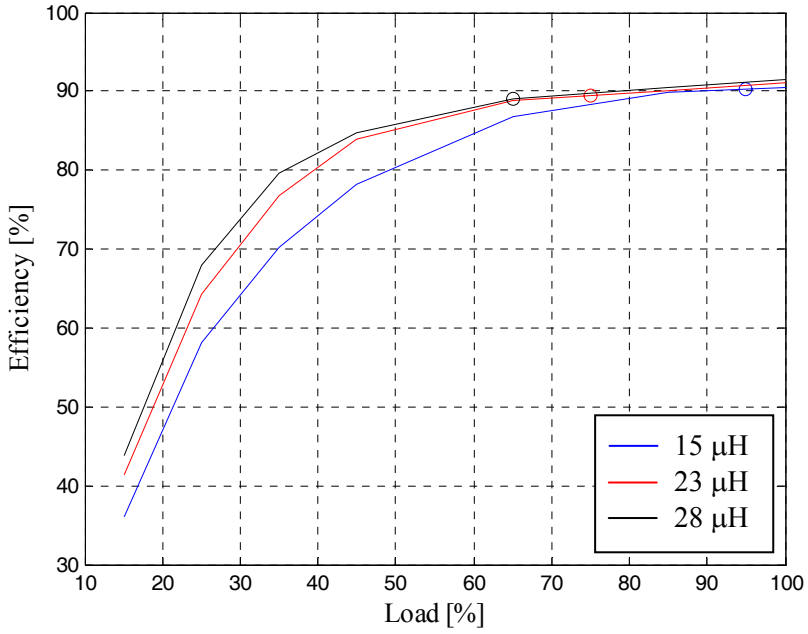


Figure 5.23 Eficiency of the FB-PS-ZVS DC/DC converter system obtained from the computer simulation results for various external inductance values.

As a result, increasing the dead-time has an adverse effect on the efficiency while increasing the reliability. As shown above, applied modifications (increasing the external inductance and capacitance) improve the efficiency for the case with 2 µs dead-time; however, it could not reach the efficiency values of the case with 0.9 µs dead-time. It can be concluded from this study that the large dead-time has

detrimental effects on the converter efficiency and this is the major factor that limits the converter energy efficiency.

5.4 Reduced Order Modelling of the System, Controller Design, and Output Current Regulation

Since the FB-PS-ZVS DC/DC converter system is designed to be utilized in a constant current welding machine, the system is controlled by regulating the output current. The general block diagram of the closed loop current controlled FB-PS-ZVS DC/DC converter system is given in Figure 5.24. In order to design an appropriate controller, the system must be modeled in detail. In this section, first each component of the system in Figure 5.24 is modeled with an appropriate continuous time transfer function block. Then, with simplifications on the full model, a reduced order mathematical model is obtained. Given the simplified system model, a compensator is designed and the system steady-state and dynamic control performance are investigated by means of computer simulations.

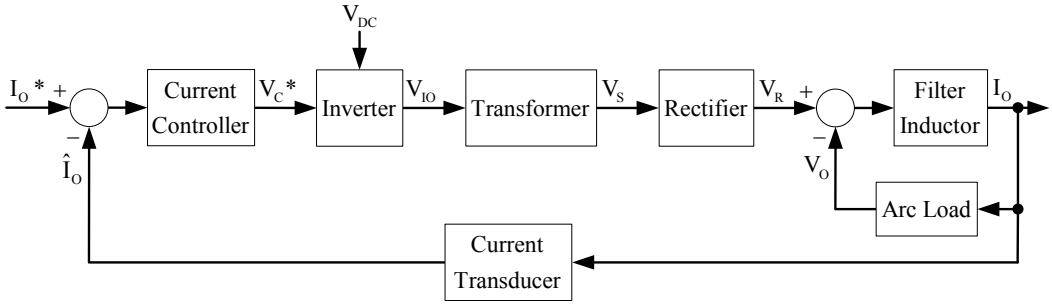


Figure 5.24 General block diagram of the closed loop current controlled FB-PS-ZVS DC/DC converter system.

The detailed block diagram of the closed loop current controlled converter system of Figure 5.24 is given in Figure 5.25. In this block diagram, there are additional blocks which are not included in the block diagram given in Figure 5.24. As will be discussed in the next chapter in detail, in this work the controller will be implemented on a digital platform. For that purpose a Digital Signal Processor (DSP)

will be employed and the control algorithm will be implemented via software. As a consequence, the converter system control block diagram involves the A/D conversion delay, computation delay, and PWM delay blocks.

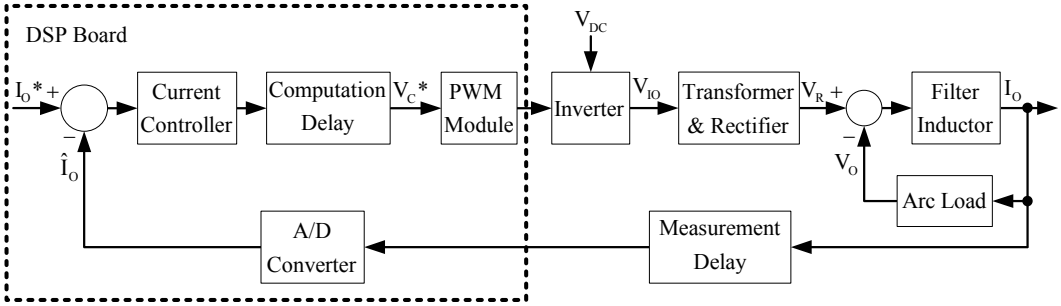


Figure 5.25 Detailed block diagram of the closed loop current controlled FB-PS-ZVS DC/DC converter system.

The load current, which is the main control variable of the FB-PS-ZVS DC/DC converter system, is measured by a current transducer and applied to the digital control unit as the feedback signal of the closed loop system. The hall-effect current sensor utilized in the experiments has a bandwidth of 200 kHz (adequate for this application), which results in a measurement delay (τ_M) of 5 μs. Thus, the measurement delay in Figure 5.25 can be modeled with a first order delay transfer function with unity gain and 5 μs time constant. The measured current signal is input to the analog-to-digital (A/D) converter of the DSP and the feedback signal is regularly sampled at the PWM frequency. Since the A/D converter settles in a finite time length, there is a delay ($\tau_{A/D}$) associated with the A/D converter, which is typically a few microseconds or less. The sampled feedback signal is utilized in the control algorithm to generate the voltage reference (V_C^*), which is applied to the PWM block at the end of the PWM cycle. Since in a discrete time controller the control functions involve computations, a computation delay (τ_C) corresponding to the number of processor instruction cycles from the beginning to the end of the code is generated. The PWM pulse generator only accepts command signals once per PWM cycle. As a result, there is an idle time between the instant where the reference voltage is ready and when the PWM signal can be updated. The A/D conversion

time, the computation delay time and the idle time can all be lumped in one delay element and termed as the sampling delay. Thus, the sampling delay (τ_S) is the sum of the A/D conversion delay time, computation delay time, and idle time and equals to one PWM period as a total.

The load current of the FB-PS-ZVS DC/DC converter is controlled by utilizing a linear proportional and integral (PI) type regulator. This controller method is preferred since it is an adequate and simple controller solution. Also, the PI controller has good regulation performance for DC signals since the integral term results in high controller gain at low frequency [17]. The continuous time transfer function of the PI controller is given in (5.1).

$$G_C(s) = K_P + \frac{K_I}{s} \tag{5.1}$$

The reference voltage (V_C^*) is applied to the PWM block and updated once every PWM cycle T_S. The PWM block generates the required gate logic signals to drive the switching devices in the full-bridge inverter. As introduced in Chapter 2, all the switch duty cycles in the phase-shifted PWM scheme are 50%, and the generated V_C^* is converted to the corresponding phase-shift angle, which is introduced between the leading and lagging leg switch PWM signals. Resulting from the applied switch PWM signals, the diagonal switches in the full-bridge inverter conduct together and apply $+V_{DC}$ or $-V_{DC}$ at the inverter output with a duty cycle of d_O. Since the PWM frequency is quite high compared to the load and filter corner frequencies, the PWM cycle average model of the inverter can be utilized in the system modeling study. The inverter PWM cycle average model is a voltage amplifier with unity gain and first order delay element with a PWM delay (τ_{PWM}) of half PWM cycle ($T_S/2$).

The rectifier output voltage involves the DC average value and the ripple at twice the inverter frequency and its multiples. In terms of delays, similar to the PWM inverter, the rectifier results in half the inverter fundamental cycle delay. Therefore, the rectifier can also be modeled with a unity-gain first order delay element, which has a

delay (τ_R) of half a PWM cycle. Located between the rectifier and the inverter, the transformer is dominantly modeled by its leakage inductances. Therefore, the transformer and also the additional series inductance can be added to the output filter inductance and the lumped inductance model represents all the magnetics in the circuit. The resulting transfer function, $G_P(s)$ for the magnetic components and the load is given in (5.2).

$$G_P(s) = \frac{1}{n} \cdot \frac{1}{(L_O + L_{LK}' + L_{ext}')s + R_d + R_O} \tag{5.2}$$

In (5.2), n is the transformer primary to secondary turns ratio, L_O is the output filter inductance, L_{LK}' and L_{ext}' are the secondary side referred values of the transformer leakage inductance and additional series inductance, R_O is the load resistance, and R_d, which is given in (5.3), is the term origining from the duty cycle loss in mode 4 [18]. As discussed in Chapter 3, the transformer secondary voltage remains zero while the primary voltage is nonzero in mode 4, which results in an output voltage duty cycle reduction. The effect of this reduction is included in the transfer function by utilizing R_d in the corresponding transfer function.

$$R_d = \frac{4 \cdot L_t \cdot f_S}{n^2} \tag{5.3}$$

The continuous time equivalent model of the closed loop current controlled FB-PS-ZVS DC/DC converter system is shown in Figure 5.26 in detail. Utilizing the given block diagram in Figure 5.26, and assuming the time constants for measurement delay, sampling delay, PWM delay, and rectifier delay are comparable to each other and small compared to the load and controller time constants, then the delays can be summed up in an equivalent total delay τ_T. As a result, the continuous time block diagram of the reduced order closed loop current controlled system model is obtained as in Figure 5.27.

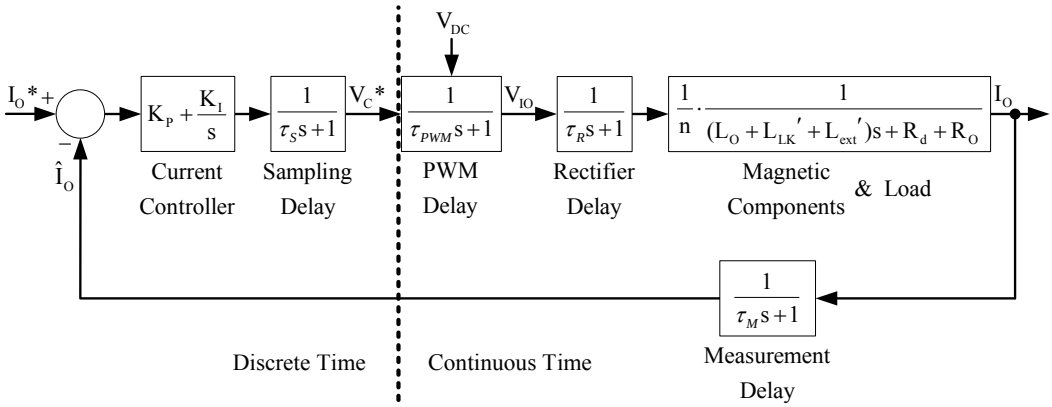


Figure 5.26 Equivalent continuous time representation of the closed loop current controlled FB-PS-ZVS DC/DC converter system block diagram.

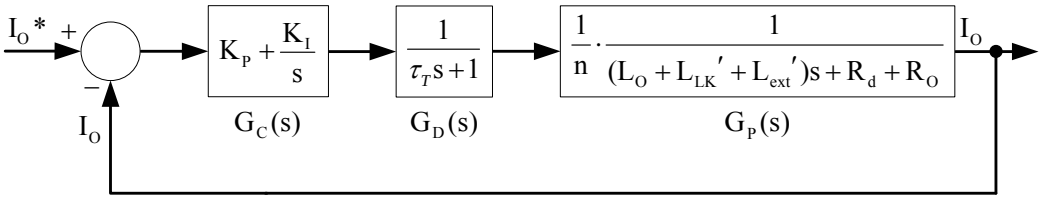


Figure 5.27 The reduced order continuous time model based block diagram of the closed loop current controlled FB-PS-ZVS DC/DC converter system.

Given the control system model of Figure 5.27, the PI controller gains are calculated for the designed converter circuit parameters. In Figure 5.27, the transfer function $G_P(s)$ is the dominant pole of the system while the transfer function $G_D(s)$ has a pole on the far left plane of the S domain. With $G_P(s)$ having the dominant pole, the optimal control law for the system is the pole-zero cancellation law. By utilizing this law, the pole of the transfer function $G_P(s)$ is canceled by the zero of the PI compensator transfer function. In order to cancel the pole with zero, the ratio of K_P to K_I is taken as equal to the ratio of the total inductance to total resistance in $G_P(s)$, as given in (5.4). The resulting open loop transfer function for the system, $G_{OL}(s)$ is given in (5.5).

$$\frac{K_P}{K_I} = \frac{L_O + L_{LK}' + L_{ext}'}{R_d + R_O} \tag{5.4}$$

$$G_{OL}(s) = \frac{K_I / \left(n \cdot R_d + n \cdot R_O\right)}{s\left(\tau_T s + 1\right)} \tag{5.5}$$

The second order closed loop transfer function of the system is given by utilizing the general representation given in (5.6), where ω_n is the undamped natural frequency, and ζ is the damping ratio of the system. The equations (5.7) and (5.8) define ω_n and ζ for this closed loop system, respectively.

$$H(s) = \frac{{\omega_n}^2}{s^2 + 2\zeta\omega_n s + {\omega_n}^2} \tag{5.6}$$

$$\omega_n = \sqrt{\frac{K_I / \left(n \cdot R_d + n \cdot R_O\right)}{\tau_T}} \tag{5.7}$$

$$\zeta = \frac{1}{2 \cdot \sqrt{\tau_T \cdot K_I / \left(n \cdot R_d + n \cdot R_O\right)}} \tag{5.8}$$

Choosing ζ as 0.707, an underdamped system behavior is obtained, where the closed loop poles are complex conjugates and on the left half plane of the S domain. Thus, K_I is calculated by using (5.9), and then K_P is calculated from (5.4). The converter circuit parameters utilized in the given equations so far, and the calculated PI controller constants, K_P and K_I are listed in Table 5.5.

$$K_I = \frac{n \cdot \left(R_d + R_O\right)}{4 \cdot \zeta^2 \cdot \tau_T} \tag{5.9}$$

Table 5.5 Closed loop FB-PS-ZVS DC/DC converter system parameters

n	4
L_O	125 μH
L_{LK}'	0.4 μH
L_{ext}'	1.4 μH
R_d	0.36 Ω
R_O	0.5 Ω
τ_T	45 μs
K_P	5.6
K_I	38222

In the controller, an anti-windup mechanism is utilized in order to avoid integrator windup. Having defined all the parameters utilized in the closed loop system block diagram, the design of the controller stage is finalized. In the following section, the performance evaluation of the designed controller is carried out by utilizing the computer simulation results.

5.5 Performance Prediction of The Designed Controller By Means Of Computer Simulations

The performance of the output current controller can be investigated by the changes in the current command, input AC grid line voltage, and load resistance. In this section the computer simulation results, which show the effect of the changes in the output current command and load resistance on the output current waveform, are given. The line disturbances are decoupled from the designed controller by multiplying the calculated reference voltage (V_C^*) with the ratio of the desired constant DC input voltage to the measured DC bus voltage. The line regulation performance of the controller is not shown here, since the controller performance will not change unless the DC bus voltage is below the value to generate the required control voltage reference.

First, the step response of controller is tested by applying a step current command signal to the system. The FB-PS-ZVS DC/DC converter system is simulated by applying a step current command signal from 0 to 100 A to the system at t=0. The output current reaches 100 A from the initial condition of zero current value in 400 μs as can be observed in Figure 5.28. Hence, it is shown that the controller bandwidth is approximately 2.5 kHz.

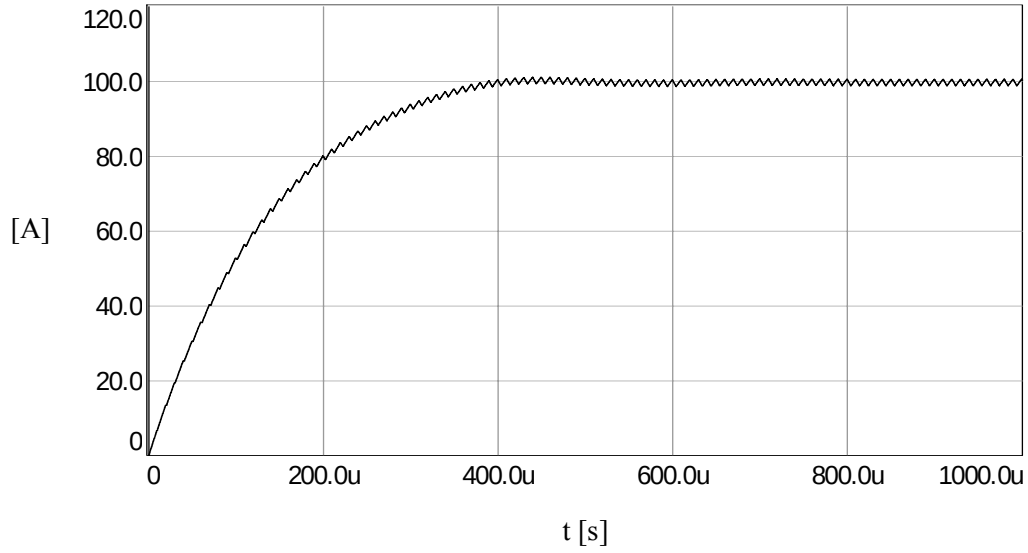


Figure 5.28 Step response performance of the output current controller.

The load regulation performance of the controller is tested by applying a step change in the load resistance while keeping the load current command constant. Initially, the output current command value is set as 100 A, and the load resistance is 0.5 Ω. At t=1 ms, the load resistance is decreased by connecting an extra parallel load resistance having a value of 0.5 Ω. Once the 100% load resistance step change occurs, the load current initially increases due to the reduced resistance, however the controller regulates the current and the load current settles at 100 A again in 500 μs with a current overshoot value of 11 A as can be observed in Figure 5.29. Here the response time of 500 μs is again related to the controller bandwidth.

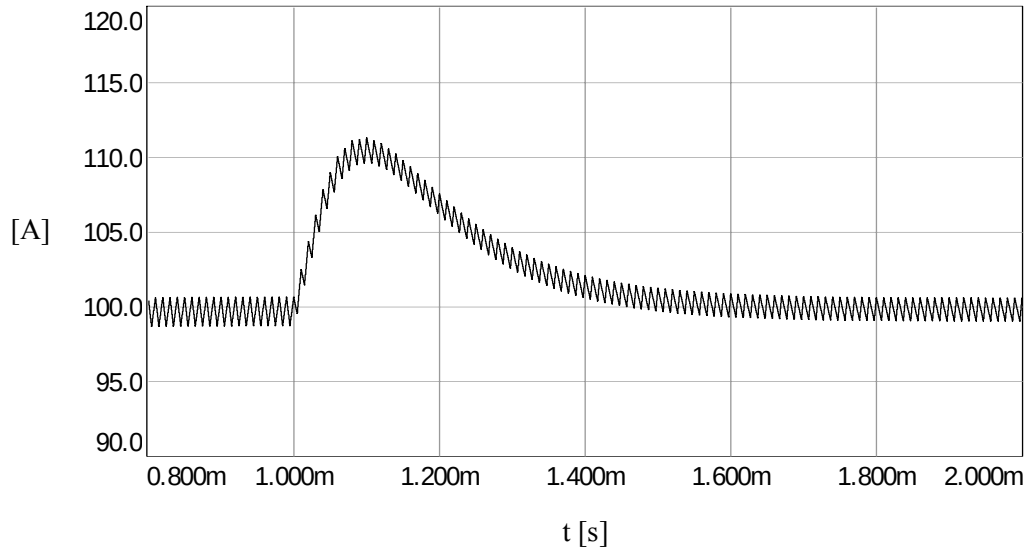


Figure 5.29 Load regulation performance of the output current controller.

In order to investigate the dynamic performance of the welding power supply, the load arc must be modeled in the system simulation. Due to the complex, nonlinear characteristic of the arc resistance, a detailed model could not be employed. Also it has been found that there is lack of literature on the subject. Since a detailed and precise model could not be found, a simplified arc load model has been utilized in the simulation. In the simulations, the arc load is modeled by a varying resistance.

The controller performance is tested by simulating the arc load behavior approximately as a varying resistance. The open-circuit, rated load and short-circuit conditions are modeled by applying the corresponding load resistance in a specified time interval. The computer simulations are carried out by utilizing the system level model for all the switches to substantially reduce the simulation time, where the switching dynamics are not essential for the simulations that investigate the controller performance. First, the load is assumed to be open-circuit for 2 ms and the load is modeled with a large resistance (50 MΩ). Then, the system is loaded to its rated value gradually in 2 ms to emulate the continuous time loading behavior. The rated load resistance is 0.5 Ω. Then, the system is operated at rated load condition for 3 ms. For the sake of brevity, this time interval is selected too short with respect to

the practical operating conditions (in practice which take more than a few seconds) since the output settles and remains at the rated values during this time interval. To show the controller performance near the short-circuit load condition, the load resistance is linearly reduced from 0.5 Ω to 0.1 Ω in a time interval of 2 ms. This operation emulates the welding condition, where the electrode of the arc welding machine sticks to the workpiece for a short time interval. Then, the load is increased to its rated value again in 2 ms and operated under rated condition for 3 ms. The load is removed gradually again in 2 ms and it is open-circuited finally. The corresponding load resistance waveform is given in Figure 5.30.a, where the open-circuit resistance between the time intervals 0-4 ms and 14-18 ms is not shown in this figure since the corresponding resistance value of 50 MΩ is relatively large. The described welding cycle has been simulated and the control performance has been investigated. Figure 5.30.b shows the output voltage and current during a welding cycle. As the figure demonstrates, the load current remains practically constant during the welding cycle, which yields a high quality weld with constant current. Also at the start-up and completion transitions, the current controller response is high and stable (unoscillatory). The high frequency operation of the DC/DC converter at 50 kHz allows for a bandwidth of 2.5 kHz that is sufficient to manipulate all the dynamics and provide satisfactory steady-state behavior. Digital control of the system at high frequency sampling and PWM yields nearly as good as typical analog controllers. It should be noted that the load resistance model variation is not adopted for in the controller and thus the controller response is not optimal. An adaptive controller or alternative method could be utilized to further enhance the control performance of the system. This issue is left as future work.

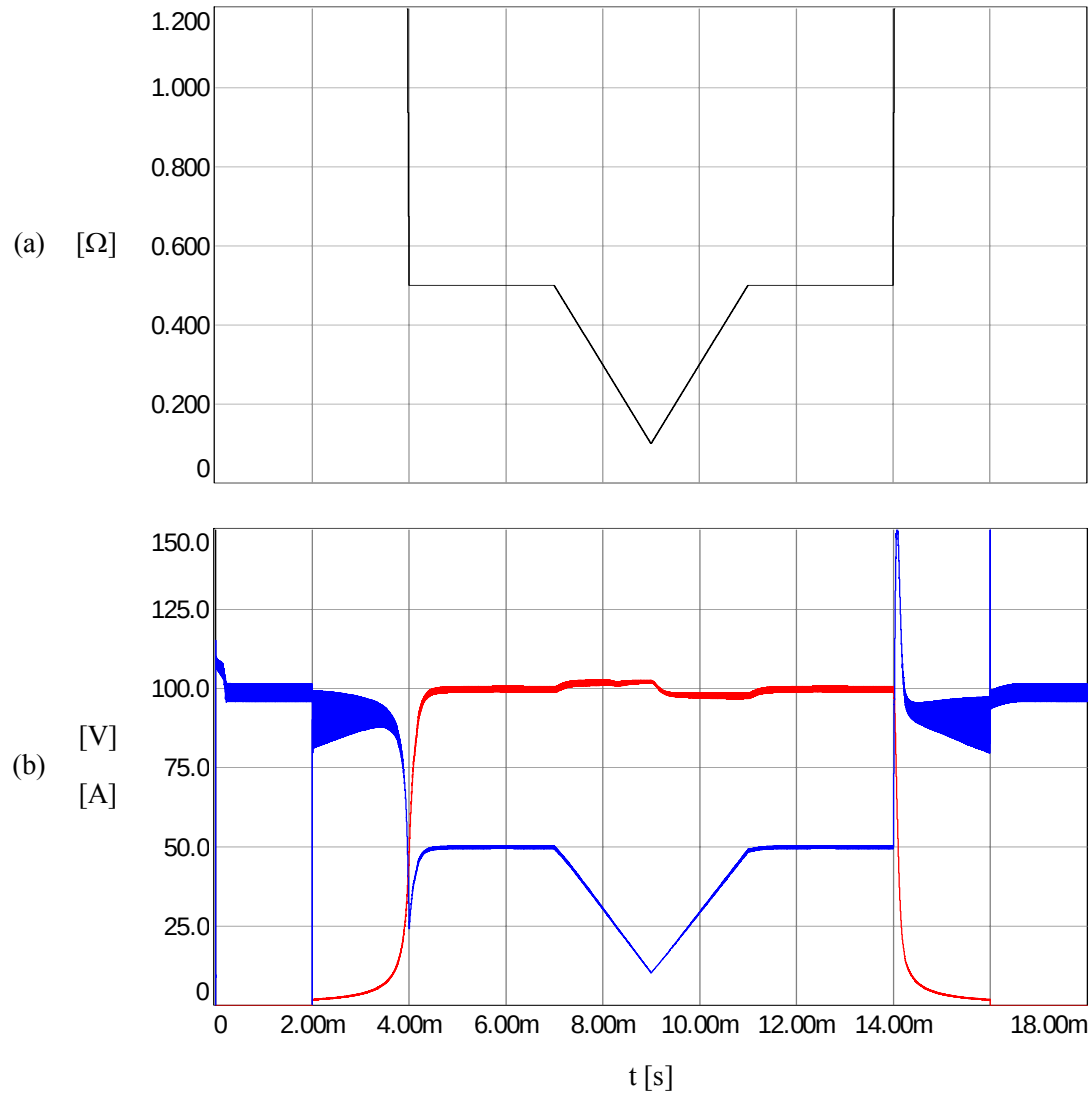


Figure 5.30 The varying load resistance waveform (a) and the output voltage (blue) and output current (red) waveforms (b) simulating the welding process.

In this chapter, the ZVS performance of the switches, power converter efficiency, and output current controller performance are investigated by means of computer simulations. Thus, the analytical converter design of Chapter 4 has been verified. Since detailed modeling of all the critical components is covered, the simulation study provides highly reliable results in terms of basic behavior and operating characteristics. However, the practical application involves further second and third

order effects (such as switch parasitics, characteristics, transformer capacitance etc.), which could only be investigated by means of laboratory experiments. In the following chapter, the manufactured converter system is described and the obtained experimental results are presented to verify the performance of the designed and performance investigated converter.

CHAPTER 6

EXPERIMENTAL RESULTS OF THE FB-PS-ZVS DC/DC CONVERTER

6.1 Introduction

This chapter experimentally investigates the performance of the FB-PS-ZVS DC/DC converter designed in Chapter 4 and performance predicted in Chapter 5. In this chapter, first the manufacturing of the 5 kW FB-PS-ZVS DC/DC converter prototype is explained in detail. Then, the experimental test procedure is described and experimental results, which show the switching performance of the power converter, the efficiency of the converter system, and the output current regulation performance of the controller, are reported. The experimental results are evaluated and compared with the analytical results of Chapter 4 and computer simulation results of Chapter 5 and strong correlation between the theory and experiments is shown.

6.2 Hardware Implementation of The 5 kW FB-PS-ZVS DC/DC Converter

The designed 5 kW FB-PS-ZVS DC/DC converter system is constructed at METU Electrical and Electronics Engineering Department, in the Electrical Machines and Power Electronics Laboratory as a prototype and an experimental setup is established. The block diagram of the experimental setup is given in Figure 6.1. The electrical power circuitry of the overall system is shown in Figure 6.2.

The laboratory AC voltage source, which is a three-phase 380 V, 50 Hz AC utility grid, is applied to a three-phase variable transformer. The output of the variable transformer feeds a three-phase uncontrollable rectifier, and it is adjusted to a value such that a DC voltage of 400 V is obtained at the rectifier output terminals. This

voltage is applied to the input of the FB-PS-ZVS DC/DC converter. Modern single-phase input type welding machines include a front-end boost PFC converter that outputs 400 V DC bus voltage from a rectified single-phase 220 V AC line. To emulate the 400 V DC bus voltage operating condition, the variable transformer is adjusted to generate 170 V_{rms} AC voltage per phase. At the variable transformer output, a three-phase 20 A automatic fuse, a three-phase 25 A circuit breaker, and a three-phase AC line smoothing reactor (L_S = 2.3 mH/phase, 20 A rms current rating), which lowers the distortion of the input current waveform, are employed. The obtained AC voltage is converted to DC voltage by a 1600 V, 100 A three-phase full-bridge diode rectifier. Two bulk capacitors (C_{DC}), having 2200 μF capacitance, 450 V DC voltage rating, and 10.7 A rms current rating each, are connected in series to form the DC bus of the FB-PS-ZVS DC/DC converter system. The bleeding resistors (R_B), which discharge the DC bus capacitors when the converter system is shut-down and balance the charges of these capacitors under normal operating conditions, are connected across the DC bus capacitors. Each utilized bleeding resistor has a resistance value of 30 kΩ and a power rating of 10 W. To prevent hazards during a short-circuit case on the DC bus, a 20 A fast fuse is inserted between the positive terminals of the diode rectifier and the DC bus capacitor bank.

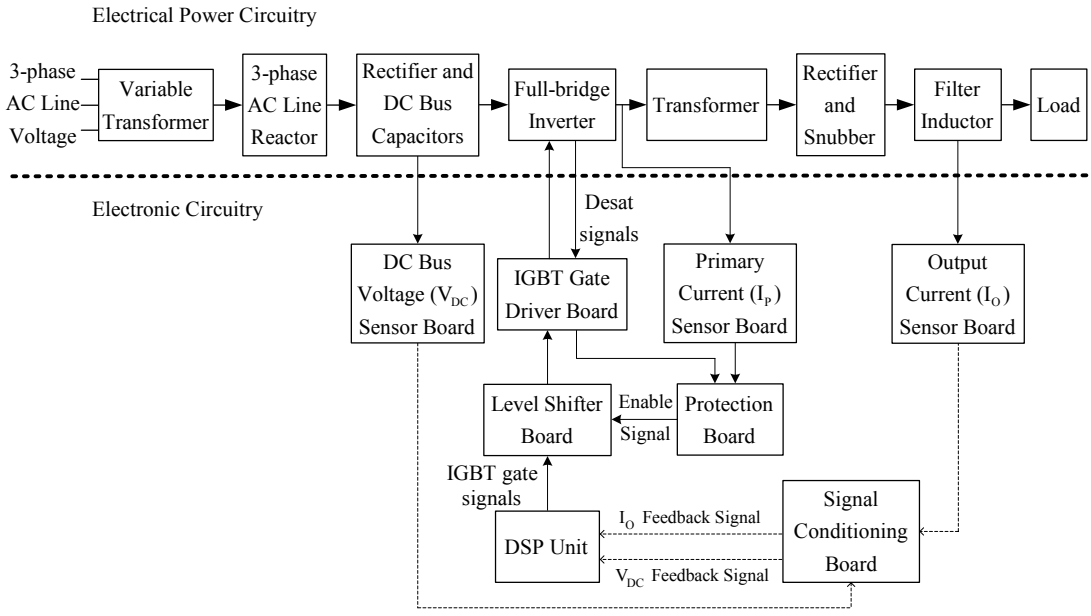


Figure 6.1 The basic system block diagram of the experimental setup.

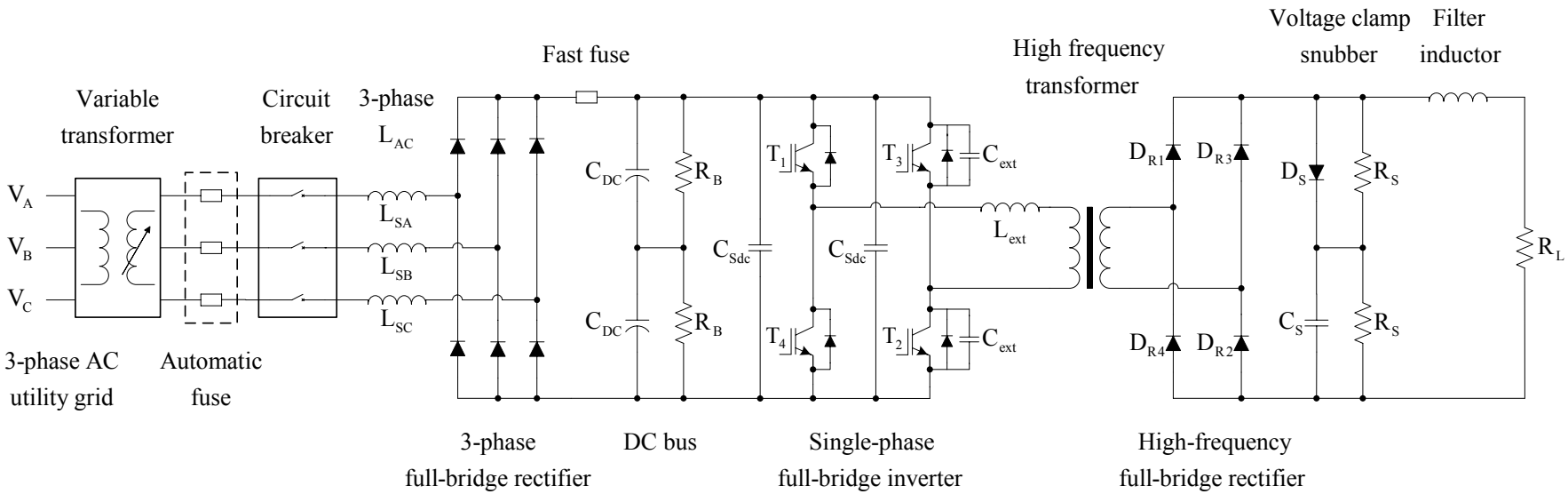


Figure 6.2 The electrical power circuitry of the overall system.

The full-bridge inverter of the FB-PS-ZVS DC/DC converter consists of two dual-pack IGBT modules, the SKM 100GB125DN model modules manufactured by Semikron. Table 5.1 (given in Chapter 5) summarizes the basic specifications of this IGBT module. The gate driver module for the IGBTs is 2SD106AN model module manufactured by Concept [19]. The basic specifications of this gate driver module, which drives both switches in each IGBT module, are given in Table 6.1. The gate driver board, which includes two gate driver modules, converts a PWM signal with +15/0 voltage levels to an isolated and amplified +15/-15 voltage levels, which is required for the IGBT turn-on and turn-off operations. The gate driver board outputs +15 V during the conduction interval of the IGBT and it applies -15 V to the gate terminal of the IGBT during the off interval to fully discharge the stored gate charge, guaranteeing the turn-off operation of the IGBT. While the gate driver module generates the gate voltage for the IGBTs, it also monitors the collector-emitter voltage for short-circuit failure condition. While the IGBT is conducting, if the collector-emitter voltage of the IGBT is higher than the preset desaturation limit voltage value, which is slightly larger than V_{CEsat}, the gate driver module turns off the IGBT and outputs an error signal to the protection board (the desat signal). The gate driver module applies the gate voltage to the IGBT gate terminals via a series gate resistor having a value of 12 Ω.

Table 6.1 Specifications of the gate driver module utilized in the implemented converter system

Concept 2SD106AN Gate Driver Module		
V_S	Supply voltage primary side	15 V
I_{SO}	Supply current primary side (no-load/maximum)	23/153 mA
P_{OGD}	Gate driver output power	2 W
V_{IT+}	Input threshold voltage (High)	11.5 V
V_{IT-}	Input threshold voltage (Low)	0.7 V
V_I	Input signal voltage ON/OFF	15/0 V
$V_{G(ON)}$	Turn-on gate voltage output	+15 V
$V_{G(OFF)}$	Turn-off gate voltage output	-15 V
I_G	Gate driver output current (minimum/maximum)	-6/6 A

As discussed in Chapter 4, additional resonant components are included in the converter. An additional capacitor (C_{ext}) of 4.7 nF is inserted across each IGBT of the lagging leg and an additional inductor (L_{ext}) having a value of 23 μH is connected in series with the full-bridge inverter output. This additional inductor is manufactured by utilizing E-80 Kool-Mu magnetic core (manufactured by Magnetics [13]) that has a relative permeability value of 26. The required inductance of 23 μH is provided by winding 15 turns of copper litz wire around the E-80 core.

IGBTs are mounted on a 99AS model heatsink and aluminum plates are mounted on the IGBTs using spacers and an insulation layer in between. The DC bus of the full-bridge inverter is constructed by utilizing a planar bus structure to obtain low parasitic inductance on the DC bus. Two aluminum plates are mounted to the inverter for positive and negative DC bus rails. Between these plates an insulation material having an insulation level of 10 kV is inserted. A snubber capacitor (C_{Sdc}) for each IGBT module is inserted across the DC bus terminals of the IGBT module. Thus, the switching stress on the IGBTs due to the DC bus stray inductance is reduced. The utilized snubber capacitors in the inverter have a 220 nF capacitance and 1000 V voltage rating.

The high frequency isolation transformer utilized in the DC/DC converter system was described in detail including the analysis, design, manufacture, and characterization steps in Chapter 4. The full-bridge rectifier diodes at the secondary side have to be fast and need to have low reverse recovery current and reverse recovery time in order to rectify the high frequency (50 kHz) AC voltage. Also low forward voltage drop is required to reduce the conduction loss and output voltage drop. Considering these requirements, the APT2x61S20J model high voltage Schottky diode modules manufactured by APT are utilized in the high frequency full-bridge diode rectifier. The basic specifications of each diode in this module, which includes two independent diodes, are summarized in Table 6.2. To form the high frequency full-bridge rectifier four diode modules are utilized. The diodes of each module are paralleled in order to obtain an equivalent diode with high current capability. Since each diode has 75 A average rating, the equivalent diode has 150 A

rating. Four modules are connected in the conventional full-bridge connection and mounted on a separate heatsink to form the high frequency rectifier.

Table 6.2 Specifications of the diode module utilized
in the high frequency full-bridge rectifier

APT2x61S20J Schottky Diode Module (per diode of the two pack)		
V_{RM}	Maximum DC reverse voltage	200 V
I_{FAVM}	Maximum average forward current	75 A
V_F	Forward voltage	0.83 V
t_{rr}	Reverse recovery time	55 ns
Q_{rr}	Reverse recovery charge	160 nC
I_{RRM}	Maximum reverse recovery current	5 A
C_T	Junction capacitance, V_R = 200 V	300 pF

An RCD type voltage clamp snubber, which clamps the transformer secondary voltage, is employed at the output of the high frequency full-bridge diode rectifier. The transformer secondary voltage oscillates due to the resonance between the secondary referred transformer leakage inductance and additional external inductance, and the high-frequency rectifier diode junction capacitances and transformer winding capacitance. Due to the resulting large voltage peaks, the voltage clamp snubber is utilized to suppress the overvoltage. The operation of this snubber was discussed in Chapter 5. In this voltage clamp snubber, the resistors having a value of 10 kΩ and a power rating of 10 W, and a capacitor having 100 nF capacitance and 1200 V DC voltage rating are employed. The diode utilized in the voltage clamp snubber is DSEP 8-02A manufactured by IXYS and the basic specifications of this fast recovery diode are summarized in Table 6.3. In the following section the voltage suppressing effect of this voltage clamp snubber is explained with the assistance of experimental results. The filter inductor in the experimental system is a parallel combination of 4 ferrite cored inductors, each having 500 μH inductance value and a current carrying capacity of 30 A, which are available in the laboratory. Thus, the load current is filtered by utilizing an equivalent

inductance of 125 μH. At the output the adjustable resistive load banks, which can be adjusted such that they have an equivalent resistance of 0.55 Ω (the rated load), are employed for the load. Also, manual switches are connected with the load bank for loading transient tests.

Table 6.3 Specifications of the diode utilized in the voltage clamp snubber

DSEP 8-02A Diode		
V_{RM}	Maximum DC reverse voltage	200 V
I_{FAVM}	Maximum average forward current	8 A
V_F	Forward voltage	0.94 V
t_{rr}	Reverse recovery time	25 ns
I_{RRM}	Maximum reverse recovery current	4.1 A

In the FB-PS-ZVS DC/DC converter system, the output current, DC bus voltage and transformer primary current are measured for control and protection purposes. The DC bus voltage of the full-bridge inverter is measured by utilizing the hall-effect based isolated voltage sensor, LV25-P model manufactured by LEM. The transformer primary current and the load current are measured by utilizing hall-effect current sensors, which are LA 55-P/SP1 and LA 100-P manufactured by LEM. The DC bus voltage and output current sensor outputs are scaled and filtered by utilizing basic operational amplifier circuits and passive noise filters in the signal conditioning board. This board provides the DC bus voltage and load current feedback signals at the required voltage level (between 0 and 3 V) for the Digital Signal Processor (DSP) unit. The transformer primary current measurement is utilized only for overcurrent protection of the IGBT modules. The scaled and filtered transformer primary current sensor output, which is also the overcurrent signal, is supplied to the protection board. The protection board monitors the overcurrent and desat signals and if an error does not occur, it enables the IGBT gate signals to be applied to the IGBT gate driver board. If a fault occurs, all IGBT gate signals are set to 0, where the converter operates in base block state (transistor base signals are set negative so the transistors remain in cut-off state).

To implement the output current control function and generate the required IGBT gate signals, a DSP unit is utilized in the experimental system. In the DSP unit, analog to digital (A/D) conversion, control block calculation, and PWM output signal generation functions are carried out. The DSP unit is chosen as the eZdsp F2808 starter kit manufactured by Spectrum Digital, which includes the TMS320F2808 DSP manufactured by Texas Instruments. Table 6.4 summarizes the main features of TMS320F2808 DSP [20]. Two PWM modules of the DSP unit, "EPWM1" and "EPWM2", are utilized to generate the PWM signals for the IGBTs of the two inverter legs. Each PWM module includes two PWM signal outputs "EPWMxA" and "EPWMxB", where "x" is utilized for 6 PWM modules of TMS320F2808 DSP unit.

Table 6.4 Main features of the TMS320F2808 DSP

Operating Frequency	100 MHz
Clock and System Control	• On-Chip Oscillator • Dynamic PLL Ratio Changes Supported • Watchdog Timer
Central Processing Unit (CPU)	32-bit high performance CPU
On-Chip Memory	• 64K×16 Flash Memory • 18K×16 RAM • 1K×16 One-Time Programmable ROM
Timers	Three 32-Bit CPU Timers
Enhanced Control Peripherals	• 16 PWM Outputs • 4 Capture Inputs • 2 Quadrature Encoder Interfaces
Analog-Digital Converter (ADC)	• 12-Bit ADC • 16 Channels • Conversion Rate: 160 ns/6.25 MSPS
General Purpose Input/Output	Up to 35 Multiplexed GPIO Pins
Serial Port Peripherals	• 4 Serial Peripheral Interface Modules • 2 Serial Communication Interface Modules • 2 Controller Area Network Modules • 1 Inter-Integrated-Circuit Bus

The counters of the utilized EPWM modules are set to a maximum value of 2000, since the DSP system clock is 10 ns while the switching period is 20 μs. The constant duty cycle value of 1000, which corresponds to %50 duty cycle, is loaded to the

compare register. While the EPWMxA compare register value is higher than the counter value of the EPWM module, EPWMxA signal is high otherwise it is low. EPWMxB signal set to be active high complementary of the EPWMxA signal. Between the complementary PWM signals, also a dead-time is inserted. As determined in Chapter 4, the dead-time between the switches in the same inverter leg is 0.9 μs, which corresponds to 90 cycles of the system clock. The control algorithm implemented in the DSP unit is executed once in every switching cycle. When the counter of the PWM module EPWM1 is zero, an interrupt, which starts the control program execution, is generated. After the program execution is finished, DSP unit waits for another interrupt to execute the control program again. In the implemented code, which is written in C programming language, one interrupt is generated in every switching period. The execution of the program code starts with the A/D conversion of the control variables (I_O and V_{DC}) after the generation of an interrupt. Then, the reference duty cycle value is calculated by utilizing the measured and reference value of the load current, and performing the control tasks. Since the phase-shift angle (ϕ), which is introduced between the EPWM1 and EPWM2 counters, is the control variable in the phase-shifted PWM method, the calculated reference duty cycle value is converted to the corresponding phase-shift angle, where their relationship is given in equation (3.1) in Chapter 3. TMS320F2808 DSP has a phase register for each EPWM module which determines the phase-shift between the counters of these EPWM modules. By disabling the phase register of the EPWM1 module, the calculated phase-shift is loaded at the end of the program code to the phase register of the EPWM2 module, which is synchronized to the EPWM1 counter. Any change in the phase register of the EPWM2 module is applied to the output PWM signals at the next switching cycle. The utilized phase-shifted PWM method in the DSP unit, which is discussed so far, is illustrated in Figure 6.3.

Since the high logic voltage level of the PWM signal output of the DSP unit is 3.3V, it must be increased to the required voltage level for the gate driver modules, which is 15 V. Due to this reason, a level shifter electronic circuit board, which shifts the high logic voltage level from 3.3 V to 15 V, is utilized in the manufactured system. Increasing the high logic signal level from 3.3 V to 15 V provides higher Signal to

Noise Ratio (SNR), which results in better noise immunity. The PWM signals are transferred from the DSP unit to the gate driver board via the level shifter, if the protection board enables the level shifter to operate. If an error (either overcurrent or desat) occurs in the converter system, the output signals of the level shifter board are all set to low voltage level (0 V) due to the disable signal generated by the protection board, while the DSP unit continues to output PWM signals. The PWM signal output of the level shifter board is applied to the gate driver board that is discussed before.

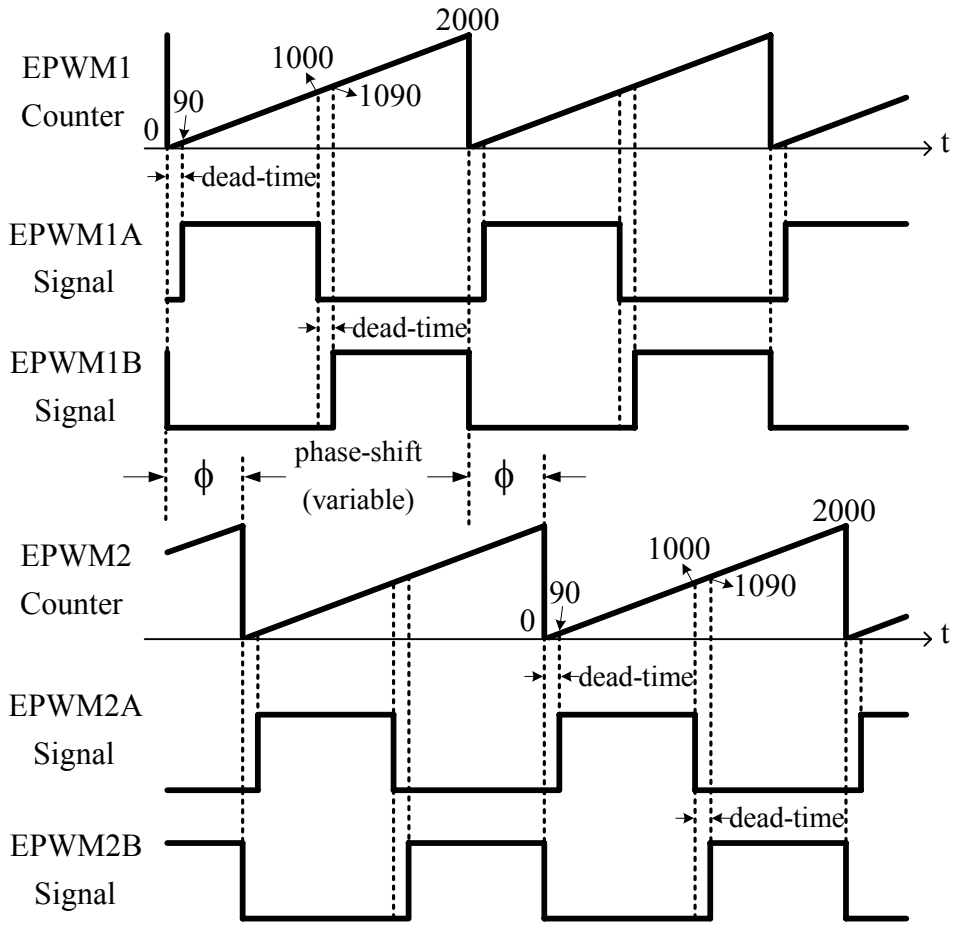


Figure 6.3 The utilized phase-shifted PWM scheme in the DSP unit.

In Figure 6.4 the photograph of the laboratory prototype FB-PS-ZVS DC/DC converter is shown, and the whole laboratory set-up of the FB-PS-ZVS DC/DC converter system is photographed in Figure 6.5.

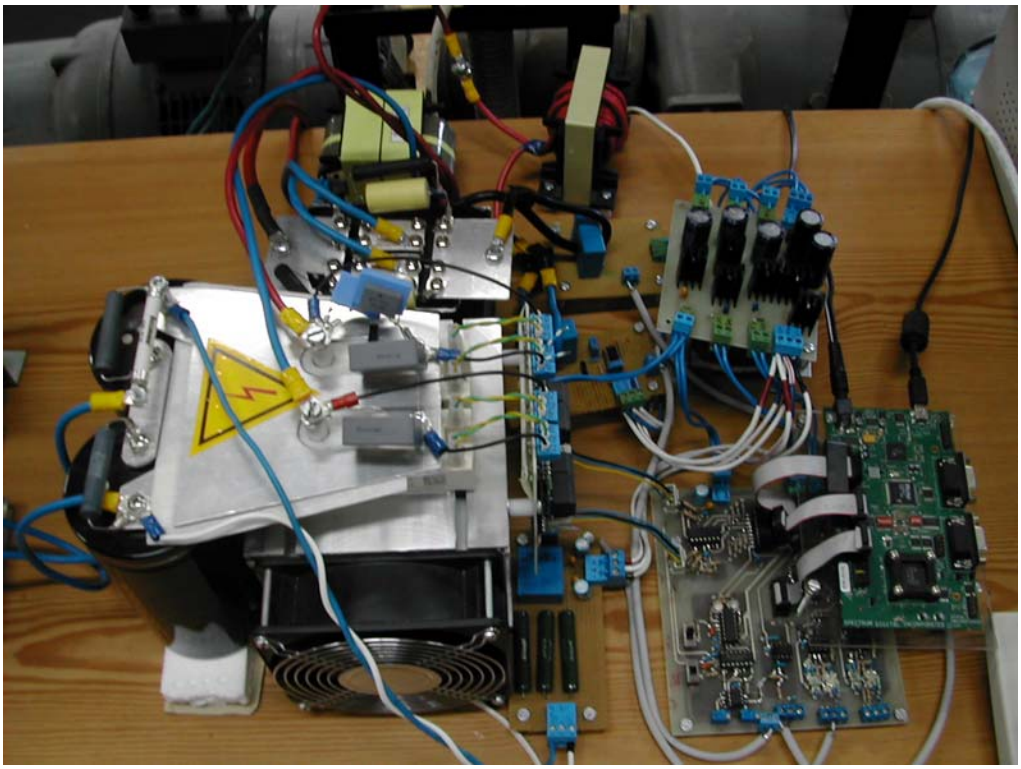


Figure 6.4 Laboratory prototype of the FB-PS-ZVS DC/DC converter.

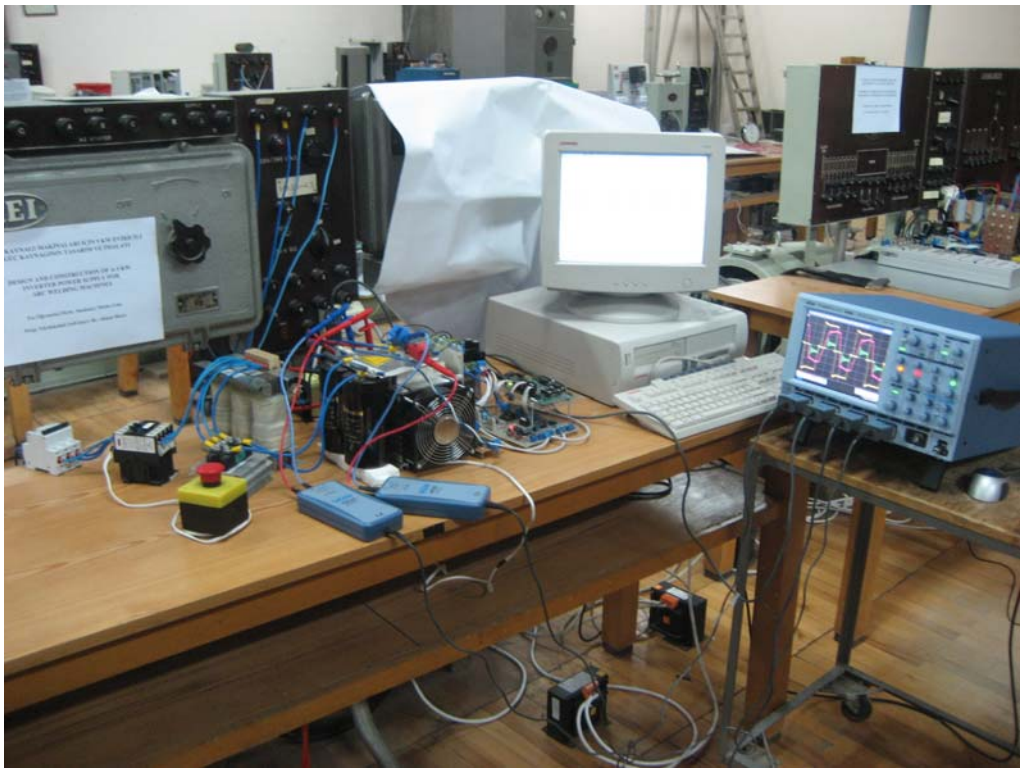


Figure 6.5 Laboratory prototype of the FB-PS-ZVS DC/DC converter system set-up.

6.3 Experimental Results

In this section, the FB-PS-ZVS DC/DC converter experimental results are presented. First, the experimental results of the converter are shown for the rated load, critical load (ZVS boundary) and under light load (hard-switching) conditions. Each experiment is carried out by applying the corresponding reference current command for the specified load conditions. After the performance of the voltage clamp snubber is investigated in detail, the measured efficiency of the FB-PS-ZVS DC/DC converter system at different load current values is given and compared with the efficiencies calculated and estimated from the computer simulation results. Then, the performance of the output current controller is verified by the experimental results, which are obtained by changing the output current command and load resistance.

6.3.1 The FB-PS-ZVS DC/DC Power Converter Experimental Results for Various Load Current Levels

6.3.1.1 Experimental Results at The Rated Load Current (100 A)

In this part, the experimental results, which show the performance of the designed and manufactured FB-PS-ZVS DC/DC power converter, are presented for the 100 A rated load current condition. In Figure 6.6, the inverter output voltage, transformer primary current, and transformer secondary voltage waveforms are shown. The obtained steady-state waveforms at the rated load current are similar to the computer simulation results shown in Chapter 5. The transformer secondary voltage and secondary current waveforms are shown in Figure 6.7. As can be observed in this figure, the transformer secondary voltage waveform oscillates due to the resonance between the secondary referred transformer leakage inductance and additional external inductance, and the high-frequency rectifier diode junction capacitances and transformer winding capacitance. From Figure 6.7, it can be observed that the oscillation period is 600 ns and the transformer secondary voltage is clamped to 150 V by the voltage clamp snubber. The utilized voltage clamp snubbers and their effects are described in detail experimental results in the following subsection.

Figure 6.6 Inverter output voltage (yellow), transformer primary current (blue), and transformer secondary voltage (red) waveforms at the rated load current (scales: 120 V/div, 15 A/div, 120 V/div, 3 µs/div).

Figure 6.7 Transformer secondary voltage (yellow) and secondary current (red) waveforms at the rated load current (scales: 50 V/div, 30 A/div, 3 µs/div).

In Figure 6.8 the load current waveform, which has a DC value of 100 A, is shown with its zoomed version. The peak-to-peak load current ripple is measured approximately between 1.5 A and 2 A, where it is obtained as 1.8 A from the computer simulation result shown in Chapter 5.

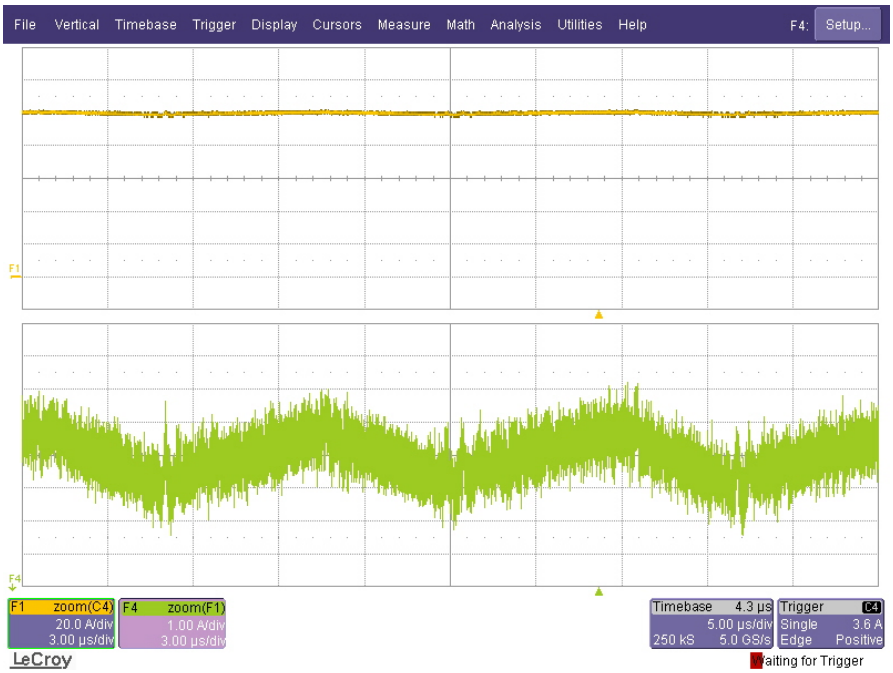


Figure 6.8 Load current waveform (top) and its vertically zoomed version (bottom) at the rated load current (scales: 20 A/div, 1 A/div, 3 µs/div).

Figures 6.9 and 6.10 are given to observe the turn-on and turn-off switching performance of the leading and lagging leg IGBTs (T_4 and T_2), respectively. In these figures, the gate-emitter voltage is shown as an indicator for the ZVS turn-on instead of the IGBT collector current since the collector current could not be observed due to unavailability of the required current measurement node in the manufactured converter. As can be observed in both figures, the ZVS turn-on is satisfied since the gate-emitter voltage rises after the voltage across the IGBT is reduced to zero.

The gate-emitter voltage of the leading and lagging leg IGBTs oscillate while both of the IGBTs are conducting simultaneously as can be observed from the Figures 6.9 and 6.10. The oscillations on the gate-emitter voltages start when the transformer secondary voltage rises. The resonance between the circuit component parasitics (diode and transformer capacitive parasitic components) at the secondary side causes the oscillations on the transformer secondary voltage waveform as previously described and showed. Thus, the gate-emitter voltages are affected from this resonance, which results in these oscillations during the power transfer interval (in Mode 0 or 5).

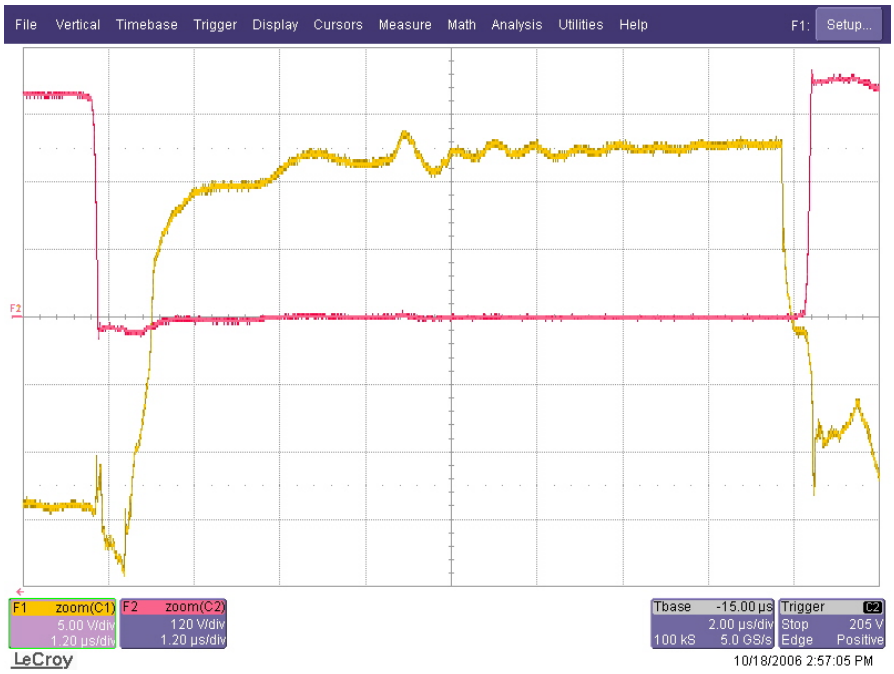


Figure 6.9 Collector-emitter voltage (red) and gate-emitter voltage (yellow) waveforms of the leading leg IGBT (T_4) at the rated load current (scales: 120 V/div, 5 V/div, 1.2 µs/div).

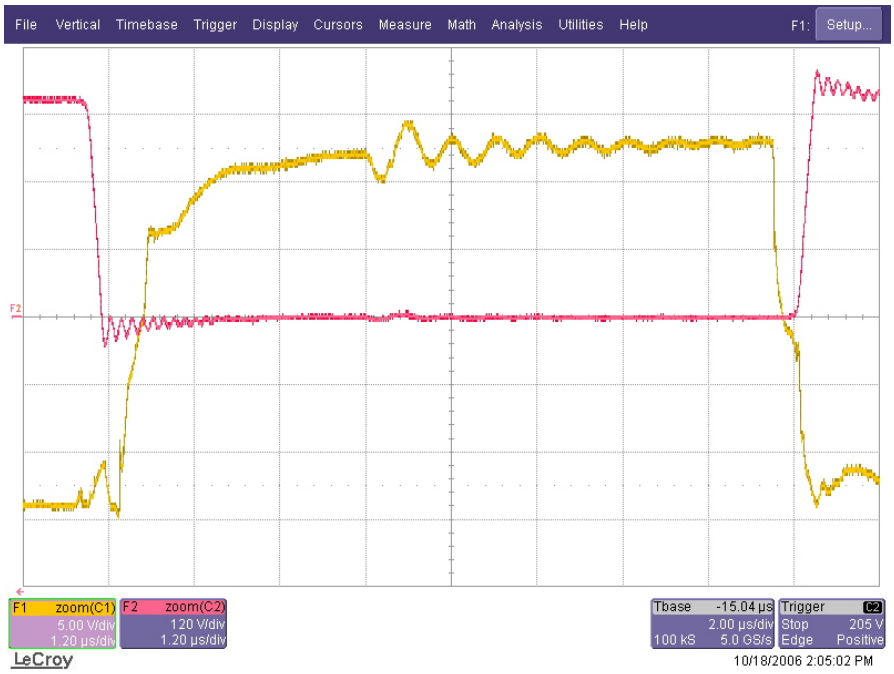


Figure 6.10 Collector-emitter voltage (red) and gate-emitter voltage (yellow) waveforms of the lagging leg IGBT (T_2) at the rated load current (scales: 120 V/div, 5 V/div, 1.2 µs/div).

6.3.1.2 Experimental Results at The Critical Load Current (35 A)

The experimental results, which show the performance of the designed and manufactured FB-PS-ZVS DC/DC power converter at the critical load current, are given in this part. The inverter output voltage, transformer primary current, and transformer secondary voltage waveforms are shown in Figure 6.11. The critical current value is obtained from the experimental work as 35 A, which is a similar result to the obtained computer simulation result in Chapter 5.

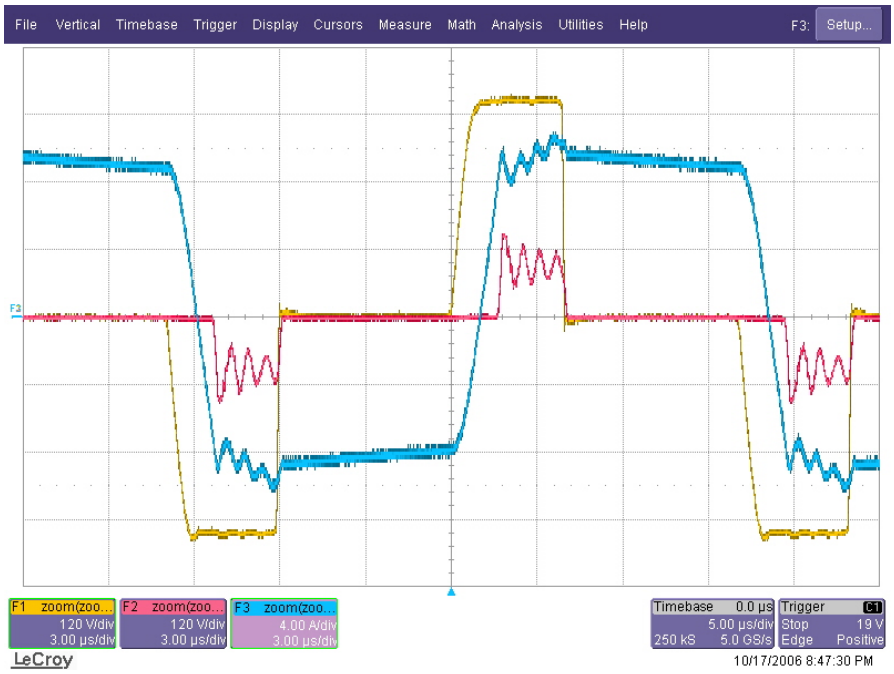


Figure 6.11 Inverter output voltage (yellow), transformer primary current (blue), and transformer secondary voltage (red) waveforms at the critical load current (scales: 120 V/div, 4 A/div, 120 V/div, 3 µs/div).

In the transformer primary current waveform, there exists a downward step during the leading leg transition (Mode 1) as can be observed in Figure 6.11. This sharp reduction occurs since the total of the load current and the magnetizing current discharge the junction capacitance of the nonconducting high frequency rectifier diodes and the stray capacitance of the transformer. Similarly, a downward step occurs in the transformer secondary current waveform as in Figure 6.12, which is given with the transformer secondary voltage waveform. The oscillations on the transformer primary and secondary current waveforms during the power transfer interval occur due to the formed oscillations on the secondary voltage.

Due to the downward step in the primary current waveform, the current value at the beginning of Mode 3 (lagging leg transition) is slightly lower than the calculated value in Chapter 4. Therefore, the obtained critical load current value from the experimental results (35 A) is larger than the calculated one (32 A).

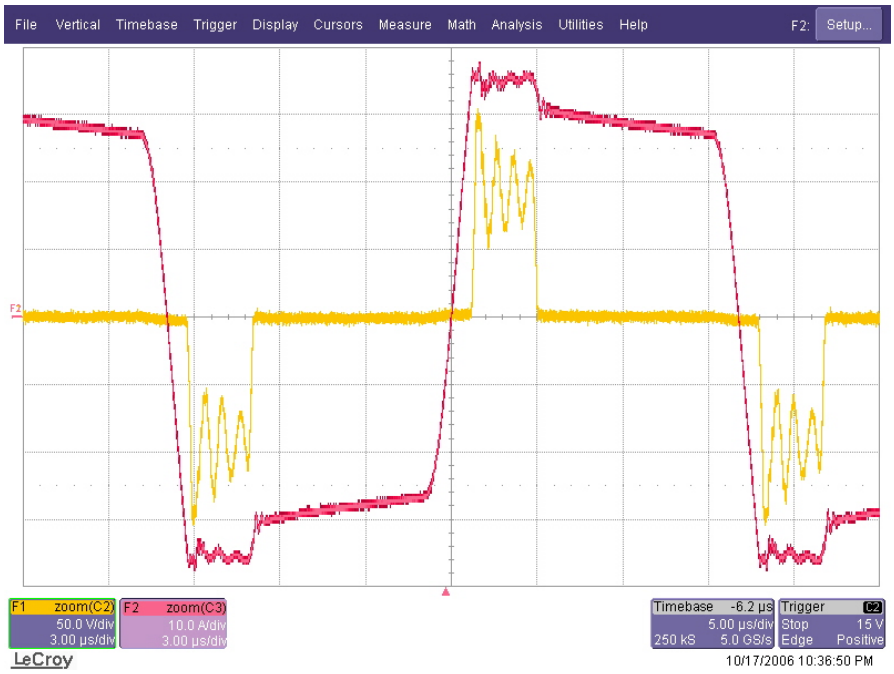


Figure 6.12 Transformer secondary voltage (yellow) and secondary current (red) waveforms at the critical load current (scales: 50 V/div, 10 A/div, 3 µs/div).

Figure 6.13 shows the load current waveform, which has a DC value of 35 A, and a peak-to-peak ripple value of 1.3 A, which is similar to the computer simulation results shown in Chapter 5. The oscillations on the rising portion of the load current waveform origin from the oscillations on the transformer secondary current waveform during the power transfer interval.

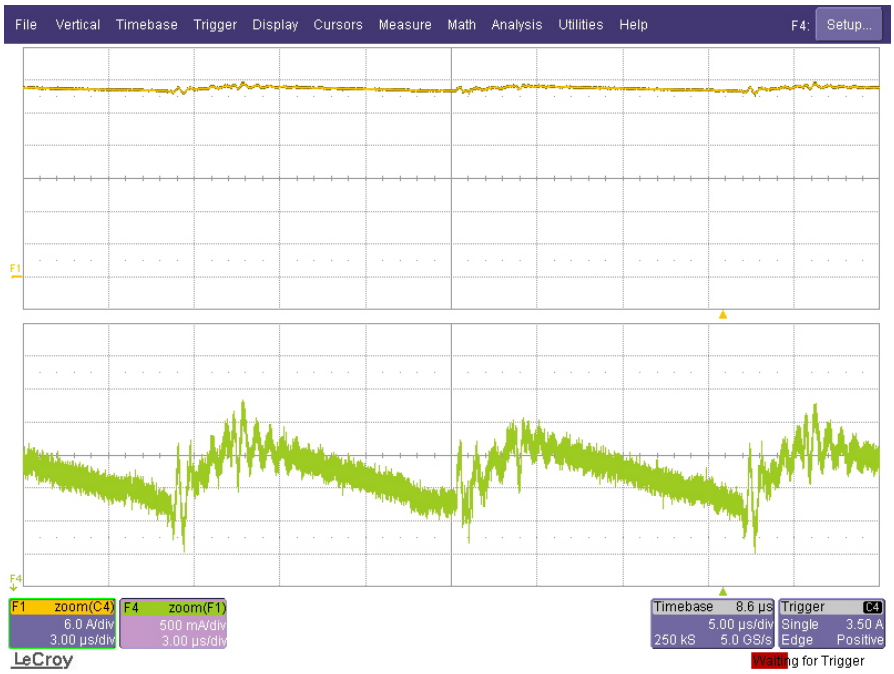


Figure 6.13 Load current waveform (top) and its vertically zoomed version (bottom) at the critical load current (scales: 6 A/div, 500 mA/div, 3 µs/div).

At the critical load current, the voltage across the leading leg IGBT (T_4) decreases to zero before the gate-emitter voltage of this IGBT rises as shown in Figure 6.14. However, the voltage across the lagging leg IGBT (T_2) has just decreased to zero before the gate-emitter voltage of this IGBT reaches to the threshold voltage value as can be observed in Figure 6.15. The gate-emitter threshold voltage, which is the required minimum voltage above which a considerable current flows through the IGBT, is measured as 7 V from this figure. Figure 6.16 is given also to observe the turn-on and turn-off switching transitions of the lagging leg IGBT in detail.

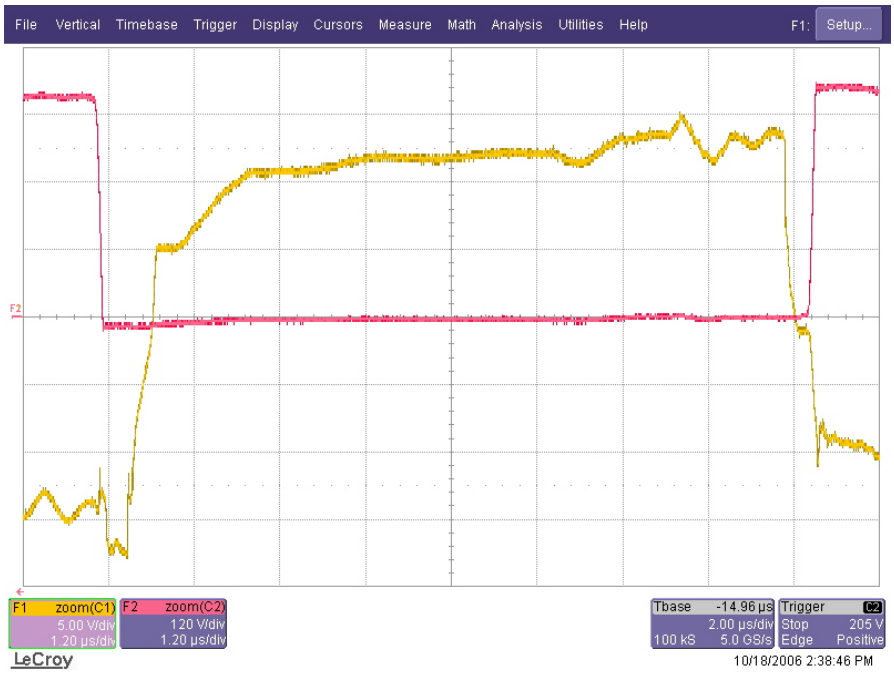


Figure 6.14 Collector-emitter voltage (red) and gate-emitter voltage (yellow) waveforms of the leading leg IGBT (T_4) at the critical load current (scales: 120 V/div, 5 V/div, 1.2 µs/div).

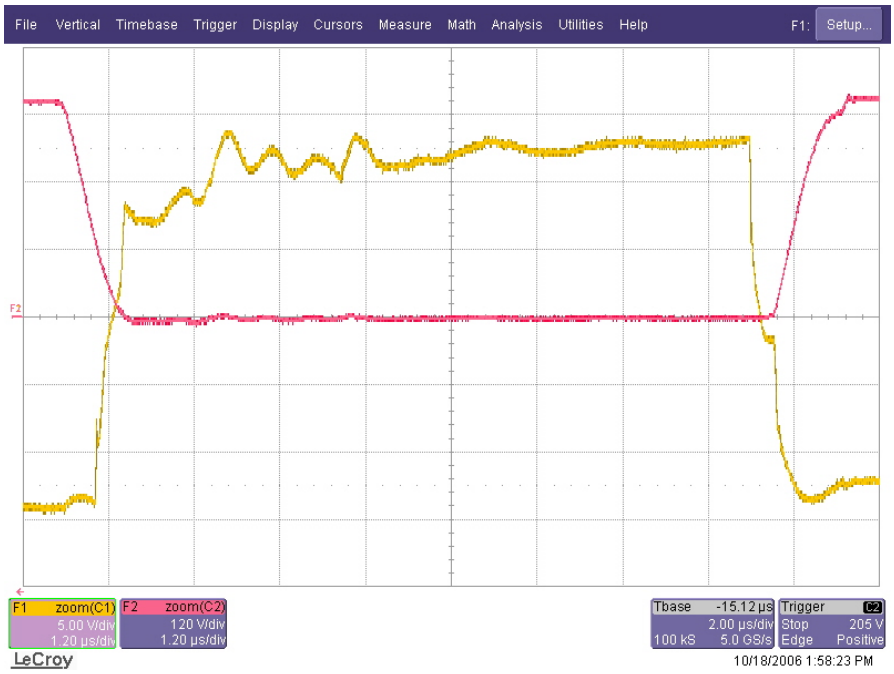


Figure 6.15 Collector-emitter voltage (red) and gate-emitter voltage (yellow) waveforms of the lagging leg IGBT (T_2) at the critical load current (scales: 120 V/div, 5 V/div, 1.2 µs/div).

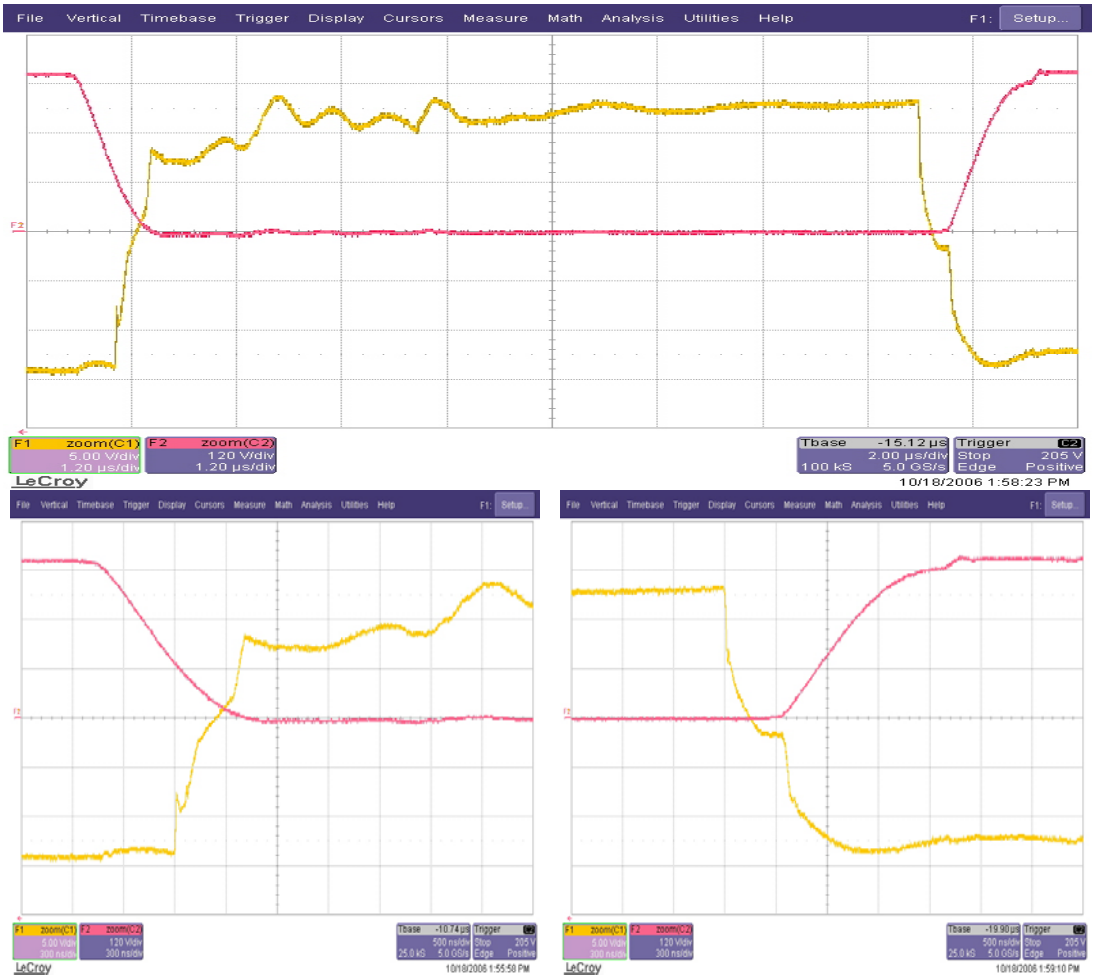


Figure 6.16 Collector-emitter voltage (red) and gate-emitter voltage (yellow) waveforms of the lagging leg IGBT (T_2) (top; scales: 120 V/div, 5 V/div, 1.2 µs/div), and the turn-on and turn-off switching transitions of this IGBT (bottom; scales: 120 V/div, 5 V/div, 300 ns/div) at the critical load current.

6.3.1.3 Experimental Results at 25% Load

So far the experimental results are given for two load conditions (rated and critical) satisfying the ZVS turn-on condition. In this and following part, the hard-switching behavior of the FB-PS-ZVS DC/DC converter is presented for 25% and 15% load.

The main power converter waveforms are given in Figures 6.17, 6.18, and 6.19 for the corresponding load current value of 25 A. Although the ZVS turn-on for the leading leg IGBT (T_4) is satisfied as shown in Figure 6.20, the lagging leg IGBT (T_2) turns on under hard-switching condition as can be observed in Figure 6.21.

Figure 6.17 Inverter output voltage (yellow), transformer primary current (blue), and transformer secondary voltage (red) waveforms at 25% load (scales: 120 V/div, 4 A/div, 120 V/div, 3 µs/div).

Figure 6.18 Transformer secondary voltage (yellow) and secondary current (red) waveforms at 25% load (scales: 50 V/div, 10 A/div, 3 µs/div).

Figure 6.19 Load current waveform (top) and its vertically zoomed version (bottom) at 25% load (scales: 5 A/div, 500 mA/div, 3 µs/div).

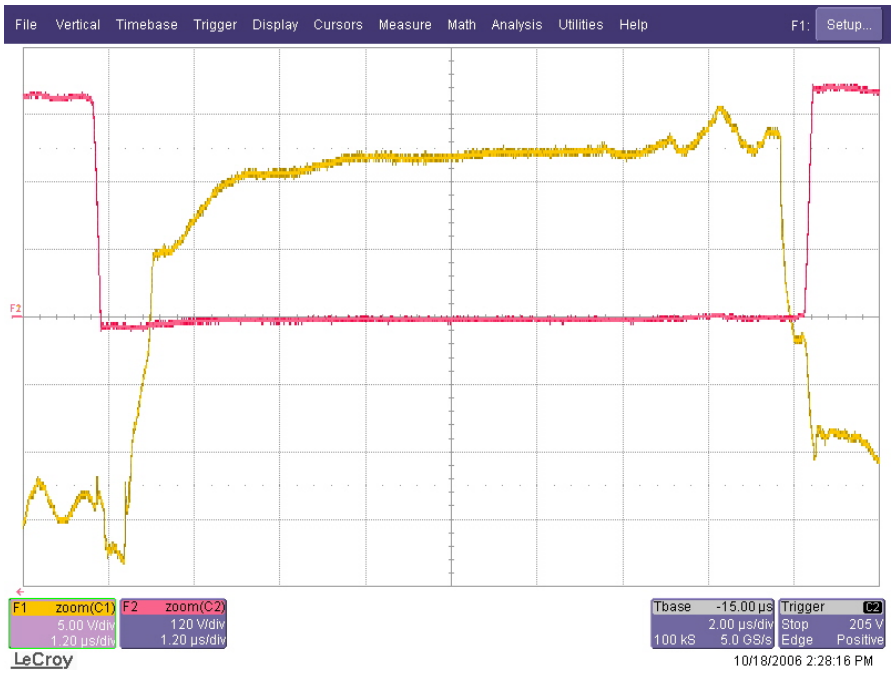


Figure 6.20 Collector-emitter voltage (red) and gate-emitter voltage (yellow) waveforms of the leading leg IGBT (T_4) at 25% load (scales: 120 V/div, 5 V/div, 1.2 µs/div).

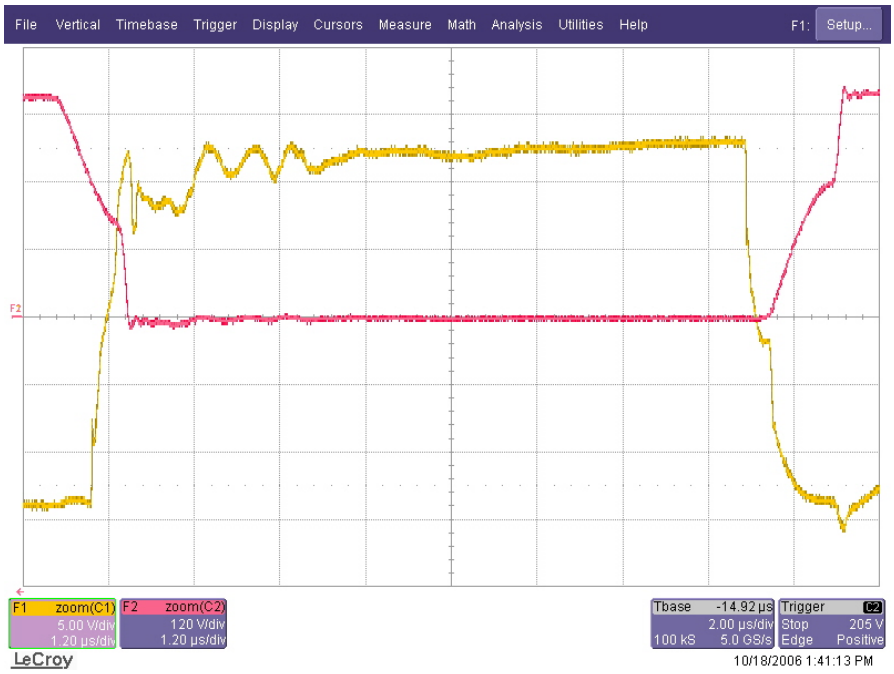


Figure 6.21 Collector-emitter voltage (red) and gate-emitter voltage (yellow) waveforms of the lagging leg IGBT (T_2) at 25% load (scales: 120 V/div, 5 V/div, 1.2 µs/div).

Since the load current value is below the critical load current value at 25% load condition, the total equivalent capacitance across the lagging leg IGBT could not be discharged completely as can be observed from the falling edge of the collector-emitter voltage waveform in Figure 6.21. The resonance operation, which discharges the total equivalent capacitance across the lagging leg IGBT at turn-on transition, ends when the primary current decreases to zero. Then, the gate-emitter voltage rises immediately and turns on the IGBT, while the collector-emitter voltage of the IGBT is decreasing faster than in the resonance operation, which results in the hard-switching turn-on condition. Figure 6.22, which also shows both switching transitions of the lagging leg IGBT, is given to observe the hard-switching condition in detail.

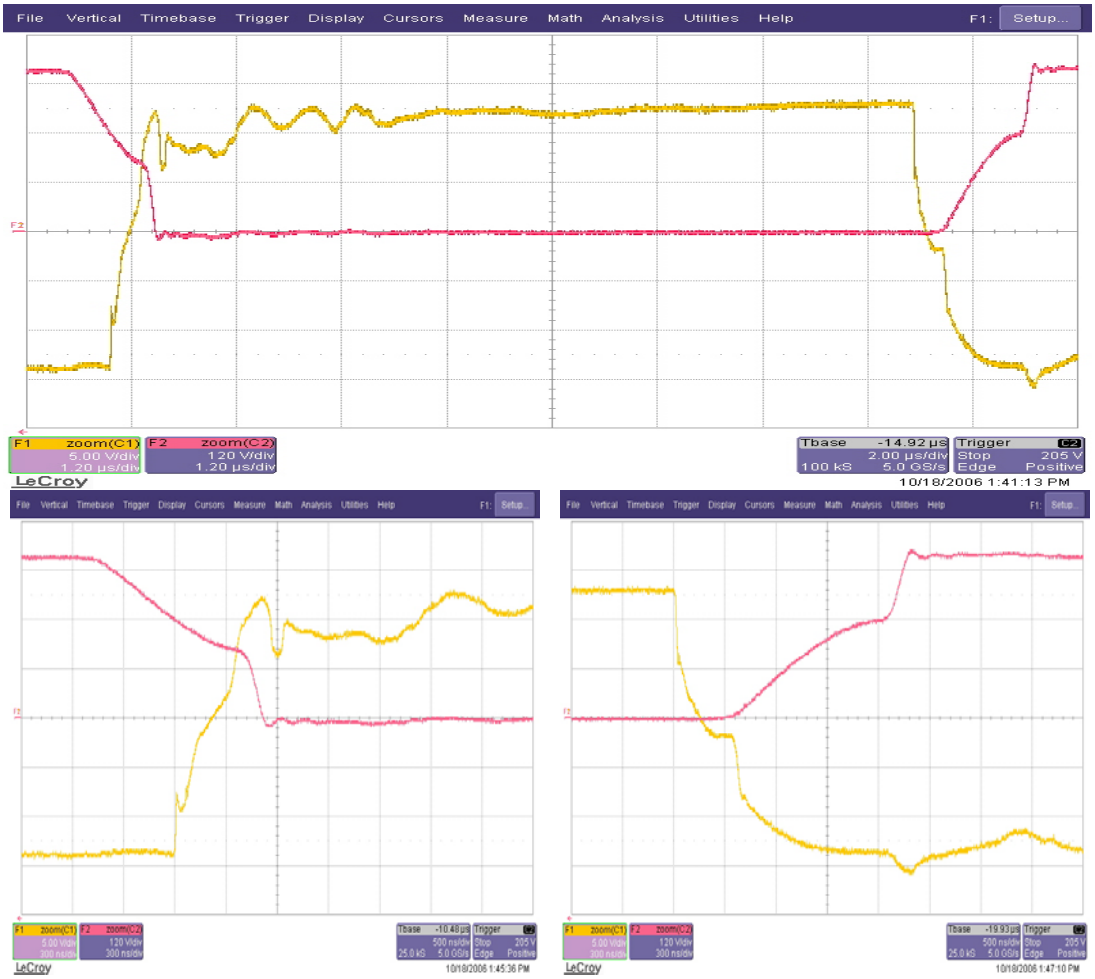


Figure 6.22 Collector-emitter voltage (red) and gate-emitter voltage (yellow) waveforms of the lagging leg IGBT (T_2) (top; scales: 120 V/div, 5 V/div, 1.2 µs/div), and the turn-on and turn-off switching transitions of this IGBT (bottom; scales: 120 V/div, 5 V/div, 300 ns/div) at 25% load.

6.3.1.4 Experimental Results at 15% Load

Finally, the experiments are carried out at a load current of 15 A, and the main power converter waveforms obtained from the experimental results are given in Figures 6.23, 6.24, and 6.25. The soft-switching and hard-switching turn-on operations of the leading and lagging leg IGBTs are shown in Figures 6.26 and 6.27, respectively. Also the detailed switching transitions are given in Figure 6.28 for the lagging leg IGBT.

Figure 6.23 Inverter output voltage (yellow), transformer primary current (blue), and transformer secondary voltage (red) waveforms at 15% load (scales: 120 V/div, 2 A/div, 120 V/div, 3 µs/div).

Figure 6.24 Transformer secondary voltage (yellow) and secondary current (red) waveforms at 15% load (scales: 50 V/div, 10 A/div, 3 µs/div).

Figure 6.25 Load current waveform (top) and its vertically zoomed version (bottom) at 15% load (scales: 3 A/div, 500 mA/div, 3 µs/div).

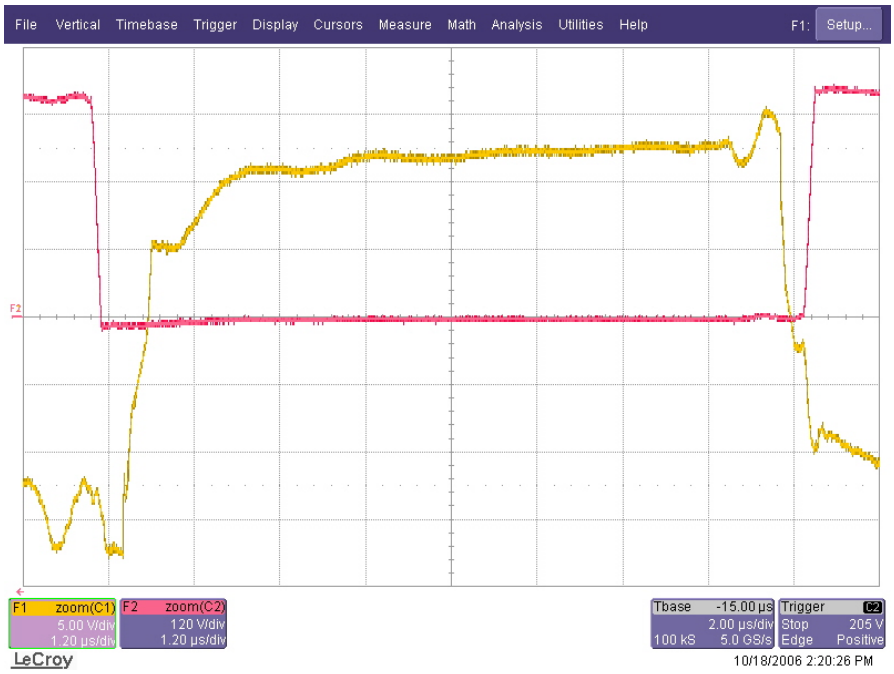


Figure 6.26 Collector-emitter voltage (red) and gate-emitter voltage (yellow) waveforms of the leading leg IGBT (T_4) at 15% load (scales: 120 V/div, 5 V/div, 1.2 µs/div).

Figure 6.27 Collector-emitter voltage (red) and gate-emitter voltage (yellow) waveforms of the lagging leg IGBT (T_2) at 15% load (scales: 120 V/div, 5 V/div, 1.2 µs/div).

Figure 6.28 Collector-emitter voltage (red) and gate-emitter voltage (yellow) waveforms of the lagging leg IGBT (T_2) (top; scales: 120 V/div, 5 V/div, 1.2 µs/div), and the turn-on and turn-off switching transitions of this IGBT (bottom; scales: 120 V/div, 5 V/div, 300 ns/div) at 15% load.

6.3.2 Performance Comparison of the Voltage Clamp Snubbers By Means of Experimental Study

As mentioned before, one problem of the FB-PS-ZVS DC/DC converter is the oscillations on the waveforms, which originate mainly from the resonance between the parasitic components of the transformer and high-frequency rectifier diodes. The resonance between the secondary referred transformer leakage inductance and additional external inductance, and the high-frequency rectifier diode junction capacitances and transformer winding capacitance results in severe overvoltage and oscillations on the secondary voltage waveform, especially due to the Schottky

diodes, which have larger junction capacitance value with respect to the pn-junction diodes. In the manufactured converter, due to the utilized components, which are the Schottky diodes in the high-frequency rectifier and additional external inductor in series with the transformer primary winding, the secondary voltage oscillates as shown in Figure 6.29. This figure is obtained while the input DC voltage is 150 V. Since 400 V input DC voltage results a peak secondary voltage larger than the blocking voltage of the Schottky diodes, higher voltages than 150V were not attempted. As can be observed in the figure, the secondary voltage rises to a peak value of 70 V while it settles at about 34 V. To clamp this overvoltage to a reasonable value, a voltage clamp snubber is utilized.

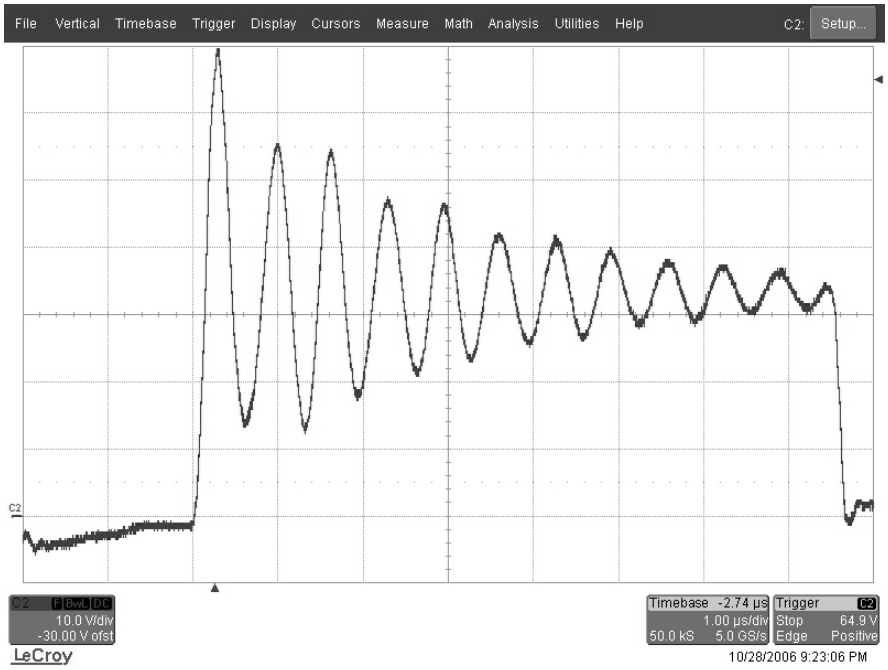


Figure 6.29 The secondary voltage waveform for an input DC voltage of 150 V when no voltage clamp snubber utilized (scales: 10 V/div, 1 μs/div).

Another point to be mentioned in Figure 6.29 is the oscillation period of the secondary voltage. While determining this quantity, the total value of the secondary referred transformer leakage inductance and additional external inductance can be calculated easily and obtained as 1.83 μH for the manufactured system. However, the total equivalent capacitance can not be obtained initially since the equivalent transformer capacitance can not be calculated accurately due to its dependency on

the frequency and temperature. Hence, the total equivalent capacitance, which includes the high-frequency rectifier diode junction capacitances and transformer winding capacitance, can be estimated from the experimental result. From Figure 6.29, the oscillation period is obtained as 600 ns and the resulting total equivalent capacitance is calculated as 5 nF.

In order to suppress the overvoltage at the rectifier output, an RCD type voltage clamp snubber is utilized at the high-frequency rectifier output. The voltage clamp snubber clamps the secondary voltage to an acceptable value. Figure 6.30 shows the configurations of the utilized voltage clamp snubbers for performance comparison.

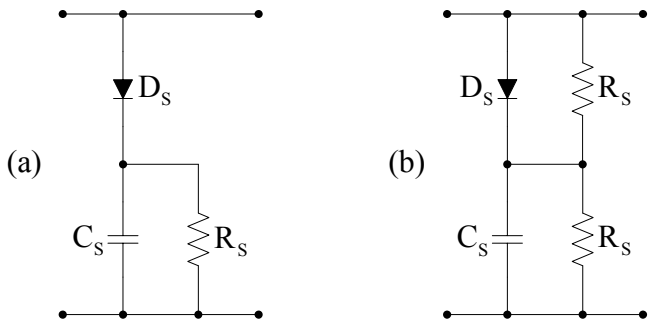


Figure 6.30 Voltage clamp snubbers utilized for performance comparison.

The snubber given in Figure 6.30.a is the conventional RCD voltage clamp snubber configuration, and to obtain further damping, a resistor is connected across the snubber diode additionally as shown in Figure 6.30.b. The performances of the snubbers given in Figure 6.30 are compared experimentally and the results are presented in Figure 6.31. The experiments are carried out with the same DC bus voltage value of 400 V. When the voltage clamp snubber in Figure 6.30.a is utilized at the output of the high-frequency rectifier, the secondary voltage reaches up to 160 V. If the voltage clamp snubber in Figure 6.30.b is utilized, the peak secondary voltage is clamped to 150 V as shown in Figure 6.31. Thus, the snubber configuration given in Figure 6.30.b is utilized in the manufactured FB-PS-ZVS DC/DC converter system since the voltage stress of the rectifier diodes is lower than in other configuration.

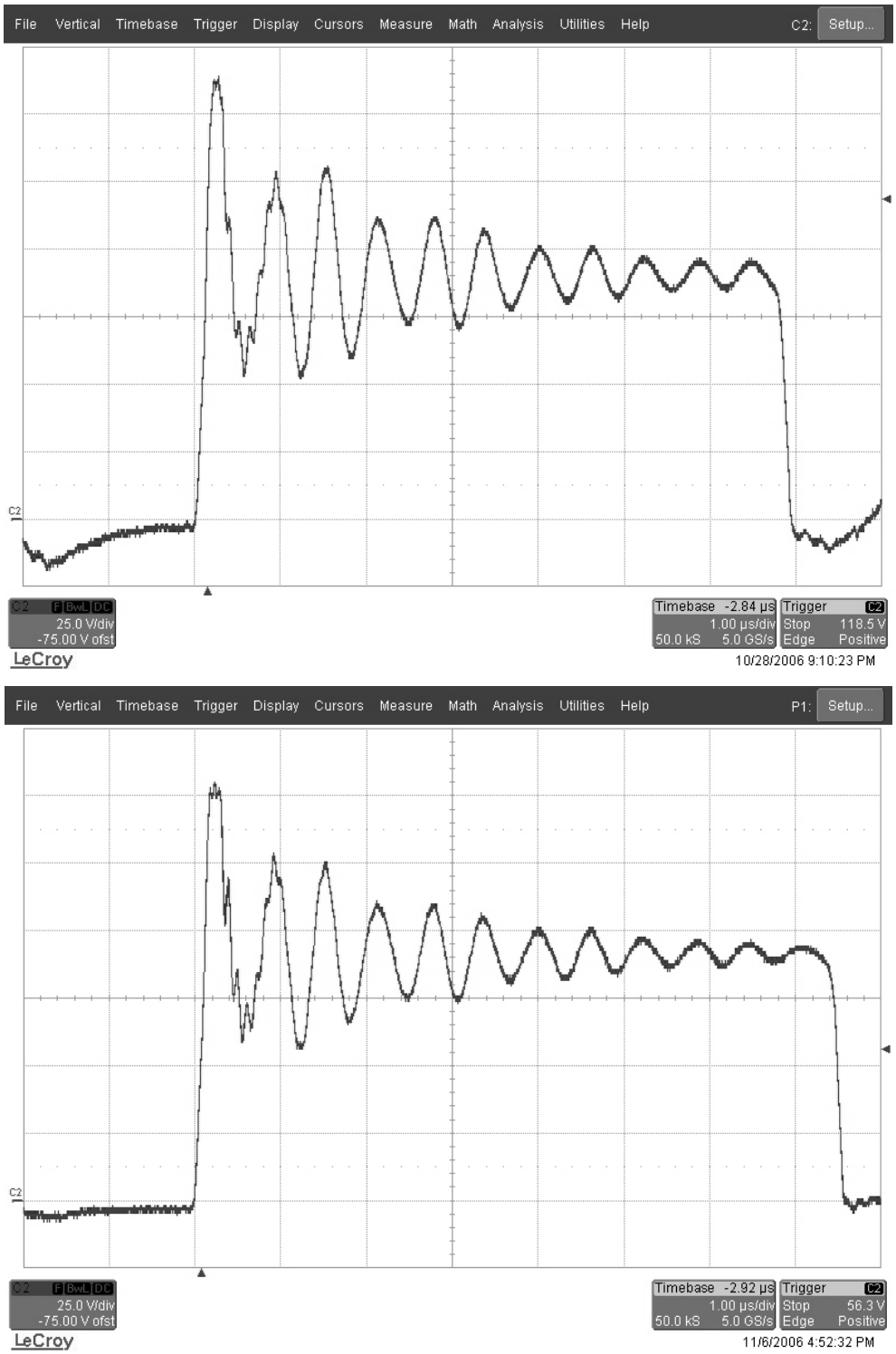


Figure 6.31 The voltage across the high-frequency rectifier output with the snubber in Figure 6.30.a (top), and with the snubber in Figure 6.30.b (bottom) (scales: 25 V/div, 1 µs/div).

6.3.3 Converter Energy Efficiency Verification By Means of Experiments and Comparison with Computer Simulation and Analysis Based Efficiency Estimation Results

In the previous chapter, the computer simulation results were utilized to estimate the converter efficiency and compared with the analytically calculated efficiency values. The resulting efficiency values were presented with respect to the corresponding load conditions in the same graph. In this section, the measured efficiency values of the FB-PS-ZVS DC/DC converter system are inserted additionally in the same graph for the same load conditions. For these four different load current values, the efficiency values are calculated by utilizing the measured DC voltage and current values at the input and output of the system and placed in the same graph that is given in Figure 6.32.

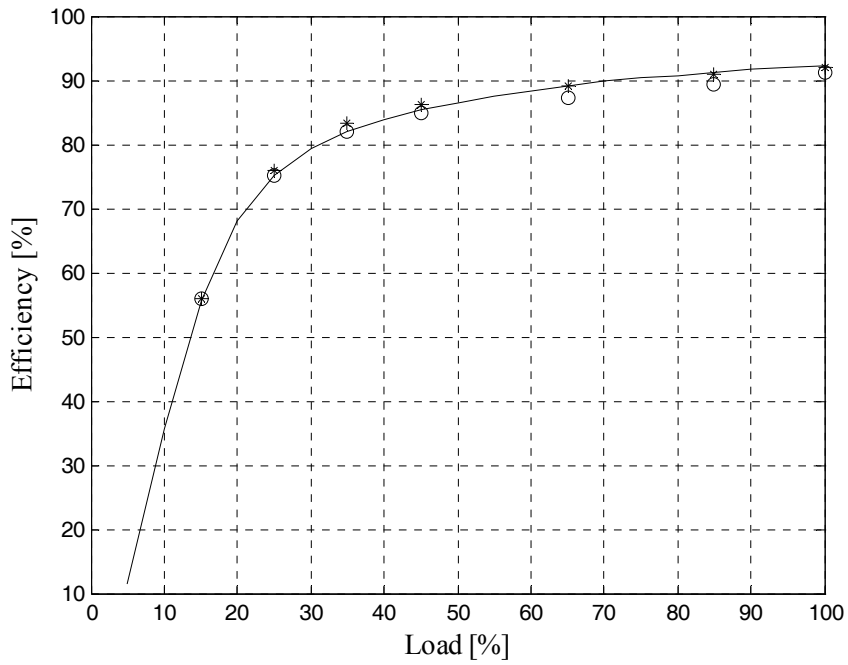


Figure 6.32 Efficiency of the FB-PS-ZVS DC/DC converter obtained from the analytical calculation (solid line), the computer simulation (stars), and the experimental results (circles).

The efficiency of the FB-PS-ZVS DC/DC converter system is high when the ZVS condition is satisfied. Based on the experimental results, the converter efficiency is 80% at the ZVS boundary and reaches to 91% at the rated load condition. Also the measured efficiency values are in strong correlation with the analytical calculation and computer simulation efficiency results.

6.3.4 Experimentally Energy Efficiency Verification of the FB-PS-ZVS DC/DC Converter Considering the Dead-Time Effect and Comparison with Computer Simulation Results

As concluded in Section 5.4 (given in Chapter 5), increasing the dead-time decreases the energy efficiency of the FB-PS-ZVS DC/DC converter, while increasing the reliability of the switching operations of the IGBTs. With a dead-time of 2 μs, the effect of the external capacitance on the efficiency is shown in this section. The simulation results shown in Figure 5.22 for three converter parameter sets (given in Table 5.3) are verified experimentally. The obtained efficiency curves from the simulation and experimental results are shown in Figure 6.33.

On the efficiency curves in Figure 6.33, “o” characters represent the ZVS boundary current values for the corresponding parameter set. The measured efficiency values are in agreement with the computer simulation efficiency results. As can be observed in Figure 6.33, increasing the external capacitance improves the efficiency curve up to the ZVS boundary current value. Also increasing the external capacitance value decreases the ZVS boundary current value resulting in a larger ZVS range, which provides a low noise operation for wider load range.

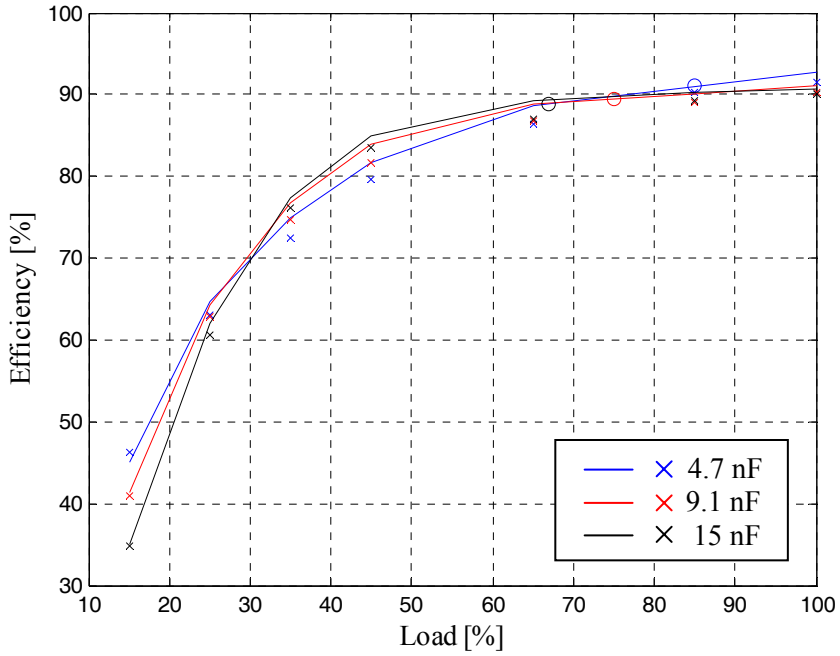


Figure 6.33 Efficiency of the FB-PS-ZVS DC/DC converter obtained from the computer simulation (solid line), and the experimental results (crosses) for various external capacitance values.

6.3.5 Controller Performance Verification By Means of Experimental Study

Performance verification of the output current controller, designed and performance predicted by the computer simulation results in Chapter 5, is carried out with the assistance of the experimental results in this section. The response to load current step command and load resistance step change (disturbance) are investigated experimentally.

First, the load current step command response performance of the designed current controller is presented experimentally. The experimental result is obtained by entering the desired load current command in the DSP programming computer interface, and the resulting load current response is acquired from the scope. A step current command change from 5 A to 100 A is applied to the current controller. The

load current reaches to 100 A in 500 μs as shown in Figure 6.34. Hence, the controller bandwidth is obtained as 2 kHz experimentally. The controlled system responds to the step current command change in a minimum possible time interval, since the calculated time constant of the converter system from Figure 6.34 is similar to the one obtained from the ratio of the load inductance to load resistance (L_O/R_O). As can be observed in Figure 6.34, the load current increases from 5 A to 60 A in 220 μs resulting a time constant of 241 μs. The calculated time constant from the utilized component values is obtained as 235 μs.

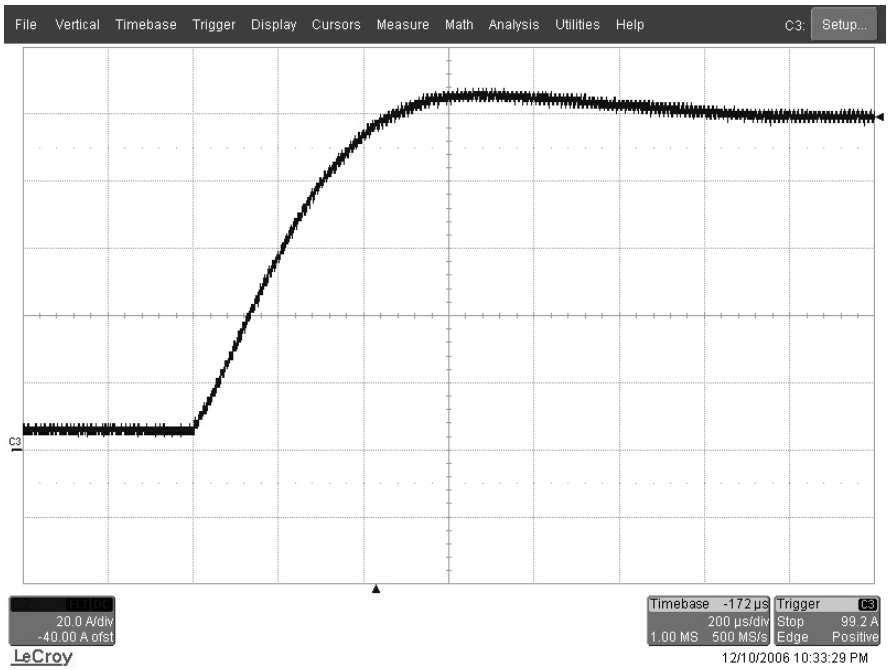


Figure 6.34 Load current waveform with an applied step current command change from 5 A to 100 A (scales: 20 A/div, 200 μs/div).

The experimental result, which verifies the load regulation performance of the controller, is obtained by applying a step change in the load resistance while keeping the load current command value as constant. In the experiment, 50% loading case of the converter system is investigated. The output of the system is loaded with a resistance of 0.8 Ω initially, and then the load current is increased by adding a parallel resistor of 1.6 Ω to the output. This loading case is applied while the load current is 75 A, and the resulting load current waveform is given in Figure 6.35. The

output current settles to the load current command value (75 A) in 700 μs, while the load current overshoot value is measured as 12 A.

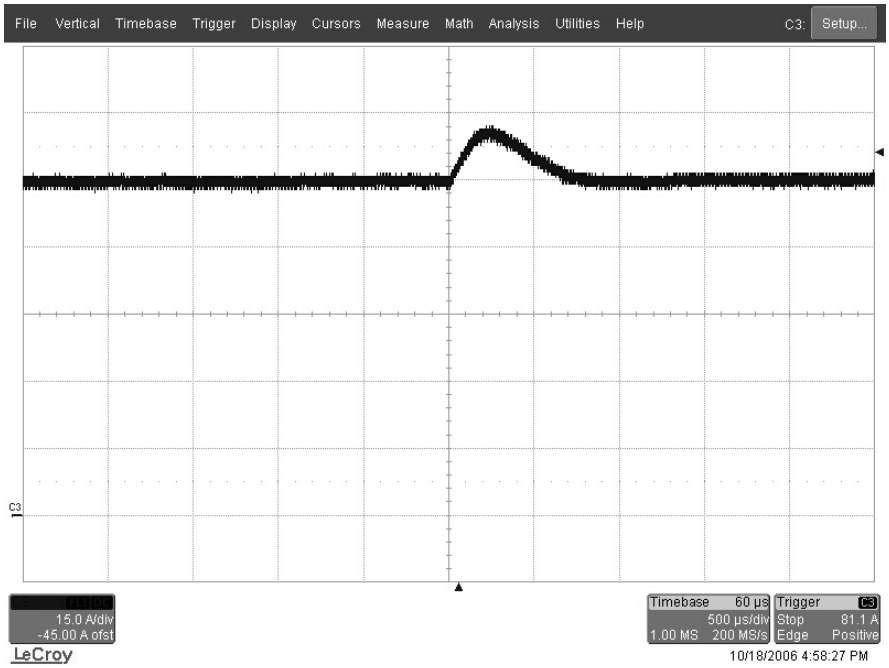


Figure 6.35 Load regulation performance of the output current controller at 75% load (scales: 15 A/div, 500 μs/div).

In this chapter, performance verification of the designed and performance predicted FB-PS-ZVS DC/DC converter regarding the ZVS performance of the switches, voltage clamp snubber performance, power converter efficiency, and output current controller performance are carried out by means of experimental results. Strong correlation between the theory, simulations and experiments is shown.

CHAPTER 7

CONCLUSIONS

In this thesis, a thorough analysis, design, and the practical implementation of the FB-PS-ZVS DC/DC converter for arc welding machine power supply applications is pursued. The thesis provides a methodical design approach yielding accurate converter system parameters for high performance, specifically for high power converters involving a large dead-time.

The first chapter reviews the switch mode power supply technology and reports its advantages. As the specific application area of the FB-PS-ZVS DC/DC converter studied in this thesis, the arc welding process is mentioned and the requirements of an arc welding machine power supply are discussed. As the most favorable power converter topology, the FB-PS-ZVS DC/DC converter is also discussed with its main attributes, including the soft-switching techniques.

The second chapter provides a general switch mode DC/DC converter overview. The popular DC/DC converter topologies and their basic operating principles are reviewed. The suitable converter topology for arc welding application is discussed and the FB-PS-ZVS DC/DC converter is shown to be the best choice. The full-bridge DC/DC converter is reviewed in more detail since it forms the main part of the FB-PS-ZVS DC/DC converter. The phase-shifted PWM method, which is the most favorable PWM scheme for this type of converter to operate under soft-switching condition, is discussed in detail.

In the third chapter, a thorough analysis of the FB-PS-ZVS DC/DC converter operating modes is provided and the circuit behavior is investigated in detail for each operating mode. The load current range for ZVS operation and the DC voltage conversion ratio of the converter are derived also in this chapter. Thus, the influence

of circuit parameters on the converter behavior becomes clearer. Henceforth, a proper design of such a converter is possible.

The fourth chapter is dedicated to the design of a 5 kW FB-PS-ZVS DC/DC converter and the determination of the converter circuit parameters. A methodical design approach is introduced to obtain convenient design parameter sets considering the practical implementation limitations such that the method leads to accurate results. The most favorable design parameter set, which includes the values of the utilized circuit components in the implemented converter, is selected by utilizing the analytical performance evaluation results. The design of the high frequency isolation transformer is given in detail also in this chapter.

The analytical design of the FB-PS-ZVS DC/DC converter system is a complex procedure due to the large number of parameters involved and the interdependence of these circuit parameters. The conventional iterative design procedure is not an appropriate design approach for the power converters employing semiconductor switches which have a significant dead-time constraint. Since a significant dead-time must be introduced between the switching devices due to safety reasons in the high voltage/current switching semiconductor devices (especially for the IGBTs due to tail current), an exhaustive search method based design procedure, which carries out an exhaustive search of the design parameters considering the dead-time constraint, is introduced. The exhaustive search is carried over a predefined parameter range determined by the application requirements. Thus, the parameter search is an efficient approach with a short computational time. The most favorable design parameter set is selected by taking the performed analytical performance evaluation of the design parameter sets into account. As a result, with thorough analysis and methodical design approach, a high performance welding power supply could be developed and manufactured.

The fifth chapter involves detailed computer simulations, which predict the performance of the designed FB-PS-ZVS DC/DC converter system involving a high accuracy system numerical model. A detailed study on the modeling of the FB-PS-

ZVS DC/DC power converter system is carried out to obtain accurate results. The device level model of the semiconductor switches, which performs similar switching characteristics to the utilized switches in the manufactured converter, is utilized in the computer simulation model of the converter power stage. Computer simulation results regarding the converter waveforms and energy efficiency are presented for several load conditions. It is shown that high efficiency and ZVS operation over the predicted load current range can be obtained. Also the effect of the dead-time on the efficiency is investigated by means of computer simulations in this chapter. It is concluded that the large dead-time required for more reliable converter operation has detrimental effect on the converter efficiency performance. The large dead-time results in significant efficiency degradation and the efficiency could not be restored despite serious modifications in the converter resonant component parameters (increasing the external inductance and capacitance values). Thus, the higher energy efficiency requirement which imply small dead-time, and higher shoot-through reliability requirement which implies large dead-time contradict. A compromise between the two gives a practical design point.

Since the FB-PS-ZVS DC/DC converter system is designed to be utilized in a constant current welding machine, the system is controlled by regulating the output current. The controller stage of the closed loop current controlled system is designed by utilizing a linear current controller. First, a reduced order system model is obtained with simplifications on the full system model. Then a linear PI controller based output current compensator is designed by utilizing the simplified system model. With the controller designed, discrete time control system implementation is pursued and the steady-state and dynamic performance of the designed controller are investigated by utilizing the computer simulations.

In the sixth chapter, the predicted performance of the FB-PS-ZVS DC/DC converter system is verified by means of experimental study of a 5 kW converter. The manufacturing steps of the 5 kW FB-PS-ZVS DC/DC converter prototype and the experimental test procedure are reported in detail. The DSP unit, which is utilized for high bandwidth current control, is introduced and the implemented control algorithm

is discussed. Then, the experimental results presenting the converter waveforms for several loading conditions, the measured efficiency values, and the performance of the output current controller are shown. The performance of ZVS operation, controller response, and efficiency were shown to be satisfactory. Also the experimental results are in strong agreement with the analytically calculated and computer simulation results. Therefore, it has been demonstrated that a converter with high energy efficiency (above 80%), high current control bandwidth (2.5 kHz) and small size and weight could be obtained.

A problematic case observed during the experimental studies is the oscillations on the converter voltage and current waveforms. The resonance between the circuit component parasitics at the secondary side (such as high frequency diode junction capacitances, transformer interwinding capacitances, etc.) cause the oscillations on the transformer secondary voltage waveform and affect other waveforms. These oscillations and also the overvoltages could be reduced by lowering the effect of the total junction capacitance of the high-frequency rectifier diodes. This could be achieved by utilizing a center-tap (half-bridge) high-frequency rectifier instead of full-bridge configuration, which has two secondary windings in the transformer. Thus, the number of the diodes in the high-frequency rectifier decreases to half and so does the total diode junction capacitance. In this case the high-frequency rectifier loss is reduced to half also, while the additional secondary winding increases the total loss in the transformer. The resulting converter system could have slightly better efficiency; however, the transformer design becomes complicated due to center-tap configuration in the secondary winding. If pn junction diodes are utilized instead of Schottky diodes, the total junction capacitance value will be further reduced. However, in this case the rectifier conduction loss will increase due to their larger forward voltage value, resulting in lower efficiency.

Another point to be concluded is about the controller of the FB-PS-ZVS DC/DC converter system. This thesis mainly focuses on the analysis, design, and implementation of the power supply of an arc welding machine considering the basic power circuit requirements. The further work could be performed on the controller of

the converter system according to the type of the considered arc welding process and its requirements. This may be a linear or a nonlinear compensator according to its steady-state and dynamic control performance. To construct a convenient and high performance controller, the welding process must be well investigated and its process control behavior must be well understood.

With the application being a constant current welding power supply, this thesis focused on current control mode operation. Thus, the controller study of the thesis was confined to current control. However, the FB-PS-ZVS DC/DC converter has quite wide range of applications, many of which involve voltage mode control. Utilizing the high performance DSP, the output voltage of the converter could be precisely controlled as well. For this purpose the converter topology should be modified and an output LC filter must be designed, a voltage feedback loop must be established along with the controller modifications.

The converter in the laboratory employed separate heatsinks for each power converter module. The IGBT inverter, the high frequency rectifier, and the input AC/DC converter rectifier were all placed on separate heatsinks. The heatsinks should be integrated for the compactness of the system.

The effect of the temperature on the parasitic output capacitance of the IGBT performance and its influence on the switching behavior should be investigated. As the device parasitic capacitances are highly dependent on the operating temperature, their influence on the converter efficiency, heatsink size optimization should be clearly defined for an accurate practical design.

In the laboratory environment due to the limited test environment, a practical arc load test could not be performed and all the tests were conducted utilizing resistive load banks which do not represent the arc load dynamics. A true control design and performance limitations can only then be tested and suitability verified. The arc load test is also left as future work.

The power semiconductor dead-time places significant constraints on the converter energy efficiency performance. The power semiconductor manufacturers do not provide detailed information on the dead-time constraints considering the ZVS operating conditions. Perhaps a more relaxed constraint could be placed on the devices or more suitable devices for ZVS condition could be developed for the ZVS application of the FB-PS-ZVS DC/DC converter. The lack of literature and product manufacturer technical information on this subject indicates knowledge in the area is missing and attention to this field is required.

Based on the above issue, perhaps the power converter efficiency could be improved by providing a voltage feedback information to operate the IGBTs under soft switching reliably. Via a feedback signal, if the zero voltage status of a device is detected, the device could be switched with low stress and low risk of inverter leg voltage shoot-through fault. Zero voltage detection and switching with high speed and accuracy for increased converter energy efficiency are subjects of future research also.

Overall, this thesis provides a thorough analysis, methodical design, and implementation of the FB-PS-ZVS DC/DC converter, which is a favorable converter topology for high power applications due to features such as high efficiency, small size, low weight, low complexity, low EMI, and reduced component stress. The study shows that the inverter dead-time strongly influences the converter energy efficiency performance and the larger the dead-time the poorer the energy efficiency and narrower the ZVS range. The study results are important for converters operating at high voltage and current (typically above several hundred volts and several ten ampers) and utilizing switches such as IGBTs. In such applications, it is shown that the thermal reliability and shoot-through reliability contradict.

All the theory and analytical results developed in this thesis were supported by means of detailed computer simulations and experimental studies, and a strong correlation between the theory and experiments was obtained.

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APPENDIX A

MATLAB CODE FOR THE EXHAUSTIVE SEARCH METHOD BASED DESIGN PROCEDURE

Matlab code utilized for obtaining the design parameter sets by the exhaustive search method based design procedure is given in the following.

```
%-------------------------------------------------------------------
% Exhaustive Search Method Based Design Procedure of
% the FB-PS-ZVS DC/DC Converter
% Author: Mutlu USLU
% Date: September, 2006
%-------------------------------------------------------------------
disp('In this matlab code an analytical design method for');
disp('the FB-PS-ZVS DC/DC Converter is utilized');
disp('to calculate the design parameter sets satisfying');
disp('the maximum critical load and primary current constraints.');
% Input Specifications
Vdc=input('Enter the converter DC input voltage value in V:');
Vo=input('Enter the converter rated DC output voltage value in V:');
Io=input('Enter the converter rated DC output current value in A:');
fs=input('Enter the switching frequency value in Hz:');
td=input('Enter the dead-time value in sec:');
Iocrmax=input('Enter the maximum output critical current value in A:');
Ippkmax=input('Enter the maximum transformer primary peak current value in A:');
% Preliminary calculations for the exhaustive search boundaries and step sizes
domax=1-2*td*fs;  % Step 1: Maximum primary duty cycle value
Nmax=(Vdc*domax)/Vo;  % Step 2: Maximum turns ratio value
```

```
Nmin=0.25*(Vdc/Vo);  % Step 3: Minimum turns ratio value
Nstep=(Nmax-Nmin)/100;  % Turns ratio step size value utilized in the search
Ltmax=((Nmax*Vdc)/(2*Io))*(3/(8*fs)-td);  % Step 4: Maximum Lt value
Ctmin=(1/Ltmax)*(((2*td)/pi)^2);  % Step 5: Minimum Ct value
Ctmax=(1/(3e-6))*(((2*td)/pi)^2);  % Step 6: Maximum Ct value
Cstep=(Ctmax-Ctmin)/200;  % Ct step size value utilized in the search
Ro=Vo/Io;  % Load resistance value
n=0;  % Initialize the convenient design parameter set number
% Loops utilized for the exhaustive search
for k=1:201;
Ct=Ctmin+Cstep*(k-1);  % Ct value for the corresponding search step
Lt=(1/Ct)*(((2*td)/pi)^2);  % Step 7: Lt value for the corresponding Ct
 for i=1:101;
 N=Nmin+Nstep*(i-1);  % Turns ratio value for the corresponding search step
 % Step 8: Critical current value for the corresponding Lt and Ct
 Icr=(sqrt(Ct)*Vdc)/(sqrt(Lt));
 % Step 9: Maximum doeff value for the corresponding search step
 doeffmax=domax/(1+((4*Lt*fs)/(N^2*Ro)));
 % Step 10: Design constraints given in (4.16), (4.17), and (4.18)
   if (doeffmax>((N*Vo)/Vdc))
    if (((Io/N)<Ippkmax)&(Icr<(Iocrmax/N)))
      % The design parameter set satisfies the constraints
      n=n+1;  % Increment the convenient design parameter set number
      Lres(n)=Lt;  % Store Lt value of the design parameter set
      Cres(n)=Ct;  % Store Ct value of the design parameter set
      Nres(n)=N;  % Store N value of the design parameter set
      Iocr(n)=N*Icr;  % Store Iocr value for the corresponding design parameter set
      Ippk(n)=Io/N;  % Store Ippk value for the corresponding design parameter set
    end
   end
 end
end
```

```
% Stored n-design parameter sets are displayed in a 5-columned result matrix
if (n>0)
  for m=1:n;
    Result(m,1)=Lres(m)*1e6;  % First column lists Lt values in µH
    Result(m,2)=Cres(m)*1e9;  % Second column lists Lt values in nF
    Result(m,3)=Nres(m);  % Third column lists turns ratio values
    Result(m,4)=Iocr(m);  % Fourth column lists Iocr values
    Result(m,5)=Ippk(m);  % Fifth column lists Ippk values
  end
  n  % Displays the number of design parameter sets
  Result  % Displays the result matrix
else
disp('No result available for the given constraints!');
end
```

APPENDIX B

MATLAB CODE FOR THE ANALYTICAL EFFICIENCY CALCULATION PROCEDURE

Matlab code utilized for obtaining the efficiency of the FB-PS-ZVS DC/DC converter for the whole load current range is given in the following.

```
%--------------------------------------------------------------------
% Analytically Efficiency Calculation Procedure
% for the FB-PS-ZVS DC/DC Converter
% Author: Mutlu USLU
% Date: September, 2006
%--------------------------------------------------------------------
disp('In this matlab code an analytical efficiency calculation method');
disp('for the FB-PS-ZVS DC/DC Converter is utilized');
disp('for the whole load current range.');
% Input Specifications
Vdc=input('Enter the converter DC input voltage value in V:');
Vo=input('Enter the converter rated DC output voltage value in V:');
Io=input('Enter the converter rated DC output current value in A:');
fs=input('Enter the switching frequency value in Hz:');
Lo=input('Enter the output filter inductance value in H:');
Lt=input('Enter the total resonant inductance value in H:');
Ct=input('Enter the total resonant capacitance value in F:');
N=input('Enter the turns ratio value:');
Vcesat=input('Enter the IGBT on state voltage drop value in V:');
Vfwd=input('Enter the freewheeling diode forward voltage drop value in V:');
Rw=input('Enter the primary referred equivalent winding resistance value in ohms:');
```

```
Pcxfmr=input('Enter the transformer core loss value in W:');
Vrd=input('Enter the rectifier diode forward voltage drop value in V:');
% Preliminary calculations
Ro=Vo/Io;  % Load resistance value
Icr=(sqrt(Ct)*Vdc)/(sqrt(Lt));  % Critical current value
dlf=1+((4*Lt*fs)/(N^2*Ro));  % Duty cycle loss factor
% Loop utilized for the efficiency calculation
for i=1:20;
Iox=5*i;  % Load current value for the corresponding step
Vox=Ro*Iox;  % Output voltage value for the corresponding step
doex=(Vox*N)/Vdc;  % doeff value for the corresponding step
dox=doex*dlf;  % do value for the corresponding step
dlx=dox-doex;  % Duty cycle loss value for the corresponding step
dIox=(((Vdc-2*Vcesat)/N-2*Vrd-Vox)*doex)/(2*Lo*fs);  % Load current ripple
m1x=Vdc/Lt;  % m1 slope value given in (4.37)
m2x=(Vdc-N*Vox)/(N^2*Lo);  % m2 slope value given in (4.38)
m3x=(N*Vox)/(N^2*Lo);  % m3 slope value given in (4.39)
I1x=(Iox-dIox/2)/N;  % IP1 value shown in Figure 4.4
I2x=(Iox+dIox/2-((Vox*(1-dox))/(2*Lo*fs)))/N;  % IP2 value shown in Figure 4.4
Ax=0.5*m1x*fs*((I1x+I2x)/(2*m1x)-dlx/(4*fs))^2;
Bx=(0.5*doex*I1x)+((m2x*doex^2)/(8*fs));
Cx=(0.5*(1-dox)*I2x)+((m3x*(1-dox)^2)/(8*fs));
Dx=0.5*m1x*fs*((I1x+I2x)/(2*m1x)+dlx/(4*fs))^2;
Pt1x=Vcesat*(Ax+Bx);  % Power loss of the IGBT T1 (or T4) given in (4.32)
Pd1x=Vfwd*(Cx+Dx);  % Power loss of freewheeling diode D1 (or D4) given in
(4.34)
Pt2x=Vcesat*(Ax+Bx+Cx);  % Power loss of the switch T2 (or T3) given in (4.33)
Pd2x=Vfwd*Dx;  % Power loss of the freewheeling diode D2 (or D3) given in (4.35)
Pcinvx=2*(Pt1x+Pt2x+Pd1x+Pd2x);  % Total power loss of the full-bridge inverter
Kx=(m1x^2*dlx^3)/(12*fs^2)-(m1x*I2x*dlx^2)/(2*fs)+I2x^2*dlx;
Lx=(m2x^2*doex^3)/(12*fs^2)+(m2x*I1x*doex^2)/(2*fs)+I1x^2*doex;
Mx=(m3x^2*(1-dox)^3)/(12*fs^2)+(m3x*I2x*(1-dox)^2)/(2*fs)+I2x^2*(1-dox);
```

```
Iprmsx=sqrt(Kx+Lx+Mx);  % Transformer primary current rms value
Pxfmrx=Rw*Iprmsx^2+Pcxfmr;  % Total power loss of the transformer
Pcdrcx=4*(0.5*Vrd*Iox);  % Total conduction power loss of the full-bridge rectifier
Phslx=0;
if (I2x<Icr)  % Hard-switching loss is calculated if IP2 value is below Icr value
  dVx=Vdc-I2x*sqrt(Lt/Ct);  % Voltage across the IGBT for the hard-switching case
  Phslx=fs*Ct*dVx^2;  % Hard-switching loss value
end
Pltotx=Pcinvx+Pxfmrx+Pcdrcx+Phslx;  % Total power loss of the converter system
Pox(i)=Vox*Iox;  % Output power of the converter system
Io(i)=Iox;
eff(i)=(100*Vox*Iox)/(Vox*Iox+Pltotx);  % Efficiency of the converter system
end

figure(1)
plot(Io,eff);  % Plot efficiency vs. load current curve
grid on;
```