Course Information

Course Code	5670446
Course Section	1
Course Title	COMPUTER ARCHITECTURE II
Course Credit	4
Course ECTS	7.0
Course Catalog Description	Arithmetic processor design, arithmetic algorithms. Memory organization, parallel processing, multiprocessors systems. Peripheral organization. I/O processing. I/O controllers.
Prerequisites	Students must complete one of the following sets to take this course.

Set	Prerequisites
1	5670445

Schedule	Tuesday , 09:40 - 10:30, EA208
	Thursday , 09:40 - 11:30, EA208
Course Website	All course materials will be on odtuclass.

Instructor Information

Name/Title	Prof.Dr. ŞENAN ECE SCHMİDT
Office Address	A-402
Email	eguran@metu.edu.tr
Personal Website	http://users.metu.edu.tr/eguran/
Office Phone	210 4405
Office Hours	None

Tentative Weekly Outline

Week	Topic	Relevant Reading	Assignments
1	Introduction- ARM Single-cycle		
2	ARM Single-cycle		
3	ARM Single-cycle		
4	ARM Multi-cycle		
5	ARM Multi-cycle		
6	ARM Pipelined		
7	ARM Pipelined		
8	Arm Pipelined Branch Prediction		
9	Memory Organization Cache		
10	Memory Organization Cache		

Week	Topic	Relevant Reading	Assignments
11	Memory Organization VM		
12	Memory Organization		
13	Advanced Topics		
14	Advanced Topics		

Course Textbook(s)

Harris & Harris, "Digital Design and Computer Architecture. ARM Edition", 1st Ed., Kaufmann, 2015.

Computer Architecture, A Quantitative Approach, 6th Edition, John Hennessy, David Patterson

Course Grading

Deliverable	Grade Points
3 short exams, equal weight	30
Laboratory and Class Project	40
Final	30
Bonus for attendance >=80%	5
Total	105