Course Information

Course Code	5670445
Course Section	1
Course Title	COMPUTER ARCHITECTURE I
Course Credit	3
Course ECTS	5.0
Course Catalog Description	Asynchronous logic system. Algorithmic state machines. CPU organization. Construction of arithmetic logic unit. Process control architectures. Instruction modalities. Microprogramming. Bit slicing.
Prerequisites	Students must complete one of the following sets to take this course.

Set	Prerequisites
1	5670348

Schedule	Monday , 11:40 - 12:30, EA208 Wednesday, 09:40 - 11:30, EA208
Learning Management System	odtuclass

Instructor Information

Name/Title	Prof.Dr. ŞENAN ECE SCHMİDT
Office Address	A-402
Email	eguran@metu.edu.tr
Personal Website	http://users.metu.edu.tr/eguran/
Office Phone	210 4405
Office Hours	None

Course Assistants

Name/Title	Araş.Gör. DOĞU ERKAN ARKADAŞ
Office Address	
Email	
Office Hours	

Course Objectives

Provide the students with an understanding of the analysis and synthesis of asynchronous sequential digital systems.

Provide the students the top-down digital system design procedure using algorithmic state machine approach and in dept understanding of basic computer architecture in register and instruction execution phases levels.

Instructional Methods

In-class lectures, problem solving and Q&A sessions

Video lectures recorded for the previous years.

Lecture notes and supplementary material on odtuclass

Tentative Weekly Outline

Week	Topic	Relevant Reading	Assignments
1	**Topics** • Introduction, EE348 Review • Algorithmic State Machines (ASM), Register Transfer Level Language (RTL): Completed with Short Exam 1 • Hardware Description Languages: Completed with Short Exam 2 • Basic Computer: Completed with Short Exam 3 • Microprogrammed Control: Completed with Short Exam 4 • Arithmetic Processor Design: Completed with Short Exam 5 • ARM ISA		Verilog implementation of the Basic Computer

Course Textbook(s)

Mano, “Computer System Architecture”, 3rd Ed., Prentice Hall, 1992

Mano, “Computer System Architecture”, 2nd Ed., Prentice Hall, 1982

Mano “Digital Design”, 4th Ed., Prentice Hall, 2006.

Supplementary Readings / Resources / E-Resources

Readings

Harris & Harris, ?Digital Design and Computer Architecture. ARM Edition?, 1st Ed., Kaufmann, 2015. (Text book of EE446)

Logic & Computer Design Fundamentals 5th Edition by M. Morris Mano, Charles Kime, Tom Martin, 2015

Computer Architecture: A Quantitative Approach (The Morgan Kaufmann Series in Computer Architecture and Design) 6th Edition, by John L. Hennessy David A. Patterson

Computer Organization and Design ARM Edition: The Hardware Software Interface (The Morgan Kaufmann Series in Computer Architecture and Design) by David A. Patterson, John L. Hennessy, 2017

William Stallings Computer Organization and Architecture, 11th edition Pearson, 2019

Assessment of Student Learning

Assessment	Dates or deadlines
Short Exams, Final Exam, HDL Short Exam and Homework All exams are face-to-face in class.	

Course Grading

Deliverable	Grade Points
Four Short Exams	52
Final Exam	36
HDL Short Exam and Homework	12
Total	100