Zero State Doped Turbo Equalizer

Orhan GAZI∗, is with Electronics and Communication Engineering Department, Cankaya University, 06530, Ankara, Turkiye (e-mail: o.gazi@cankaya.edu.tr). Tel: +90 3122844500/4015. Fax: +90 3122848043
A. Özgür YILMAZ, is with Electrical and Electronics Engineering Department, Middle East Technical University, 06530, Ankara, Turkiye (e-mail: aoyilmaz@eee.metu.edu.tr) Tel: +90 3122102337. Fax: +90 3122101261.

Abstract—Although iterative equalizers perform well at low signal to noise ratios, high latency is a major disadvantage for their use in practical communication systems. In this article we propose zero state doped turbo equalizers (ZSDTEs) which can be processed in parallel and have significantly reduced processing delays. The proposed technique shows better performance when compared to the sliding window method.

Index Terms—Turbo Codes, Turbo Equalizer, Zero State Doped Turbo Equalizer.

I. INTRODUCTION

MANY communication systems suffer from inter-symbol interference (ISI) in frequency selective channels. A channel equalizer is usually employed at the receiver side to estimate the data and alleviate the effect of ISI. Traditional equalizers are linear filters whose parameters are determined according to some optimization criteria such as zero forcing (ZF), minimum mean square error (MMSE) etc. With the invention of the turbo codes in 1993 [1] iterative algorithms gained much popularity among communication society. The iterative approach was extended to channel equalization in [2] where turbo equalizer was introduced.

Turbo equalization is the process of combining channel and decoding operations in an iterative manner. The information produced in the decoders and equalizers are traded back and forth to enhance the overall performance. A turbo equalizer (TE) system usually employs soft-input, soft output (SISO) algorithms at the decoder and equalizer block. The popular SISO algorithms employed are usually the maximum a posteriori (MAP) and Viterbi based algorithms which are sequential in nature. However, sequential solutions such as MAP and soft output Viterbi suffer from high complexity and high latency which is a limiting factor in practical applications.

To reduce complexity and the large latency, a number of algorithms to use at the equalizer block have been suggested in [3] where minimum mean square error (MMSE) equalizer is used at the equalizer block. However, its performance degrades seriously in severe ISI cases [4]. A joint structure that combines coding and equalization different than turbo equalization is suggested in [5] where decision feedback equalizer soft information is exchanged with the decoder hard decisions in an iterative manner. Although the use of the sub-optimum algorithms results in reduced complexity, the performance loss cannot be tolerable for some cases [4].

Turbo product codes based on convolutional codes are studied in detail in [6]. We extend the idea in [6] and use it for turbo equalizer. We introduce ZSDTE structure which uses trellis based optimal decoding algorithms and is very suitable for parallel processing at the receiver side. ZSDTE has significantly low latency compared to the classical turbo equalizer structure and at the same time exhibits the same performance. We also compared our system performance to that of the well known sliding window technique [7].

The outline of the paper is as follows. In Section II, the structure of a communication system is explained. ZSDTE model is introduced in Section III. Section IV provides a discussion on the latency gain of the proposed structure. Finally, simulation results and conclusions are given in Sections V and VI.

II. COMMUNICATION SYSTEM MODEL

The transmitter and receiver sides of a communication system that sends data through a frequency selective channel is depicted in Figs. 1 and 2. The channel is also included in the transmitter side for ease of representation. In the transmitter model, the transmit filter, the channel, and the receive filter were incorporated into the ISI channel model which is represented by a discrete time linear traversal filter with the finite length impulse response given by [8]

\[ h[n] = \sum_{k=0}^{L_c-1} h_k \delta[n - k] \]

where \( h_k \) are the filter coefficients and \( L_c \) is the filter length which is known at the transmitter side. The channel coefficients \( h_k \) are time invariant and are available at the receiver.

To mitigate the effects of the ISI at the receiver,
decoding and equalization operations are combined such that soft information exchange among blocks occurs. This iterative structure is called the turbo equalizer which is depicted in Fig. 3. Although we have used MAP algorithm for both equalizer and decoder blocks in Fig. 3 any SISO algorithm can be adopted for both blocks.

Fig. 3. Turbo equalizer. y is the received signal. L_3, L_1, L_2, L_3, L_4 and L_5 denote log-likelihoods.

III. ZERO STATE DOPED TURBO EQUALIZER (ZSDTE)

Trellis termination bits are added to the binary information bits in a periodic manner so that the trellis diagram of the convolutional encoder visits the zero state periodically. The same procedure is repeated for the ISI channel input symbol sequence, i.e., trellis termination symbols are inserted in a periodic manner into the BPSK modulated code sequence. Hence, the ISI channel trellis is also periodically terminated. This procedure is illustrated in Fig. 4. This approach can also be interpreted as pre-coding. The binary information sequence is pre-coded and then passed through a convolutional encoder. The encoded binary data is binary phase shift keying (BPSK) modulated. The BPSK symbol sequences are pre-coded and passed through an ISI channel. White Gaussian noise with double sideband power spectral density N_0/2 is added to the channel output. The pre-coding effectively divides the incoming sequence of blocks into smaller blocks which can be processed separately by multiple equalizers and decoders in a parallel manner at the receiver side. To clarify the pre-coding operation further, an equivalent representation that better illustrates the overall operation in Fig. 4 is explained in the following section.

A. Transmitter Side Equivalent Model

The zero ZSDTE model in Fig. 4 may seem complex in the first look. However, the same system can be expressed with a simplified model. This model is depicted in Fig. 5. As it is seen from the Fig. 5, serial to parallel (S/P) and parallel to serial (P/S) converters are employed. All of the outer constituent encoders add trellis termination bits to the coded data sequences. Inner ISI channel trellises are also terminated. Such a scheme may be impractical for long channel impulses since trellis termination reduces the rate significantly. This transmitter side equivalent model enables us for parallel decoding and equalization operations at the receiver side.

Fig. 4. Zero state doping process at the transmitter side. t_c and t_s are the trellis termination bits and symbols respectively.

Fig. 5. Parallel equivalent model. N is the number of constituent encoders in outer cluster, M is the number of parallel ISI channels.

B. Parallel Decoding and Equalization

The parallel turbo equalizer structure for the proposed system is illustrated in Fig. 6. As it is very obvious from the Fig. 6, equalizers Eq_1..Eq_M and decoders D_1..D_N can run in parallel. This reduces the processing delay enormously.

Fig. 6. Parallelized iterative equalization and decoding. y is the received signal. L_3, L_2, L_1, L_4 and L_5 are the log-likelihoods. INT is the interleaver, D-INT is the de-interleaver. M is the number of MAP equalizers, N is the number of decoders.

IV. LATENCY GAIN

The latency gain will be computed assuming that the log-MAP algorithm [1] is used in both the equalizer and decoder structures. Both the component codes and the channel have memory 2. Assume that BPSK modulation is used. The input sequence length of the channel is twice that of the convolutional code. In a classical turbo equalizer, for an input information sequence of length L two log-MAP units are needed. Let c be the complexity amount and t be decoding latency of a single stage of the code trellis. The equalizer log-MAP unit has a complexity of 2L \times c and a time delay of 2L \times t, the decoder log-MAP unit has a complexity of L \times c and latency of L \times t. The total complexity is of 3L \times c and the total latency is of 3L \times t. For ZSDTE structure, assuming that the number of outer and inner branches equal N, the outer equalizer block, ignoring the trellis termination bits, has a total complexity of 2L \times c and a time delay of (2L/N) \times t, and the inner decoder block again ignoring the trellis termination bits has a total complexity of L \times c and latency of (L/N) \times t. The total latency is of (3L/N) \times t.
Hence, although the complexities are the same in both the classical turbo equalizer and ZSDTE, the latter has a latency gain of $N$. This is a big advantage in communication systems.

V. SIMULATION RESULTS

We use RSC $(1, 5/7)_{\text{octal}}$ for the outer code. An $S$-random (S=18) interleaver is employed between the convolutional encoder and BPSK modulator. The three tap ISI channel model in [8] is adopted. The channel coefficients are $h_0 = 0.407$, $h_1 = 0.815$ and $h_2 = 0.407$. The log-MAP algorithm is used for both the decoder and equalizer blocks. Trellis termination bits were taken into account while computing the overall rate and thus the energy per bit. Input information frame length is chosen as 1024 bits. Twelve iterations are performed for each frame. For statistical significance, simulations were run until at least 60 erroneously decoded frames have been observed. The number of outer and inner branches were chosen equal, i.e., $N=M=1$, $N=M=4$, $N=M=16$. The asymmetric case was also considered, i.e., $N$ value changes and $M=1$ fixed. We also simulated turbo equalizer using the sliding window method in [7]. The performance graphs are shown in Figs. 7, 8, and 9. As seen from Figs. 7 and 8, ZSDTE shows very close performance to that of the classical turbo equalizer for even large $N$ and $M$ values, i.e., $N=M=16$. As the number of branches increases, BER and FER performance degrade slightly. As it is obvious from the figures, ZS doping method shows better performance than the sliding window technique. The simulation results for the asymmetric situation is depicted in Fig. 9. It is seen that the performances are quite comparable.

VI. CONCLUSION

The ZSDTE structure was introduced. It was shown by simulation results that the proposed system shows almost the same performance as that of the classical turbo equalizer even for large number of parallel branches. In addition, the proposed system is very suitable for parallel processing. Hence, it has very low latency compared to the classical turbo equalizer.

REFERENCES


